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Gate-Tunable Semiconductor Heterojunctions from 2D/3D van der Waals Interfaces

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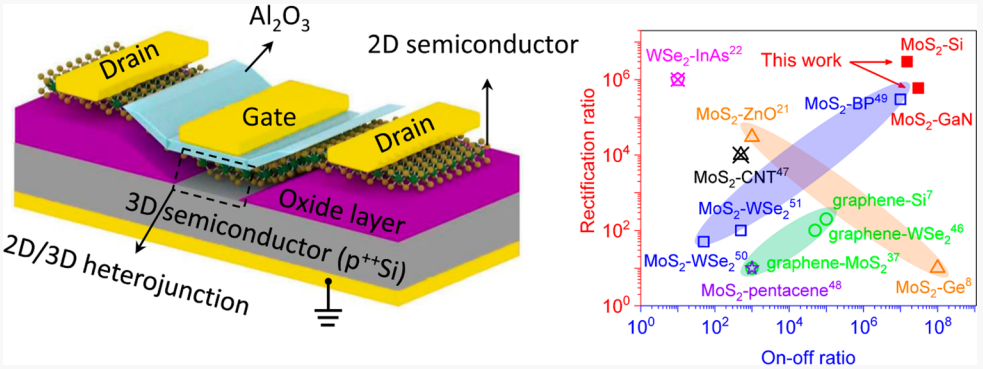

ABSTRACT: van der Waals (vdW) semiconductors are attractive for highly scaled devices and heterogeneous integration as they can be isolated into self-passivated, two-dimensional (2D) layers that enable superior electrostatic control. These attributes have led to numerous demonstrations of field-effect devices ranging from transistors to triodes. By exploiting the controlled, substitutional doping schemes in covalently bonded, three-dimensional (3D) semiconductors and the passivated surfaces of 2D semiconductors, one can construct devices that can exceed performance metrics of "all-2D" vdW heterojunctions. Here, we demonstrate 2D/3D semiconductor heterojunctions using MoS_2 as the prototypical 2D semiconductor laid upon Si and GaN as the 3D semiconductor layers. By tuning the Fermi levels in MoS_2, we demonstrate devices that concurrently exhibit over 7 orders of magnitude modulation in rectification ratios and conductance. Our results further suggest that the interface quality does not necessarily affect Fermi level tuning at the junction, opening up possibilities for novel 2D/3D heterojunction device architectures.

KEYWORDS: *van der Waals, transition metal dichalcogenides, gallium nitride, silicon, gate-tunable, heterostructure*

INTRODUCTION

The advent of van der Waals (vdW) materials has renewed enthusiasm in novel device designs for highly scaled field-effect devices.[1−6] This is in part due to the atomically thin two-dimensional (2D) bodies and self-passivated surfaces that allow superior electrostatic control over all known covalently bonded three-dimensional (3D) semiconductors.[7,8] This self-passivation in vdW materials arises from the nature of their binding, where the surface atoms in each layer have no unsaturated orbitals and hence show no tendency toward chemical bonding or reactions with the neighboring medium. As a consequence, it is significantly easy to embed a vdW 2D semiconductor between metal gates separated by thin dielectrics for strong electrostatic modulation. However, Si and III−V technology is very mature, and therefore the introduction of new materials is a significant challenge. Further, vdW materials with band gap values and material quality comparable to that of Si or III−V materials are not readily available.[9] In addition, stable, complementary doping in vdW semiconductors remains a persistent challenge which prevents the realization of low-power circuits.[10−15] Conversely, 3D semiconductors have well-established and stable complementary doping schemes available. However, the lack of self-passivated interfaces and bulk structure prevents superior electrostatic modulation in a planar geometry.[16,17] Therefore, there exists an opportunity to combine 2D materials with 3D semiconductors to explore fundamental charge-transport phenomena at their interfaces and exploit them for devices.[18] This approach is particularly appealing as it is easy to transfer 2D vdW layers on 3D surfaces, which can, in turn, help passivate the 3D surface due to the inert chemical nature of the

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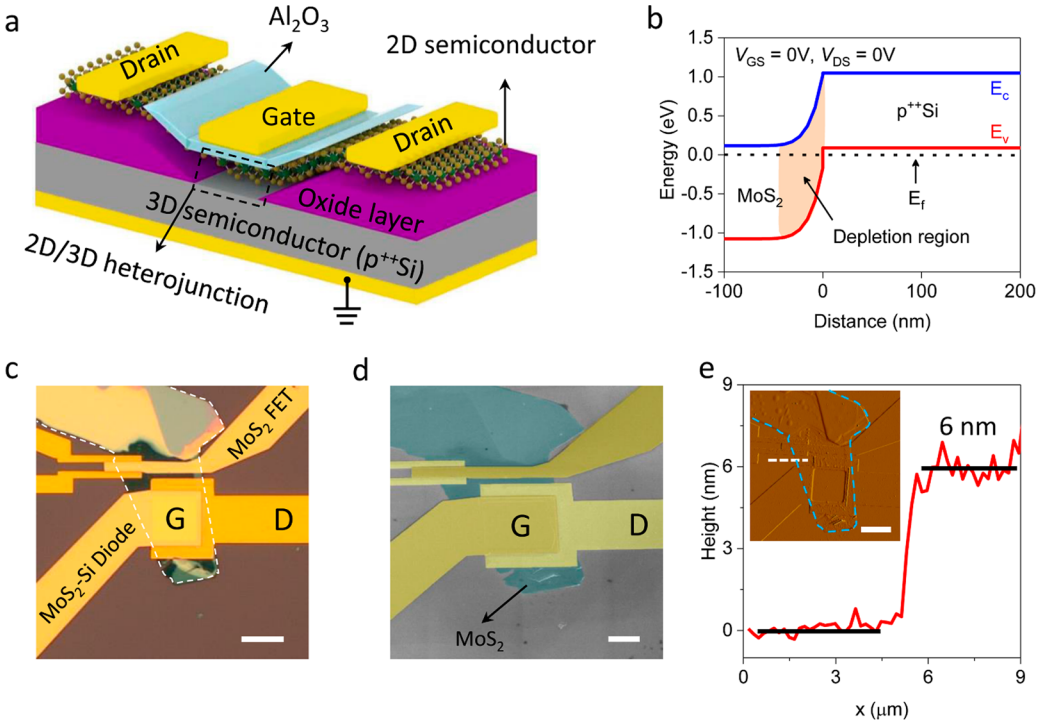

Figure 1. 2D/3D heterojunction diode and characterization. (a) Schematic illustration of a gate-tunable diode based on 2D MoS_2 and 3D Si van der Waals heterostructure. The 2D layer drapes over the etched oxide recess to form direct contact with the 3D semiconductor wafer, as indicated with the dashed line box. Source and drain electrodes comprise Ti/Au (10 nm/40 nm). The gate oxide is 30 nm of Al_2O_3 *via* atomic layer deposition, and the gate electrode is also Ti/Au (10 nm/40 nm). (b) Simulated band diagrams of $p^{++}Si$-MoS_2 heterojunction diodes under equilibrium showing conduction band (E_c), valence band (E_v), Fermi level (E_f), and depletion region. Si band gap (E_g) = 1.1 eV, MoS_2 band gap (E_g) = 1.2 eV, Si electron affinity (χ) = 4.01 eV, MoS_2 electron affinity (χ) = 4.1 eV. (c) Optical micrograph of a representative $p^{++}Si$-MoS_2 heterojunction diode. MoS_2 flake is indicated by a white dashed line. Scale bar, 10 μm. (d) False-colored scanning electron microscopy image of the device. MoS_2 flake and electrodes are indicated by light blue and yellow color, respectively. Gate (G) and drain (D) electrodes are appropriately labeled, whereas the source electrode is the $p^{++}Si$ substrate. Scale bar, 5 μm. (e) AFM height profile across the MoS_2 flake as measured from a topography map. The inset provides the device AFM tip amplitude image concurrently acquired with the topography image, with the corresponding height profile region indicated by the white dashed line. The MoS_2 flake is indicated by a blue outline. Scale bar, 10 μm.

2D layers, thereby forming an electronically active interface.[7,8] Further, this also opens avenues to vertical integration of more devices on top of a fully fabricated 3D complementary metal–oxide semiconductor (CMOS) platform.[19,20] Along these lines, several approaches have been adopted for varying purposes, ranging from low-power to high-current modulation switching.[7,8,21,22] However, few efforts exist in making high-performance switching devices from 2D/3D heterojunctions. Early attempts to interface graphene with 3D semiconductors, although successful, have been limited in performance due to the limited barrier height between semimetallic graphene and the 3D semiconductor.[7,23] Other approaches have been limited to exploiting low-power operation or tunneling phenomena and photoresponse in two-terminal devices.[24−29] Overall, the advantage of using ultrathin 2D materials and exploiting their field tunability has not been systematically investigated and exploited.

In this work, we address this challenge by fabricating three-terminal, gate-tunable diodes (triodes) comprising monolayer to few-layer MoS_2 as the 2D semiconductors and degenerately doped Si and GaN as the 3D semiconductors. At the interface of these junctions, we demonstrate that Fermi level is tunable in the MoS_2 to achieve highly tunable rectification ratios across 7 orders of magnitude, that is, from 0.1 to 10^6. Concurrently, we have also demonstrated that these triodes can effectively serve the purpose of a switching device with on/off ratios exceeding 10^7. Our results suggest that the 2D/3D semiconductor heterojunction system is highly tunable, nearly ideal, and effective for electronic applications despite the lack of perfect passivation at the interface. Given the hybrid nature of the device, it can serve the function in both switching and rectifying applications. Therefore, this device opens new possibilities of using hybrid architectures such as diode transistor logic (DTL)[30,31] and other hybrid logic concepts,[32] all integrated on top of the Si CMOS. With a wealth of 2D semiconductors now isolated, combined with the availability of controlled complementary doping in 3D semiconductors, in addition to epitaxial liftoff[33,34] and remote-epitaxy-enabled layer transfer[35] techniques, our work opens up new opportunities in high-performance and multifunctional heterostructure devices for vertical integration on conventional semiconductor architectures.

RESULTS AND DISCUSSION

We begin by fabricating devices on highly doped wafers of silicon or galium nitride. Figure 1a shows the schematic of a p–n heterojunction consisting of a 2D/3D vdW heterostructure between a few-layer MoS_2 (n-type) and degenerately p-doped Si covered with an alumina gate dielectric and metal electrodes. Details of the microfabrication processes are provided in the Supporting Information (SI) (Materials and Methods and Figures S1 and S2). A finite-element simulation of this heterojunction system shows that the band diagram of

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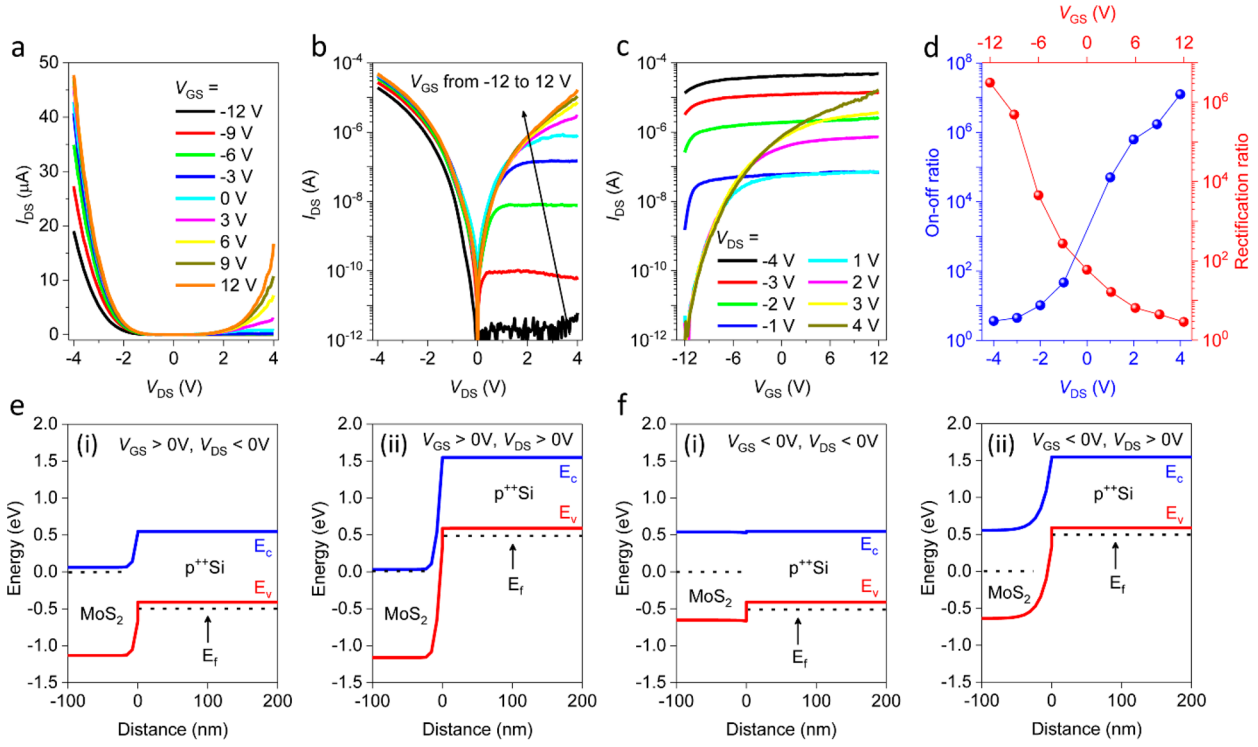

Figure 2. Room-temperature electrical characterization of $p^{++}Si$-MoS_2 heterojunction diodes. (a) Linear scale output characteristics of the device at various gate voltages, showing a clear transition from a highly diode-like rectifying behavior at $V_{GS} = -12$ V to an almost symmetric $I_{DS}-V_{DS}$ behavior at $V_{GS} = 12$ V. The drain bias is on MoS_2, and the contact to $p^{++}Si$ (source) is grounded. (b) Semilogarithmic scale output characteristics of the device. V_{GS} varies in the range of −12 to +12 V, with a step size of 3 V. The highly rectifying behaviors of the $I-V$ characteristic in addition to exponential modulation of reverse saturation current with V_{GS} can be seen. (c) Transfer characteristics of the device at various drain biases. The characteristics show a clear n-type transistor behavior. The high on/off ratio at $V_{DS} > 0$ V and negligible modulation at $V_{DS} < 0$ V can be seen. (d) Device on/off ratio versus V_{DS} (blue) and rectification ratio versus V_{GS} (red). (e) Simulated band diagrams of the $p^{++}Si$-MoS_2 heterojunction for (i) $V_{GS} > 0$ V and $V_{DS} < 0$ V and (ii) $V_{GS} > 0$ V and $V_{DS} > 0$ V. (f) Simulated band diagrams of the $p^{++}Si$-MoS_2 heterojunction for (i) $V_{GS} < 0$ V and $V_{DS} < 0$ V and (ii) $V_{GS} < 0$ V and $V_{DS} > 0$ V.

the $p^{++}Si$-MoS_2 ($p^{++}Si$ resistivity ≤0.005 ohm·cm) heterojunction p−n diode (Figure 1b) is a type-II junction under equilibrium. Based on known work functions and electron affinities,[36−39] the $p^{++}Si$ conduction band lies above the MoS_2 conduction band. Further, owing to the degenerately doped nature of Si, the depletion width exclusively resides within the MoS_2 part with the width equaling ∼50 nm in our simulation. The alignment and widths agree well with previously reported values.[22,40] This observation also suggests that the MoS_2 (∼6 nm) used in our devices must be completely depleted in the entire overlapping junction region with $p^{++}Si$. However, a small depletion region of ∼50 nm may exist within the MoS_2 flake at the boundary of the junction with Si. Other structural characterizations including optical and electron microscopy suggest the clear formation of heterojunction regions (Figure 1c,d). Topography analysis by atomic force microscopy (AFM) reveals the thickness of the MoS_2 layer (∼6 nm, Figure 1e), whereas the spatial map of tip amplitude (Figure 1e, inset) clearly shows the square depression below the gate electrode where the 2D/3D heterojunction forms. Additional optical and electron microscopy characterizations including cross-sectional composition analysis are provided in the SI (Figures S2 and S3).

Upon structural characterization and evaluation of the electronic structure, direct current (DC) electrical transport measurements were performed under varying drain (V_{DS}) and gate (V_{GS}) biases. The $I_{DS}-V_{DS}$ output characteristics of $p^{++}Si$-MoS_2 heterojunction diodes at different V_{GS} show strong modulation of current, as shown in Figure 2a,b. This strong modulation shows no dependence as a function of MoS_2 thickness in the limit that we have investigated, which is from 6 to 8 layers, as seen in Figure 2, down to monolayers (see SI Figure S4). In particular, the reverse saturation current (positive V_{DS}) is observed to be modulated from the pA range to above 10 μA. This results in the device transitioning from a highly rectifying state at $V_{GS} = -12$ V (black line) to an ohmic-like state at $V_{GS} = 12$ V (orange line), demonstrating the gate tunability of current through the $p^{++}Si$-MoS_2 heterojunction. As the reverse current can be strongly modulated, the device can be operated as a digital logic switch when biased in this voltage range. The $I_{DS}-V_{GS}$ transfer characteristics (Figure 2c) at different reverse drain biases show this on/off current modulation. It is also observed that gate modulation characteristics of the drain current in forward bias versus reverse bias are fundamentally different, which is explained below with band diagrams. In contrast, the transfer and output characteristics of a control MoS_2 field-effect transistor (see SI Figure S5) built from the same flake show ohmic-like $I-V$ behaviors, suggesting that the 2D/3D junction dominates current output. Metal contacts to the $p^{++}Si$ substrate are also ohmic, as confirmed by the linear $I-V$ relationship with small resistance (∼44 Ω) (see SI Figure S6). Our triode heterojunctions show on/off current ratios of 2×10^7 (at $V_{DS} = 4$ V) and a rectification ratio of up to 3×10^6 (at $V_{GS} = -12$ V). The comparison of on/off ratio versus V_{DS} (blue) and rectification ratio versus V_{GS} (red) can be seen in Figure 2d.

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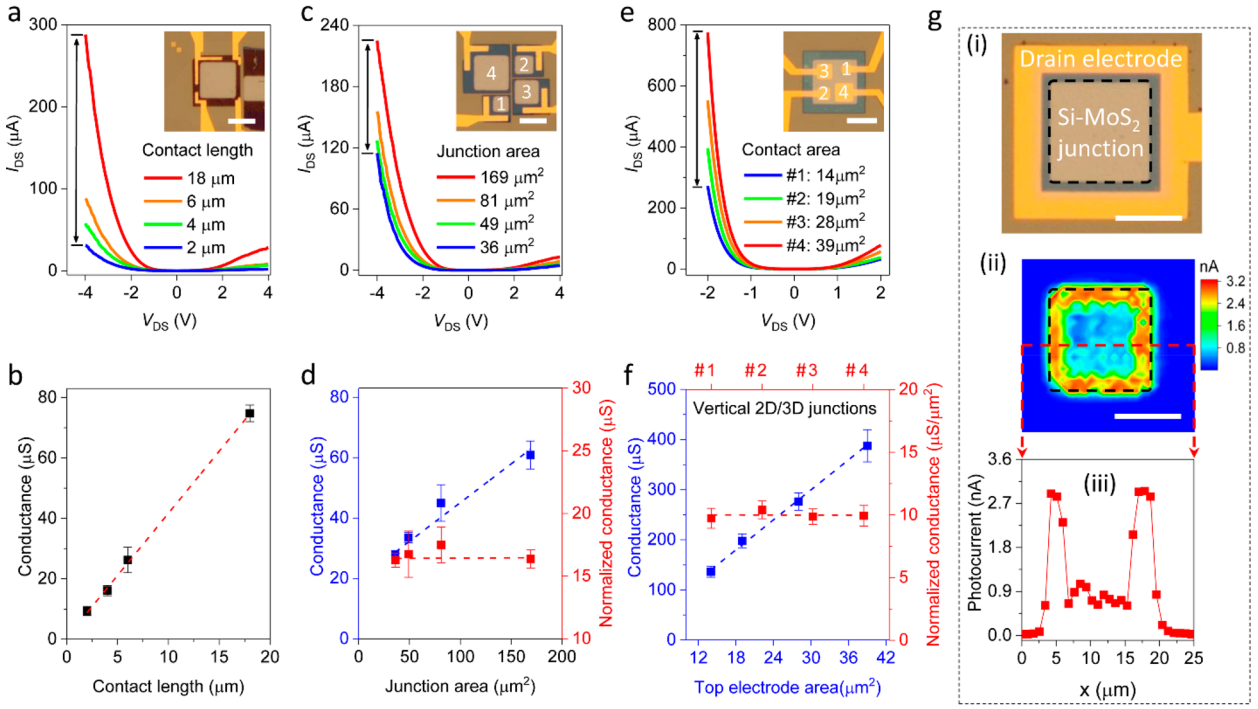

Figure 3. Lateral and areal scaling in the p^{++}Si-MoS_2 heterojunction diode. (a) Output characteristics of the device with different metal contact lengths (L = 2, 4, 6, and 18 μm). Inset: Optical micrograph of the device. The light gray square represents the overlapping p^{++}Si-MoS_2 junction. Scale bar, 5 μm. (b) Device conductance (at V_{DS} = −4 V) as a function of metal contact length extracted from panel (a). The error bars result from the averaging of seven measurements. (c) Output characteristics of the device with different junction areas (A = 36, 49, 81, and 169 μm^2). Inset: Optical micrograph of four p^{++}Si-MoS_2 heterojunction devices which are marked as 1, 2, 3, and 4. The light gray squares represent the overlapping p^{++}Si-MoS_2 heterojunction regions. Scale bar, 5 μm. (d) Conductance (blue) and perimeter-normalized conductance (red) as a function of junction area extracted from panel (c). The error bars represent standard deviations from seven such measurements. The perimeters of four 2D/3D junctions (inset, panel c) are 24, 28, 36, and 52 μm, and the contact electrode length of the four 2D/3D junctions (inset, panel c) is 14 μm. Perimeter-normalized conductance = (conductance (I_{DS}/V_{DS}) × contact electrode length)/(perimeter of 2D/3D junction). (e) Output characteristics of the device with various drain electrodes (A = 14, 19, 28, and 39 μm^2) fabricated onto the same 2D/3D heterostructure. Inset: Optical micrograph of the device with four drain electrodes which are marked as 1, 2, 3, and 4. The light gray square represents the overlapping p^{++}Si-MoS_2 heterojunction region. Scale bar, 5 μm. (f) Conductance (blue, at V_{DS} = −2 V) and area-normalized conductance (red) extracted from panel (e). The error bars represent standard deviations from four such measurements. (g) Optical micrograph (i), photocurrent map (ii), and photocurrent versus laser position (iii) of a representative 2D/3D junction device for 633 nm laser excitation. Scale bar, 10 μm.

The rectification ratio varies by 6 orders of magnitude with V_{GS}, whereas the on/off ratio varies by 7 orders of magnitude with V_{DS}. We further note that this superior performance arises from the highly asymmetric nature of the junction that is obtained by the use of p^{++}Si. This allows the depletion region to be completely concentrated in the MoS_2, which is effectively modulated by the gate. In addition, the lack of Fermi level pinning due to the passivated vdW nature of the MoS_2 further contributes to effective gate tunability. Our triode device can serve more functions than simply serving as a rectifying diode (for negative V_{GS} values) or transistor (for reverse V_{DS} values). In particular, under forward bias, there is minimal current modulation as a function of gate voltage (Figure 2c, V_{DS} = −2 to −4 V, and Figure S7). This suggests that the triode can be used as a tunable current source whose magnitude is dictated purely on the V_{DS} value, which is of particular importance in analog circuits and light-emitting diode drivers for noise-induced fluctuations.[41]

To develop a mechanistic understanding of the device operation, we investigate the junction band diagrams under various biasing conditions by finite-element simulations, as shown in Figure 2e,f. For V_{GS} > 0 V, the Fermi level in MoS_2 is pulled up, whereas the Fermi level in p^{++}Si is pinned below the valence band (Figure 1e(i)). As a result, a p−n junction is formed and the built-in potential barrier for electrons and holes is lowered with V_{DS} < 0 V, leading to a large current dominated by diffusion. For V_{DS} > 0 V, the conduction band of MoS_2 is pushed further below the valence band of p^{++}Si, narrowing the depletion region further to ∼10 nm. In this state, the electrons from the valence band of p^{++}Si can directly tunnel into the conduction band of MoS_2 due to the availability of density of states (DOS) in the MoS_2 conduction band, resulting in high current flow (Figure 2e(ii)). When the MoS_2 is depleted to near intrinsic levels (V_{GS} < 0 V), the Fermi level moves to the middle of the band gap, forming an i−p^{++} junction, which when forward biased (V_{DS} < 0) narrows down the depletion region and produces a large diffusion-dominated current (Figure 2f(i)). The converse is true under reverse bias (V_{DS} > 0 V), which produces a wide depletion region almost exclusively in the MoS_2, which not only increases the width for direct tunneling but also reduces availability of electron states in MoS_2, leading to a low off-state current (Figure 2f(ii)).

Whereas the above results of I−V characteristics suggest superior rectification and modulation, the fundamental nature of charge injection at a 2D/3D interface remains to be determined. To ascertain the current flow in the p^{++}Si-MoS_2 heterojunction diode, we first characterize the current as a function of the metal contact length and 2D/3D junction area.

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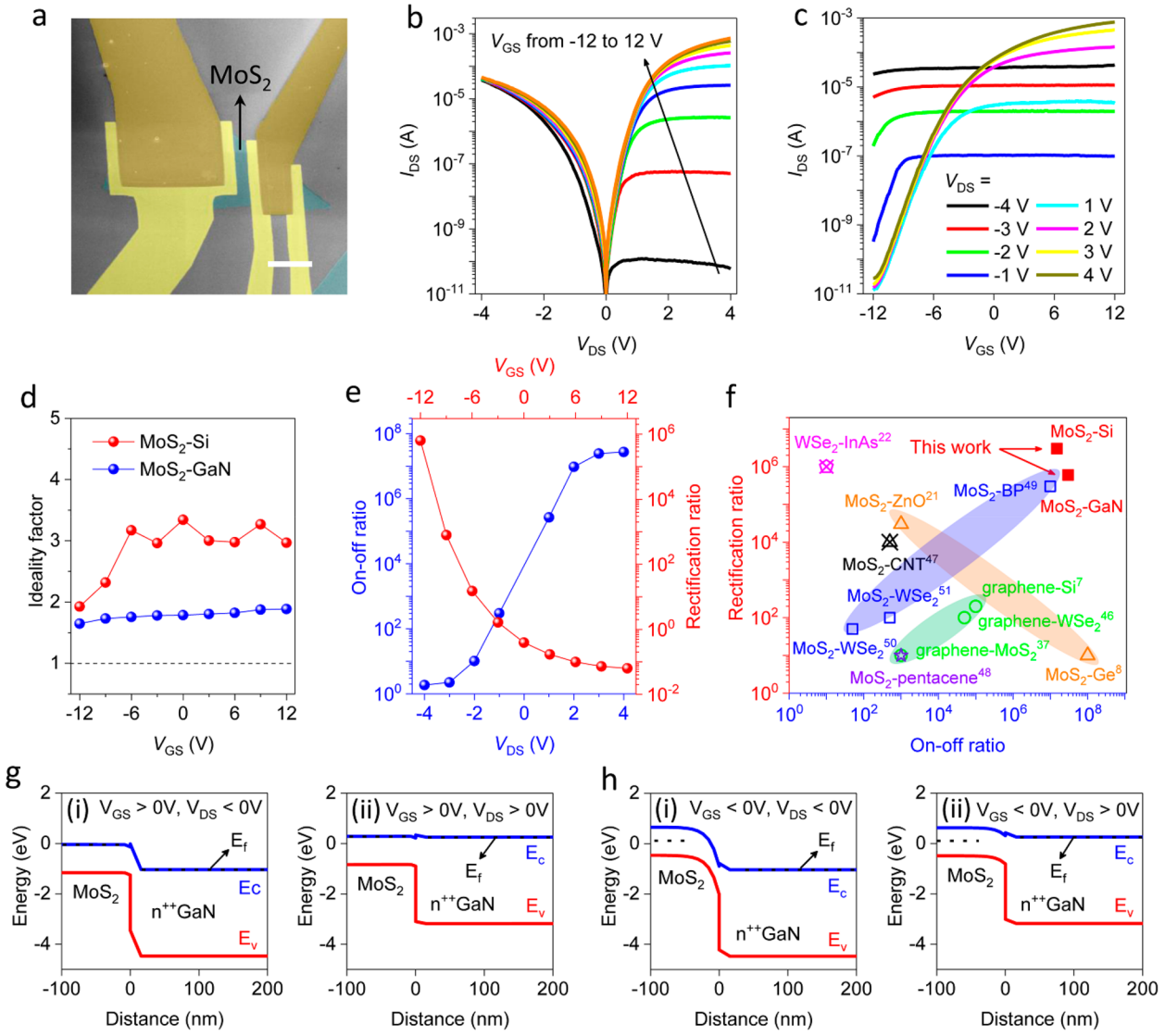

Figure 4. Room-temperature electrical characterization of the n^{++}GaN-MoS_2 heterojunction diode. (a) False-colored scanning electron microscopy image of a representative n^{++}GaN-MoS_2 heterojunction diode. MoS_2 flake and electrodes are indicated by light blue and yellow colors, respectively. Scale bar, 10 μm. (b) Output characteristics of the device at various gate voltages, showing a clear transition from a highly rectifying state at V_{GS} = −12 V to an almost symmetric I_{DS}−V_{DS} behavior at V_{GS} = 12 V. V_{GS} varies in the range of −12 to 12 V, with a step size of 3 V. (c) Transfer characteristics of the device at various drain biases showing a clear n-type transistor behavior. The device exhibits an ultrahigh gate modulation under positive drain bias (V_{DS} > 0 V). In particular, under forward bias (V_{DS} = −2 to −4 V), there is little or no current modulation as a function of gate voltage. (d) Ideality factors of n^{++}GaN-MoS_2 (blue) and p^{++}Si-MoS_2 (red) diodes as a function of gate voltage. (e) Device on/off ratio versus V_{DS} (blue) and rectification ratio versus V_{GS} (red). (f) Comparison of on/off ratio and rectification ratio with values reported in the literature. (g) Simulated band diagrams of the n^{++}GaN-MoS_2 heterojunction for V_{GS} > 0 V, V_{DS} < 0 V (i) and V_{GS} > 0 V, V_{DS} > 0 V (ii), where the applied drain bias is on MoS_2 and the contact to GaN is grounded. (H) Simulated band diagrams of the n^{++}GaN-MoS_2 heterojunction for V_{GS} < 0 V, V_{DS} < 0 V (i) and V_{GS} < 0 V, V_{DS} > 0 V (ii), where the applied drain bias is on MoS_2 and the contact to GaN is grounded. GaN band gap (E_g) = 3.4 eV, GaN electron affinity (χ) = 4.1 eV.

The fabrication process is detailed in SI Figures S8 and S9. I_{DS}−V_{DS} output characteristics with varying contact lengths (Figure 3a) show that the current decreases by approximately ∼700% as the contact length changes from 18 to 2 μm. On the other hand, the output characteristics versus the 2D/3D junction area (Figure 3c) show that current decreases slowly by only ∼200% as the junction area changes from 169 to 36 μm^2. Device conductance versus contact length at V_{DS} = −4 V extracted from Figure 3a is shown in Figure 3b, which further demonstrates that the conductance linearly depends on contact length with a slope of ∼4 μS/μm. However, the perimeter-normalized conductance is independent of the junction area (slope of ∼0.1 μS/μm^2), and it shows no change for varying junction areas, as shown in Figure 3d. Based on these electrical characteristics, we conclude that although the 2D/3D interface is planar in nature, the current injection is primarily one-dimensional (1D) because of lateral drain contact geometry. To confirm the 2D/3D nature of the vdW junction, we fabricated and measured two-terminal vertical transport devices with varying areas of top drain electrodes (Figure 3e (inset)). In these devices, the conductance changes by 184.4% as the drain electrode area changes by 178.6%, suggesting that the device conductance linearly depends on vertical 2D/3D junction area, as shown in Figure 3e,f. Further, the area-

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normalized conductance stays constant at ~10 $\mu S/\mu m^2$ (Figure 3f), confirming the uniformity and electronic homogeneity of the 2D/3D contact. We have further verified our claims of electronic homogeneity and uniformity of the 2D MoS_2 /3D $p^{++}Si$ contact by measuring multiple vertical junction devices of constant contact area (SI Figure S10) and performing spatial mapping of conductance using conductive AFM measurements (SI Figure S11), both of which agree with the above-discussed results and solidify our claim.

To get more direct evidence and further reinforce our observations from electrical measurements, we perform photocurrent measurements to deduce the electronically active area of the junction. Photocurrent microscopy shows a large photocurrent near the edge of the 2D/3D junction (Figure 3g(ii)) because MoS_2 collects photogenerated electrons and Si collects photogenerated holes, leading to the photocurrent (see SI Figure S12). A photocurrent signal suggests that the illuminated junction spot is electronically active as excited electrons and holes can separate, drift out, and get collected at the electrodes under zero bias. By reciprocity, the same regions would participate in diffusive current transport under forward and reverse bias conditions in the absence of illumination. This observed photocurrent signal diminishes further away from the 1D edge created by the etched oxide at which the 2D/3D junction initiates. The photocurrent is measurable along the edges up until the points where the metal electrodes extend along the length of the square. The photocurrent is, however, more than 3 times lower than that at the center of the square (Figure 3g(ii,iii)), suggesting negligible carrier separation and collection from the center. This observation provides a direct illustration that the carrier separation/collection and hence injection in a 2D/3D junction primarily occurs at a 1D interface, as confirmed by the 1D square shape in Figure 3g(ii). It is also worth noting that no measurable photocurrent is observed from the non-overlapping region of MoS_2 or the metal contact, suggesting that there is minimal contribution from drift or metal/MoS_2 contact-induced charge separation, further indicating that the current flow in the $p^{++}Si$-MoS_2 junction is dominated by the junction (Figure 3g(iii)). Therefore, we conclude that the device output current is dominated by the junction, and more importantly, the carrier injection occurs predominantly at the 1D edge of the 2D/3D junction. This observation concurs related observations in the electronic transport studied of metal contacts to 2D materials. The 3D metal contacts to 2D transition metal dichalcogenides and graphene are known to have a 1D edge length dependence.[42] However, often in the case of 3D metal contacts, there is covalent bonding involved.[43] In contrast, this is the first demonstration of this kind for a 2D/3D vdW semiconductor junction, wherein we observe that even in a vdW 2D/3D contact, the carrier injection is mainly 1D. This observation also has further implications in terms of areal scaling of the device. As long the device geometry entails charge injection and collection via metal side contacts, the 2D/3D junction area should not matter, and thus arbitrarily narrow 2D/3D junction devices can be packed in a given area to achieve large packing density or current density.

Finally, to establish comparative performance in a 2D/3D interface, we also use 3D GaN to build gate-tunable 2D/3D heterojunction diodes (Figure 4a and SI Figures S13 and S14). The motivation to use GaN is two-fold: (1) does isotype (n^{++}/n) versus anisotype (p^{++}/n) heterojunctions have an impact on a 2D/3D junction performance, and (2) does the interface atomic and electronic structure affect field modulation characteristics? Figure 4b shows the gate-dependent output current (I_{DS}) as a function of applied drain bias (V_{DS}) on MoS_2, whereas the contact to GaN is grounded. Similar to the silicon case, the GaN-based device exhibits a high rectification ratio of up to $\sim 6 \times 10^5$ at $V_{GS} = -12$ V, and it varies by over 6 orders of magnitude as a function of gate voltage. Figure 4c shows the drain current (I_{DS}) as a function of gate voltage (V_{GS}), with the drain bias changing from −4 to +4 V. It is observed that the device on/off ratio at positive drain biases (V_{DS} = 1 to 4 V) is higher than that at negative drain biases (V_{DS} = −1to −4 V). It is worth noting that the switching mechanism is somewhat different for the GaN/MoS_2 isotype (n^{++}/n) junctions in comparison to that of the Si/MoS_2 anisotype (p^{++}/n) junctions, as detailed below with simulated band diagrams. Further, we observe that the ideality factor of GaN-MoS_2 diodes ($1.5 < n < 2.0$) is smaller than that of Si-MoS_2 diodes ($2.0 < n < 3.5$) because, in contrast to GaN, the Si surface has a thin native oxide layer that degrades the interface quality of the 2D/3D junction (Figure 4d and SI Figures S3 and S15).[26,44,45] Despite the differences in quality of the interface, the gate tunability of rectification ratio maintains the same trend (Figure 4e, red plot), and the rectification ratio reaches a maximum when the MoS_2 is fully depleted, suggesting a maximum in built-in potential and formation an n^{++}/i junction. Likewise, a high asymmetry is observed in gate-dependent conductance (transfer characteristics), depending on whether the diode is forward biased ($-V_{DS}$) versus reverse biased ($+V_{DS}$). This is once again a distinguishing feature of this device in which the drain current remains constant as a function of V_{GS} under forward bias. Even under reverse bias, at high positive values of V_{GS}, the drain current reaches saturation (Figure 4c). We believe this is the case as one side of the junction is fully depleted. In summary, a high-performance three-terminal device with a record-high on/off ratio and diode with a high rectification ratio is simultaneously achieved in a single GaN/MoS_2 heterostructure, as summarized in Figure 4e. It is worth noting, however, that several attempts have been made at making gate-tunable vdW heterojunctions.[7,8,21,22,37,46−51] In most 2D/2D or 2D/3D cases, the doping levels in both semiconductors are simultaneously moving due to the semitransparency of the 2D layer to electric fields. Therefore, either these devices were limited by off-currents or on-currents (hence a trade-off in their ratio) or built-in potential (rectification ratio). If we fix the doping level in one semiconductor and make it 3D, a maximum in both can be concurrently achieved in the same device, which is the case here. This is shown as a comparison of the rectification ratio and on/off ratio with values reported in the literature (Figure 4f).

Simulated band diagrams under gate-induced accumulation (Figure 4g) and depletion (Figure 4h) of MoS_2 further elucidate the operation of this triode device. Unlike the case of $p^{++}Si$-MoS_2, simulated band alignments of n^{++}-GaN and n-MoS_2 show their Fermi levels and built-in potential barriers inversely aligned due to the comparable electron affinities of MoS_2 and GaN.[45] This also suggests that n-doped MoS_2 can serve as an efficient electron injection or collection contact for GaN devices. Under positive gate voltage ($V_{GS} > 0$ V), the MoS_2 is under accumulation and the Fermi level is raised close to its conduction band, and the Fermi level in n^{++}-GaN is equal to or above its conduction band. There is no potential barrier for electrons in the MoS_2 conduction band, which can diffuse

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unhindered into the GaN conduction band at $V_{DS} < 0$ V, resulting in a high current (Figure 4g(i)). Even for reverse bias ($V_{DS} > 0$), there is no barrier for electrons in this junction, which leads to a high drift current for electrons (Figure 4g(ii)). In fact, for sufficiently high V_{DS} (>2 V), the current in reverse bias (drift) exceeds the current in forward bias without causing a breakdown and conceptually inverting the diode rectification (Figure 4b,c). Under depletion of MoS_2 (i.e., $V_{GS} < 0$ V), the Fermi level in MoS_2 shifts to the middle of band gap while the Fermi level in n^{++}GaN is still pinned above the conduction band owing to the lack of electric field modulation in a heavily doped 3D semiconductor with a high DOS. For $V_{DS} < 0$ (forward bias), once again there is a large diffusion current due to lowering of the junction barrier, and there is a small reduction in magnitude due to depletion of the MoS_2 (Figure 4b, black plot). However, this diffusion current will have a greater contribution from holes in MoS_2 as the Fermi level is in the center of the gap (Figure 4h(i)) as opposed to an electron-dominated current in the previous case of MoS_2 under accumulation ($V_{GS} > 0$). Finally, the MoS_2 part is fully depleted at $V_{GS} < 0$ V and $V_{DS} > 0$ V (reverse-biased diode), which results in a very small drift current (Figure 4h(ii)).

CONCLUSIONS

In conclusion, we have demonstrated gate-tunable heterojunction diodes through vdW integration of 2D and 3D semiconductors. Owing to the ultrathin nature of 2D semiconductors and fixed doping of the 3D part, charge carriers across the 2D/3D junction can be effectively modulated by a capacitively coupled gate, enabling wide tunability of diode rectification ratio of up to 10^6 concurrently with an on/off current ratio $>10^7$, enabling utility for tunable rectification as well as digital switch. Also, we find that charge injection at a 2D/3D junction occurs along with a 1D contact interface with implications on scalability. Finally, the wide tunability of the junction and small ideality factors ($1.5 < n < 3.0$), despite an unpassivated 3D semiconductor surface, suggests a path toward heterogeneous integration on top of the Si CMOS at low temperatures. In particular, with the availability of remote epitaxy and epitaxial lift-off techniques to lift and peel Si and III−V 3D semiconductors, the possibilities for integrating 2D layers with Si or III−V on arbitrary substrates toward multifunctional sensors or memory or optoelectronic layers in conjunction with a high-performance computing part poses to be a promising direction for the field in years to come.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.0c00741.

Experimental methods, additional experimental data, calculations, and analysis (PDF)

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Notes

The authors declare no competing financial interest.

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