Dual Inductor Hybrid Converter for Point-of-Load Voltage Regulator Modules

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***Abstract*—Achieving high-efficiency power conversion with high power density for a large conversion ratio is crucially needed yet challenging in point-of-load applications because of increasing demands of loads. This article presents a new hybrid converter to address this need. The converter uses two interleaved inductors for complete soft charging of flying capacitors to provide high output currents with no capacitor hard-charge loss. This dual inductor hybrid (DIH) converter features a smaller number of switches and more effective switch utilization than a recently reported hybrid Dickson converter, yielding substantially less switch losses represented by smaller volt–ampere products and smaller equivalent output resistance. Converter operation principle is analyzed in detail to confirm the feasibility and benefits, and design considerations are provided to identify a practical design process. Experimental results verify the converter's operation principles and advantages with a 300-kHz 20-W prototype achieving 95.02% peak efficiency and 225-W/in^3 power density. The converter's advantages and performance make the point-of-load converter architecture a good candidate for demanding applications, such as in data centers, telecommunications, and high-performance digital systems.**

***Index Terms*—GaN devices, hybrid converter, inductor current sharing, point-of-load, power density, soft charging, switched-capacitor converter.**

I. Introduction

With drastically increasing demands for cloud computing and big data processing, the electric energy consumption of data centers in the U.S. is expected to reach 73 billion kWh by 2020 [1], accounting for about 2% of U.S electricity consumption. A large portion of this consumption is caused by losses in inefficient power delivery architectures that require a lot of attention and improvement [2]–[4]. As the required distribution currents keep increasing for more demanding digital loads, the conventional 12 V bus architecture exposes increased losses, complexity, and cost for interconnection and power delivery. To address these issues, the 48-V bus architecture has emerged as a new industry standard, employed by Google, HP, and other prominent data center designers and users [5]. However, the large conversion ratio from a four times higher input voltage, i.e., nominally 48 V, to core voltages, i.e., approximately 1–1.8 V, poses significant challenges in the design of point-of-load voltage regulator modules (VRMs) [6]–[9], pressing for high efficiency and high power density for installations in the vicinity of CPUs.

To deal with the challenges in the 48-V VRM, new ideas and improvements have been proposed and implemented. The Center for Power Electronics Systems (CPES) proposed a two-stage 48-V VRM architecture using a 48 to 12 V *LLC* converter, which uses a matrix transformer to achieve 850 W/in^3 power density, cascaded by 12 to 1.8 V multiphase buck converters [4]; however, the two-stage structure appears to be the main cause for its efficiency limit of 91%. The switched tank converter (STC) reported in [10] is another potential solution for a 48-V VRM with two-stage approach. The STC replaces some of the flying capacitors of the Dickson switched-capacitor converter with resonant tanks to achieve soft charging of capacitors and zero-current switching of switches, which leads to high efficiency and high power density. Although the STC 48 to 12 V reportedly achieves 97.18% and 750 W/in^3 [11], the subsequent regulation stage needed for 12 to 1 V would limit the overall performance, or its unregulated output can be addressed by the partial power architecture at the cost of complexity [12].

To overcome the limited efficiency of the two-stage structure, hybrid converters bridge the large conversion ratio by efficient utilization of passive components [13], [14]. The seven-level flying capacitor multilevel (FCML) converter presented in [13] converts 48 to 2 V using $12 + 1$ switches, 5 flying capacitors, and 1 output inductor. In N-level multilevel converters, the inductor can be significantly reduced compared to a conventional buck converter counterpart, but it requires $2(N - 1)$ switches, half of which experience the output current in operations, leading to large conduction losses in low-voltage, high-current applications, such as in data centers. Another hybrid converter based on a Dickson switched-capacitor converter can be a potentially better candidate for the 48 V-VRM, thanks to reduced stresses on the switch voltage and switch current as well as efficient

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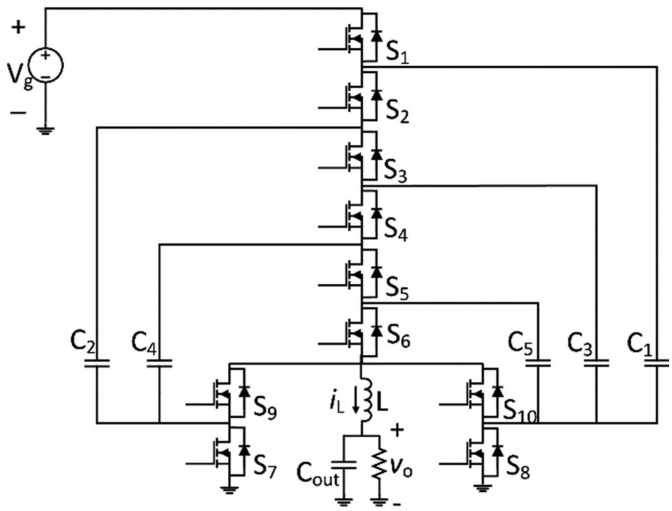


Fig. 1. 6-to-1 hybrid Dickson converter.

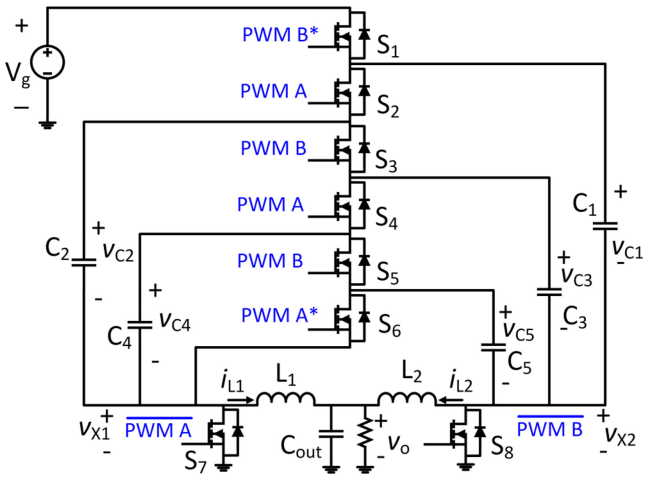


Fig. 2. DIH converter (case of 6-to-1 division in the drawing). It has interleaved dual inductors that are self-balanced and enable soft charging of flying capacitors.

charge delivery performance [14]. The hybrid Dickson converter shown in Fig. 1 (6-to-1 division) reported in [14] uses a single inductor at the output to achieve complete soft charging for the flying capacitors. A shortcoming of this converter is exposed in low-voltage, high-current applications that require large conversion ratios and thus small duty cycle. Although the upper switches, $S_{1\text{-}6}$, need to conduct only input current, the bottom switch pairs, $S_{7,9}$ and $S_{8,10}$, need undesirable series connections when carrying the output current in the inductor's freewheeling mode, leading to high conduction losses (more details in Section III).

In this article, a *dual inductor hybrid* (DIH) *converter*, originally reported in [15], also based on a Dickson switched-capacitor converter, is analyzed to effectively address the drawbacks of the conventional approaches. The DIH converter is also referred as DIHC in [15]. The DIH converter, shown in Fig. 2, employs two interleaved inductors at the output and eliminates two large synchronous switches, S_9 and S_{10}, that are required in the configuration of the hybrid Dickson converter shown in Fig. 1. These modifications enable the DIH converter to have nearly two times lower dc output resistance contribution from the conduction of switches and flying capacitors and thus approximately two times smaller conduction losses than the hybrid Dickson converter. In addition, the two interleaved inductors with naturally self-balanced currents provide the DIH converter with the same benefits of multiphase converters suitable for high-current applications [16] without additional current balancing complexity. Split-phase operation, having sub-modes during a phase, proposed in [14] is employed in the DIH converter to achieve complete soft charging for all the flying capacitors. The efficient hybrid operation of DIH converters, merging switched-capacitor and switched-inductor converters, provides an effective way to achieve high power density by increased capacitor utilization with soft charging to allow for a large flying capacitor voltage ripple and by favorable inductor design with reduced inductor voltage stress, without increasing switching frequency (more details in the following sections). To validate the claim of the new converter's key benefits, a 300-kHz prototype converter with 225-W/in^3 power density is demonstrated.

The rest of this article is structured as follows. Section II describes the proposed DIH converter's circuit operation. Section III provides its steady-state characteristics to identify its key features and advantages. Design considerations for the converter realization are presented in Section IV. Experimental results of the converter prototype are presented in Section V, and this article concludes in Section VI.

II. Circuit Operation of DIH Converter

This section provides an analysis of the converter operation to reveal its operation principle.

A. Operation Principle of DIH Converter

This section investigates a 6-to-1 DIH converter shown in Fig. 2, and the following analysis can be extended to its variations using different divisions, i.e., *N*-to-1 DIH converter, e.g., 10-to-1 using 12 switches and nine capacitors, for different operating conditions and optimization strategies. Because an odd-numbered division DIH converter, e.g., 7-to-1, obtains significantly different original features, including inherent capacitor soft charging by capacitor sizing and inductor current offset, the majority of the discussion in this article applies only to even-numbered division DIH converters (see [17] for further details). The 6-to-1 DIH converter employs five capacitors, $C_{1\text{-}5}$, with equal capacitance and two identical inductors, $L_{1,2}$. In steady state, the capacitor voltages, v_{C1}, v_{C2}, v_{C3}, v_{C4}, and v_{C5}, are assumed to have the same small voltage ripple, Δv_C; and the average voltages, V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5}, prove to be $\frac{5}{6}V_g$, $\frac{4}{6}V_g$, $\frac{3}{6}V_g$, $\frac{2}{6}V_g$, and $\frac{1}{6}V_g$, respectively. The identical average currents and capacitor voltages are proved in Section II-B. The converter can be modeled as shown in Fig. 3 where the flying capacitor network operates as an *N*-to-1 dc transformer (dcX) followed by an interleaved buck converter. Detailed circuit operations and analyses are presented in the following sections.

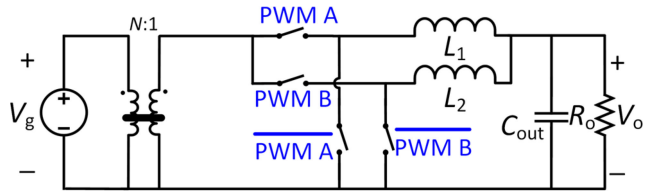


Fig. 3. Equivalent circuit of DIH converter in steady-state operation with ideal flying capacitor network operation assumed. The capacitor network serves as an N-to-1 dc transformer, and the rest of the converter operates as an interleaved buck converter.

The DIH converter operation can be explained using five equivalent circuits of five operation modes shown in Fig. 4 together with the operating waveforms of capacitor voltages v_{C1-5} and inductor currents i_{L1-2} in Fig. 5. To facilitate mode analysis and to provide the insights of the converter operation, the capacitor ripple voltages and inductor ripple currents are assumed to be small [18]. Having the two sub-modes, called split-phases, modes 1a and 3a, allows the converter to achieve complete soft charging in the same mechanism of the hybrid Dickson converter in [14]. Theoretically, assuming small inductor current ripple, modes 1b and 3b are equally timed and twice longer than modes 1a and 3a or $D_s = 1/3D$ in case of a 6-to-1 DIH converter. In practice, the ratio would be optimally engineered considering the inductor ripple to achieve complete capacitor soft charging (see more details in Sections IV-C). The ratio of mode 1 (1a + 1b) or mode 3 (3a + 3b) to the rest of a period determines the converter duty cycle D as illustrated in Fig. 5, and it is used to regulate the converter output, similar to conventional pulsewidth modulated (PWM) power converters. With these considerations, the converter operates as follows.

Mode 1a starts with S_2, S_4, and S_8 turned ON, forming two parallel branches of two series-connected capacitors, C_1-C_2 and C_3-C_4, sharing the current I_{L1}, while C_5 is open-circuited and conducts no current. Switching node v_{x1} receives $\frac{1}{6}V_g$ from the capacitors, charging L_1. S_8 conducts $i_{L1} + i_{L2}$ with L_2 discharging, as displayed in Fig. 4(a). Compared with mode 1a, mode 1b, illustrated in Fig. 4(b), has S_6 turned on to add an additional branch of single capacitor C_5 to the capacitor network sharing I_{L1}. With half equivalent capacitance compared with the C_5 branch, C_1-C_2 and C_3-C_4 branches conduct only $\frac{I_{L1}}{4}$, whereas C_5 conducts $\frac{I_{L1}}{2}$, leading to two times lower charging/discharging slopes for $C_{1\text{-}4}$, as illustrated in Figs. 4(b) and 5. Since all capacitor branches equate same voltages, switching node voltage remains at $\frac{1}{6}V_g$ and continues charging L_1 as

$$v_{x1} \approx V_{C1} - V_{C2} = V_{C3} - V_{C4} = V_{C5} = \frac{1}{6}V_g. \qquad (1)$$

In Mode 2, similar to synchronous buck converters, the freewheeling switches S_7 and S_8 conduct discharging inductor currents, i_{L1} and i_{L2}, respectively, whereas high-side switches $S_{1\text{-}6}$ stay turned off, opening the capacitors and leaving their voltages unchanged, as illustrated in Figs. 4(c) and 5.

Mode 3a begins with S_3, S_5, and S_7 turned on, initiating the same charging/discharging currents, $\frac{I_{L2}}{2}$, on two capacitor branches, C_2-C_3 and C_4-C_5, in the opposite direction compared

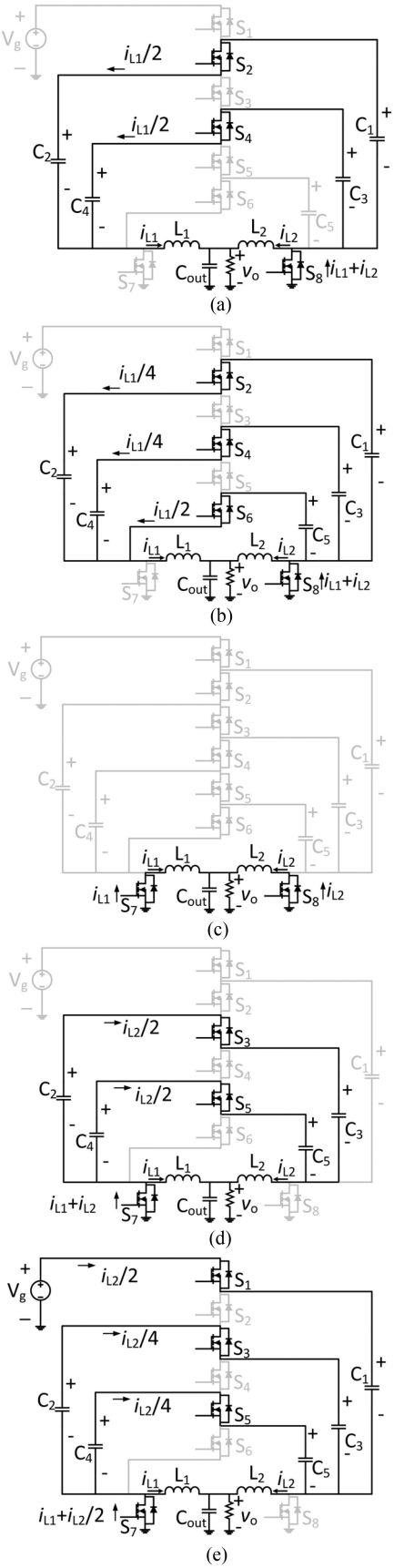


Fig. 4. Equivalent circuits of DIH converter in different modes: (a) Mode 1a. (b) Mode 1b. (c) Mode 2. (d) Mode 3a. (e) Mode 3b.

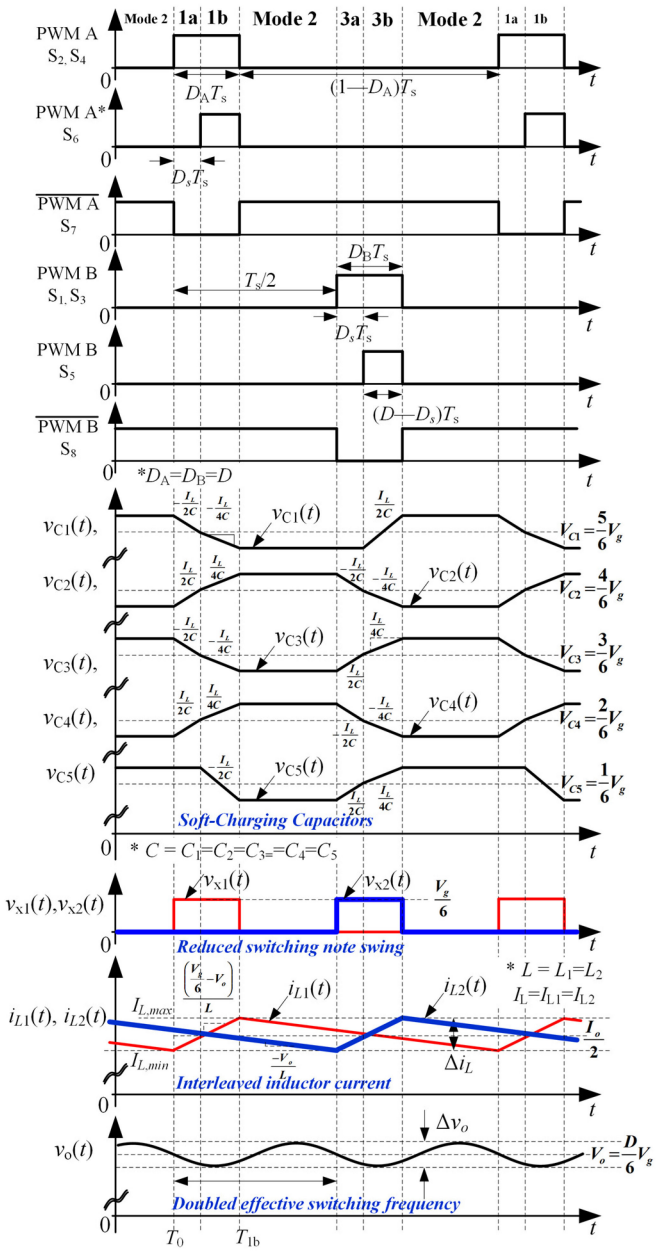


Fig. 5. Circuit operation of 6-to-1 DIH converter.

with modes 1a and 1b. S_7 conducts the sum of two inductor currents, similar to S_8 in mode 1a, as noted in Fig. 4(d). In mode 3b, C_1 connected to V_g by S_1 conducts $\frac{I_{L1}}{2}$, changing the currents through the other capacitors to $\frac{I_{L2}}{4}$ and, as a result, reducing the current on S_7 by half of I_{L2}, as stated in Fig. 4(e). It is the same with mode 1: switching node voltage v_{x2} is defined by the capacitor branch voltages, expressed as

$$v_{x2} \approx V_g - V_{C1} = V_{C2} - V_{C3} = V_{C4} - V_{C5} = \frac{1}{6}V_g. \quad (2)$$

Mode 2 again follows mode 3 and completes one switching period.

By recognizing the voltages applied to the inductor L_1, the inductor current i_{L1} can be expressed as

$$i_{L1}(t) = I_{L,\min} + \frac{\left(\frac{1}{6}V_g - V_o\right)}{L_1}(t - T_o) \quad (3)$$

in modes 1a and 1b and

$$i_{L1}(t) = I_{L,\max} - \frac{V_o}{L_1}(t - T_{1b}) \quad (4)$$

in the rest of the modes or when $T_{1b} \le t \le T_0 + T_s$. The equation for L_2 can be similarly derived, and the two inductors are operated in interleaved manner, just like the interleaved buck converter [19]. This original feature is desirable for high-current applications since the interleaved inductor operation implies favorable inductor sizing and thus a better loss factor compared to a single-inductor hybrid Dickson converter [20], which is discussed in more details in Section II-B. Due to the integrated interleaved operation, duty cycle D is limited to 50%.

With the discussed converter operations, all flying capacitors are soft charged/discharged with inductor currents and thus without hard charging loss, which is $0.5C(\Delta v_C)^2$ in conventional switched-capacitor converter modeled as slow-switching limit [21]. This is a key advantage of the proposed converter, especially for high-power and high-current applications. As the flying capacitors achieve complete soft charging, the DIH converter can reduce capacitor size while operating at a lower switching frequency, avoiding the fundamental tradeoff between capacitor size and switching frequency requirements in regular switched-capacitor converters [22]–[24].

In addition, the inductors can be favorably sized small by the hybrid operation without increasing switching frequency for high power density and large conversion ratios because of the reduced switching node voltage, i.e., $v_{x1,2}$ only switch between $\frac{1}{6}V_g$ and 0, similar to the three-level or multilevel topologies [25], [26].

B. DC Characteristic and Inherent Inductor Current Balance

According to the volt-second balance of the inductor, DIH converter's ideal voltage conversion ratio is defined as

$$\frac{V_o}{V_g} = \frac{D}{N} \quad (5)$$

where N is the number of division ($N = 6$ for the DIH converter in Fig. 2), compared to $\frac{V_o}{V_g} = \frac{2D}{N}$ in the hybrid Dickson converter [14]. With two times larger duty cycle, the DIH converter design can have more relaxed timings of high-side switches for the same conversion ratio, or support a two times larger conversion ratio with the same duty-cycle timing constraints. Since the switching-node voltage swing, $v_{x1,2}$, is reduced by N times compared to the buck converter counterpart, and the output capacitor receives interleaved inductor currents, its output filter inductors and capacitor can be significantly reduced for the same output ripple [19].

While balancing inductor currents is a real design challenge in conventional interleaved buck converters, the two inductor currents of the DIH converter are guaranteed to be balanced, i.e., $I_{L1} = I_{L2}$, by nature of the flying capacitors' operation.

The periodic charges delivered to L_1 and L_2 are guaranteed to be identical by charge balance of flying capacitors in steady state. Therefore, with the same charge time, DT_s, average values of the two inductor currents remain same even with different inductances and/or different resistive components. In detail, to satisfy the charge balance of capacitor C_1, the net charge for the capacitor over a cycle should be zero, that is

$$\int_{T_0}^{T_0+T_s} i_{C1}dt = 0. \tag{6}$$

With the analysis in Section II-A and small ripple approximation

$$\int_{T_0}^{T_0+T_s} i_{C1}dt = -\frac{I_{L1}}{2}\left(\frac{D_A}{3}T_s\right) - \frac{I_{L1}}{4}\left(\frac{2D_A}{3}T_s\right) + \frac{I_{L2}}{2}\left(\frac{2D_B}{3}T_s\right). \tag{7}$$

As a result, the two inductor current averages are guaranteed to be equal, i.e., $I_{L1} = I_{L2}$, as long as the capacitor charge balance is satisfied and $D_A = D_B$, where D_A (D_B) is the duty cycle of PWM A (PWM B) shown in Fig. 5. Note also that the sensitivity of inductor current mismatch, i.e., $I_{L1} \neq I_{L2}$, caused by variations in duty cycles, $D_A \neq D_B$, is unity. Therefore, balanced inductor currents are indeed achievable with high-resolution duty cycle controls in today's digital controllers.

Similar to the charge balance used to prove the identical inductor average currents, the volt-second balance of the two inductors can be used to find the average values of the capacitor voltages. To satisfy the volt-second balance of the two inductor currents in steady-state operation

$$\int_{T_0}^{T_0+T_s} v_{L1}dt = (V_{x1} - V_o)\,DT_s - V_o\,(1-D)\,T_s = 0 \tag{8}$$

for L_1, and

$$\int_{T_0}^{T_0+T_s} v_{L2}dt = (V_{x2} - V_o)\,DT_s - V_o\,(1-D)\,T_s = 0 \tag{9}$$

for L_2, which yields $V_{x1} = V_{x2}$. Combining this equality, (1), and (2) to solve the average capacitor voltages yields $V_{C1} = \frac{5}{6}V_g$, $V_{C2} = \frac{4}{6}V_g$, $V_{C3} = \frac{3}{6}V_g$, $V_{C4} = \frac{2}{6}V_g$, and $V_{C5} = \frac{1}{6}V_g$.

III. Steady-State Analysis of DIHC

As expressed in the ideal voltage conversion ratio (5), the DIH converter has an approximately two times longer charge time than a hybrid Dickson, implying better switch and capacitor utilization or reduced conduction loss with the same switch and capacitor. To quantitatively evaluate this statement, this article provides two analyses: analysis on the total switch volt–ampere (V–A) product and average model to compare the DIH converter with different topologies for the same input–output operating condition.

A. Total Switch Volt–Ampere Product Analysis

The total switch V–A products, i.e., the sum of the products of the switch voltage and current stress, can be used to evaluate the switch utilization of the power conversion circuits [21]. The V–A metric, together with its dual the G–V^2 product, where G is the switch conductance, allows comparing the fundamental performance of different converters given a total switch size constraint in practical semiconductor implementation.

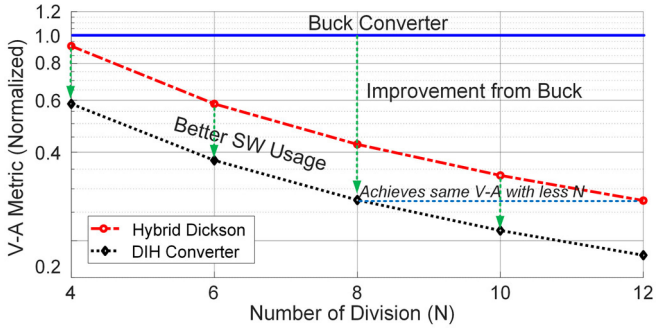


Fig. 6. V–A metric comparison. DIH converter improves the V–A metric compared to hybrid Dickson by having less current stress.

Noting peak voltage and current stress on each switch for N-to-1 DIH converter yields

$$VA_{DIH} = \frac{2V_gI_o}{N\left(\frac{N}{2}+1\right)} + \frac{(N-2)\,V_gI_o}{N\left(\frac{N}{2}-1\right)} + \frac{2V_gI_o}{N}. \tag{10}$$

In (10), the first term on the right-hand side represents the contribution of S_1 and S_N considering $\frac{V_g}{N}$ voltage stress and the peak current stress of $\frac{I_o}{(\frac{N}{2}+1)}$ during modes 3b and 1b; the second term for $(N-2)$ switches, from S_2 to $S_{(N-1)}$, having peak stresses of $2\frac{V_g}{N}$ and $\frac{I_o}{2(\frac{N}{2}-1)}$; and the third term for the two bottom switches, S_{N+1} and S_{N+2}, with peak stresses of $\frac{V_g}{N}$ and I_o. On the other hand, the V–A metric for the hybrid Dickson converter is derived as

$$VA_{HD} = \frac{4V_gI_o}{N\left(\frac{N}{2}+1\right)} + \frac{2\,(N-2)\,V_gI_o}{N\left(\frac{N}{2}-1\right)} + \frac{2V_gI_o}{N}. \tag{11}$$

Compared with the DIH converter, the hybrid Dickson converter has two times the peak current on the top switches, S_{1-N}, and half the current stress on each of the four bottom switches, $S_{(N+1)-(N+4)}$, while having the same voltage stresses. Fig. 6 illustrates the two V–A metrics. Compared with a buck converter counterpart, the metrics are normalized by $2V_gI_o$. As shown in Fig. 6, the improvement in the V–A metric by the hybrid converters from the buck converter increases as the division N increases, implying they would be more favorable in applications that require a large conversion ratio. In addition, with a lower V–A metric, the DIH converter can achieve a higher conversion with a simpler structure compared with a hybrid Dickson, e.g., an 8-to-1 DIH converter has the same V–A metric with a 12-to-1 hybrid Dickson but requires six switches less.

B. Average Model

As an additional measure for topology merit comparison, the average models of the DIH converter and hybrid Dickson converter are derived. The converter average model, shown in

TABLE I
AVERAGE MODEL PARAMETER COMPARISON OF THE DIH CONVERTER AND HYBRID DICKSON

	M	DC Output Resistance, R_{out}
DIH Converter	$\frac{D}{N}$	$R_{out} = D\left(\frac{1}{N}\right)^2\left(\sum_{i=1}^{N} R_{s,i}\right) + \left(\left(\frac{(N-1)^2}{N^2} - \frac{1}{2}\right)D + \frac{1}{4}\right)R_{s,N+1} + \left(\frac{1}{2}D + \frac{1}{4}\right)R_{s,N+2}$
Hybrid Dickson	$\frac{2D}{N}$	$R_{out} = D\left(\frac{2}{N}\right)^2\left(\sum_{i=1}^{N} R_{s,i}\right) + \left(\left(\frac{(N-2)^2}{N^2} - \frac{1}{2}\right)D + \frac{1}{4}\right)(R_{s,N+1} + R_{s,N+3}) + \left(\frac{1}{2}D + \frac{1}{4}\right)(R_{s,N+2} + R_{s,N+4})$

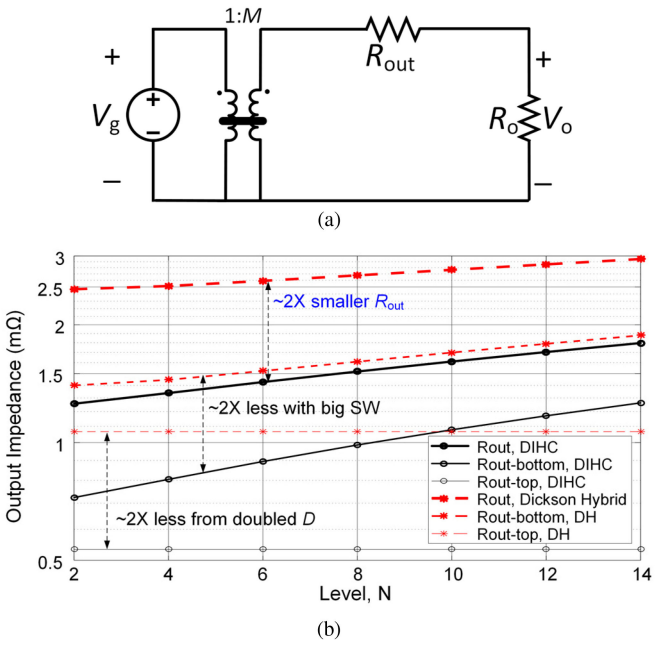


Fig. 7. Analysis of equivalent output resistance using average model. (a) Average model of a converter with an ideal 1:M dc transformer for conversion ratio modulation and a lumped output resistance R_{out} to represent loss factors. (b) Output resistance comparison of DIH converter to hybrid Dickson.

Fig. 7(a), can capture key dc characteristics, such as input-to-output voltage conversion ratio incorporating the effect of power processing losses. It can also be used to compare different topologies at different conditions [18], [21]. In this modeling approach, it is necessary to derive key loss factors and the equivalent output resistance R_{out} for the two converters.

Since the two converters have similar switching operations, i.e., two effective turn ON and turn OFF times in a period, and thus similar switching losses, this article focuses only on the conduction loss of switches that is the key factor to drive the difference in the converters' losses. Identifying the current conduction of individual switches, as illustrated in Fig. 4, and deriving loss equations as a function of output current leads to different coefficients of loss contributions. Table I presents average-model parameters of the conversion ratio and dc output resistance considering switch rms currents for the two N-to-1 division converters, where $R_{\text{s},i}$ is the on-resistance of S_i. In both converter average models, power switches are assumed to conduct constant current (fraction of inductor current) during DT_{s}, i.e., assuming small inductor current ripples.

Fig. 7(b) illustrates a representative set of output resistances calculated using practical GaN switches: EPC2014C (40 V, 16 mΩ) for top switches $S_{1\text{-}6}$ and EPC2023 (30 V, 1.45 mΩ) for bottom switches $S_{7\text{-}10}$ in two 6-to-1 converter implementations. The analysis shows that the DIH converter achieves approximately two times smaller R_{out} as a result of a combination of two times longer on-time for the top switches (1/2 rms^2 → 1/2 loss) and half the number of bottom switches. This advantage of two times lower switch conduction loss indicates the DIH converter is a more favorable option for applications that require high output currents while still supporting large conversion ratios.

IV. DESIGN CONSIDERATIONS

Since the DIH converter circuit has the unique features, it is necessary to acquire design insights through discussions on design considerations for practical converter implementation. In addition, in this section, effects of nonidealities, such as finite inductance (nonzero inductor current ripple), dead-time control, and body diode forward voltage drop will also be discussed.

A. Converter Circuit Configuration

Since the flying capacitor network operates as a dcX to reduce the voltage swing at the inductors' terminals, the converter has a higher duty cycle for the same conversion ratio and thus lower rms currents and less conduction loss. On the other hand, the presence of the flying capacitor network fundamentally limits the converter conversion ratio range. While the conversion ratio of a buck converter ranges from 0 to 1, the DIH converter has its range limited to $\frac{D_{\max}}{N}$, as expressed in (5). In other words, given an N division from the flying capacitors, the worst-case maximum output voltage is determined by

$$V_{o,\max} = D_{\max}\frac{V_{g,\min}}{N}, \text{and } N < D_{\max}\frac{V_{g,\min}}{V_{o,\max}} \tag{12}$$

where $V_{g,\min}$ is the minimum input voltage, and $v_{o,\max}$ is the maximum output voltage. This relationship in (12) indicates a limit on the value of N. For example, for a power conversion from an input of 40–54 V to an output of 1–2 V, the theoretical maximum number of divisions, N, is 10 (8, if the dead time and engineering margin are considered), considering the worst-case input and output voltages, $V_{g,\min}$ and $V_{o,\max}$, are 40 V input and 2 V output, respectively.

In addition to considering the maximum division number, the converter design should account for the device availability with certain voltage and current ratings available. Since the switch voltage ratings available in the market are discontinuous—e.g.,

15, 30, 40, or 60 V—this discontinuity should be considered for optimal switch selection to maximize converter performance.

Although the switched-capacitor network brings the multiple benefits in the DIH converter, this comes at a cost of increased complexity in switch drivers and control. As the converter controls more switches, managing the PWM signals would require more attentions, e.g., matching the propagation delays of multiple gate drivers.

B. Switching Interval and Dead-Time Control

The switching behavior of the DIH converter is similar to the conventional synchronous buck converter: upper switches, S_{1-N}, are hard switching (like the high-side switch of the buck), and the bottom switches are zero-voltage switching (ZVS) turn ON (like the low-side switch of the buck) with sufficient dead time. In the DIH converter, four dead time intervals exist: the first two are hard switching, and the latter two are ZVS—between modes 2 and 1a, modes 2 and 3a, modes 1b and 2, and modes 3b and 2. Transitions from the split-phase operation to the rest of a phase causes negligible switching loss (see Section IV-D).

Since the converter switching loss mechanism is similar to the synchronous buck converter, dead-time control can be designed by considering the switch turn ON and OFF characteristics and body diode commutation depending on the inductor current (load condition). To optimize the switching loss during the soft transitions (ZVS), the effect of different load conditions and body diode commutation should be taken into account [27].

Especially when the GaN switch is used, dead-time control should be carefully designed because of its higher forward voltage drop, i.e., about 2 V, though it does not have diode reverse recovery. Use of the Schottky diode in parallel with the bottom switches alleviates the adversary effect of a fixed dead time and parameter variations.

C. Split-Phase Operation in Practical Designs

The small-ripple inductor current assumption (zero ripple) used in Section II and Section III facilitates the analyses that provide insights into the converter operation and hold their validity in reasonable operating conditions, i.e., when the inductors' dc currents are significantly larger than their ripples. However, with the demand for higher power density under which inductors' sizes and values are forced smaller or at relatively lighter loads when inductor current ripples become significant compared with dc currents, the assumption and split-phase timing calculation described in Section II incurs errors, leading to partial hard charging and thus reduced converter efficiency. Therefore, it is necessary to develop a more rigorous method to calculate split-phase timings that consider inductor current ripples to achieve complete capacitor soft charging. To this point, a general expression for the split-phase operation is derived for both ideal and nonideal conditions, i.e., finite inductance and switching frequency.

To derive a general expression for the split-phase for the ideal condition, the charge balance of flying capacitor C_1 for N-to-1 DIH converter is used

$$\int_{T_0}^{T_0+T_s} i_{C1}dt = \frac{2I_L\,(D-D_s)\,T_s}{\left(\frac{N}{2}+1\right)} - \frac{I_L(D-D_s)T_s}{\left(\frac{N}{2}+1\right)} - \frac{I_L D_s T_s}{\left(\frac{N}{2}-1\right)} = 0. \quad (13)$$

Rearranging (13) for the split-phase duty cycle, D_s, yields

$$D_s = \left(\frac{N-2}{2N}\right) D = k_{\text{ideal}} D. \quad (14)$$

Fig. 8 provides a graphical presentation of the ideal-case split-phase factor k_{ideal}. As the division number increases, the portion of the split-phase to the total on-time approaches to 0.5 due to the reduced current difference between the split-phase and normal mode.

In a practical design where the inductor current ripple is significant, note that the split-phase starts at the valley of the inductor current waveforms, indicating that the value of actual D_sT_s needs to be larger, i.e., $k_{\text{actual}} > k_{\text{ideal}}$, as illustrated in Fig. 9. The actual split-phase factor k_{actual} required for complete soft charging can be derived by noting the time interval to obtain an extra charge matched with the deficient charge in Fig. 9, that is

$$\frac{(N-2)}{2N} I_L D T_s = \int_{T_0}^{T_0+t_s} \left(I_{L,\min} + \frac{V_x - V_o}{L}\tau\right) d\tau. \quad (15)$$

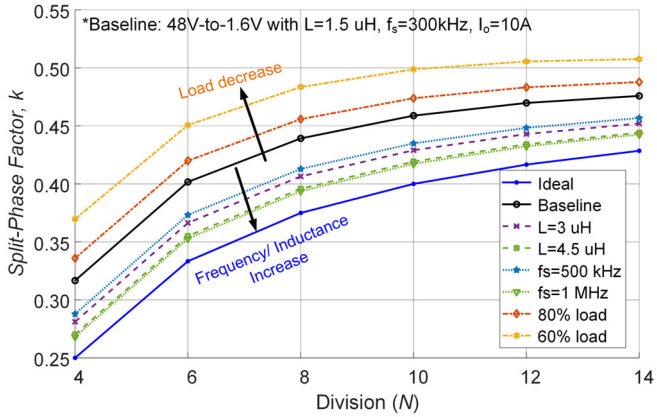


Fig. 8. Split-phase factor comparison to analyze effects of inductance, switching frequency, and load conditions on the actual split-phase factor.

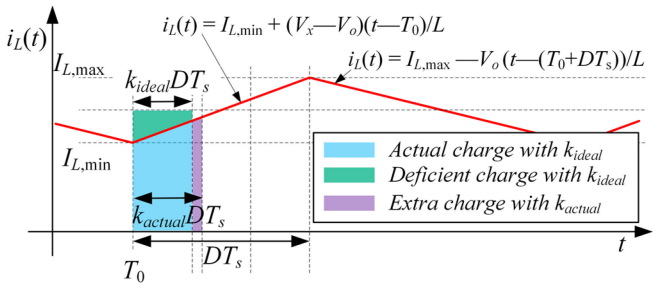


Fig. 9. Graphical explanation of the need for split-phase interval increase.

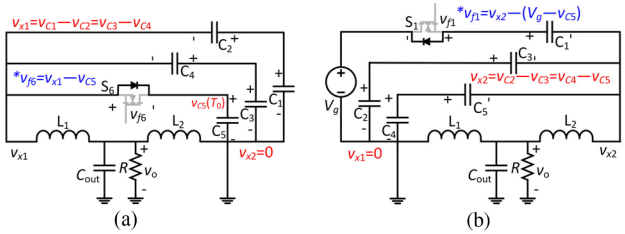


Fig. 10. Equivalent circuits during. (a) Mode 1a. (b) Mode 3a.

Solving (15), a second-order polynomial, yields

$$t_s = \frac{-I_{L,\min} + \sqrt{I_{L,\min}^2 - \frac{(V_x - V_o)(N-2)}{L \cdot N} I_L D T_s}}{(V_x - V_0)/L} = k_{\text{actual}} D T_s. \tag{16}$$

Therefore, $k_{\text{actual}} = \frac{t_s}{DT_s}$. Impacts of inductance, switching frequency f_s, and load condition on the actual split-phase timing can be evaluated by a graphical approach. The condition of the baseline case is 48 to 1.6 V, $L = 1.5\ \mu$H, $f_s = 300$ kHz, and $I_o = 10$ A. Compared to the ideal condition, a longer split-phase interval is required for soft charging. Inductance increase reduces the additional time needed resulting from the decrease of deficient charge. The switching frequency change has the same effect with that of the inductance since it scales the inductor current ripple in the same way; i.e., two times the frequency has the same effect of two times the inductance.

On the other hand, the load condition heavily affects the split-phase factor since it exponentially changes the proportion of the inductor current ripple (deficient charge) to the average dc current (total charge). In addition, this implies that a fixed split-phase factor can cause partial capacitor hard charging off the design point and that it can be challenging to achieve complete soft charging across all operating conditions. On the other hand, the loss from partial hard charging may not be significant since it is proportional to ${I_L}^2$, showing a drastic decrease at light loads. Alternatively, an adaptive split-phase control for this loss minimization can be programmed on the controller based on this analysis.

D. Capacitor Sizing Considering Switch Limitation

Provided that the split-phase operation is accurate to obtain complete soft charging, i.e., switched-capacitor loss is eliminated, the DIH converter can theoretically allow large voltage ripple on the flying capacitors and thus allow smaller capacitors for higher power density. In practice, however, the maximum capacitor voltage ripples should be limited considering switch voltage stresses. Fig. 10 illustrates the equivalent circuit during the split-phase to demonstrate the switch voltage stresses. This representation identifies that the split-phase operation is available because of the switch body diode blocking the voltage difference between the branches. Specifically, the following conditions:

$$(v_{C1}(T_0) - v_{C2}(T_0)) - v_{C5}(T_0) = v_{f6}(T_0) < v_{f,th} \tag{17}$$

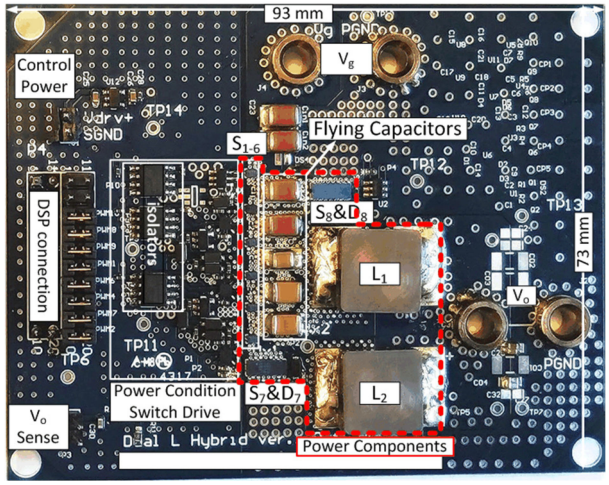


Fig. 11. 6-to-1 DIH converter prototype for 40–54 V to 1–2 V/10 A.

for the beginning of mode 1a and

$$(v_{C2}(T_2) - v_{C3}(T_2)) - (V_g - v_{C1}(T_2)) = v_{f1}(T_2) < v_{f,th} \tag{18}$$

for the beginning of mode 3a should be satisfied to obtain complete soft charging. $v_{f,th}$ is the threshold voltage to turn on the switch body diode. Deriving the voltage compensation during the split-phase operation yields

$$v_{f6}(T_0) = v_{f1}(T_2) = \frac{2 I_L D_s T_s}{\left(\frac{N}{2} - 1\right) C} \tag{19}$$

and, as a result, the minimum capacitance to achieve complete soft charging without turning on the switch parasitic body diodes is found as

$$C_{\min} = \frac{2 I_L D_s T_s}{\left(\frac{N}{2} - 1\right) v_{f,th}}. \tag{20}$$

The Efficient Power Conversion Corporation (EPC) GaN devices used in this article have a 1.5–2.0 V source-to-drain forward threshold voltage that should be taken account in the converter design process.

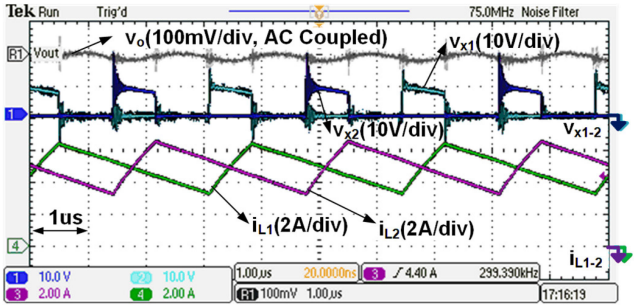
Another design consideration on the capacitor sizing is the switching loss. Since the capacitor voltage swing reflects on the switching nodes and thus its associated switches, the excessive voltage swing aggravates the switching loss, a function of V_x^2 during mode transitions, especially the switching loss of the bottom switches.

V. Experimental Verifications

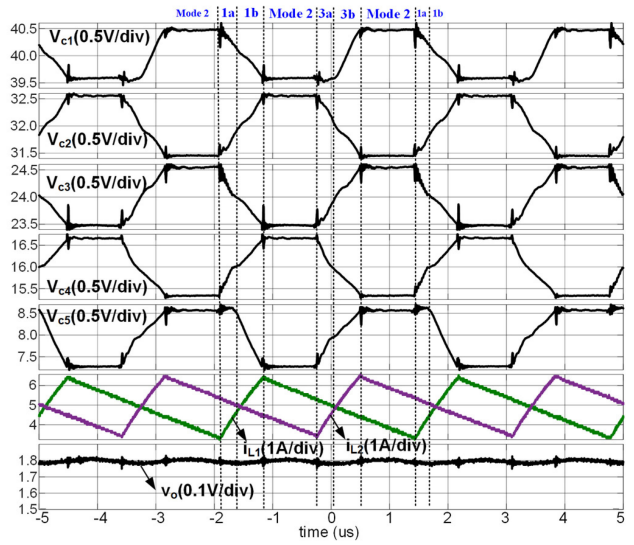
To verify the feasibility of the new converter topology, a 20 W 48-V VRM prototype is implemented. The printed circuit board implementation is shown in Fig. 11. The 6-to-1 DIH converter prototype is designed based on the discussions in Section III and Section IV. The design of the converter can differ with different objectives, taking into consideration the representative trade-off between complexity/cost and benefits from reduced voltage stress and favorable inductor design. Low-voltage EPC GaN devices are used for switches. Switch on-resistances can

TABLE II
CIRCUIT COMPONENTS AND PARAMETERS

Item	Design Selection
Controller	TMS320F28377, Texas Instruments
Switching freq.	300 kHz
C_1, C_2, C_3, C_4, C_5	2.2, 1.5, 1.5, 1, 1 µF, X7R, 1812/1210, TDK
C_{out}	6.8 µF, X5R, 0603, 10V, TDK
Inductors, L_1 & L_2	1.5 µH, IHLP-5050CE-01
$S_{1\text{-}6}$	EPC2014C, 40 V, 16 mΩ, EPC
$S_{7\text{-}8}$	EPC2023, 30 V, 1.45 mΩ, EPC
D_7, D_8	CRS08, 30 V, 1.5 A, Schottky with $S_{7\text{-}8}$
Gate drivers	3 x LM5113, 2 x LM5114
Signal isolators	Si8422, Silicon Labs

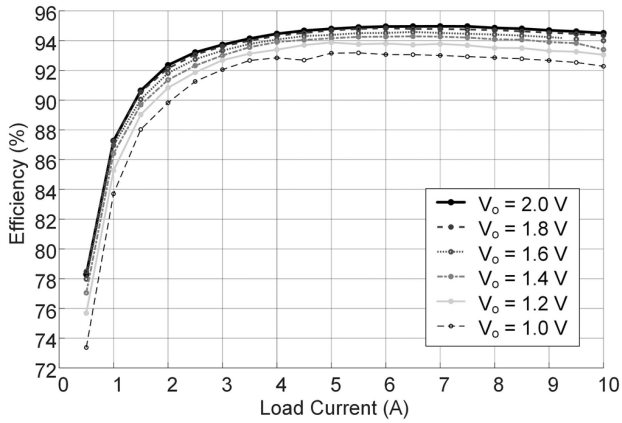


(a)

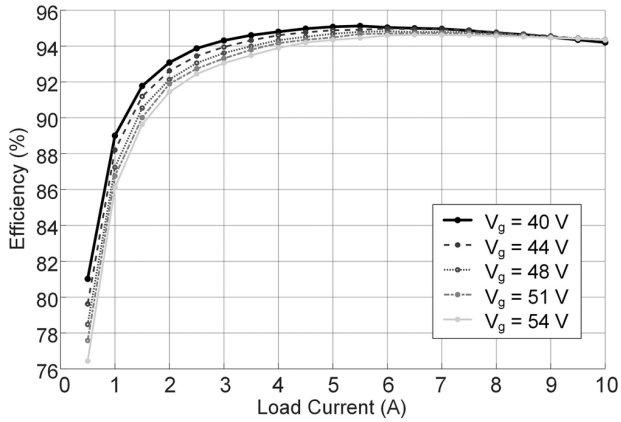


(b)

Fig. 12. Prototype operation waveforms at 48 to 1.8 V under 10 A. (a) Output regulation waveforms including inductor currents and switching nodes. (b) Flying capacitor voltage waveforms.



(a)



(b)

Fig. 13. Measured efficiency of prototype. (a) Efficiency at 48 V input with different output voltages. (b) Efficiency at 1.8 V output with different input voltages.

be determined based on the average model to identify desirable loss contributions and availability. Since the tradeoff between the on-resistance (conduction loss) and drain-to-source capacitance (switching loss) is similar to that of the conventional converters, the design can be finalized with a traditional design methodology [28].

The flying capacitors are designed according to the discussions in Section IV, eventually using (20), to avoid hard charging with selected switch devices. Considering the converter input and output conditions, the minimum capacitance of 1 μF, identified by (20), is used for flying capacitors. Capacitor parts are strategically selected to achieve the same effective capacitance considering the capacitance degradation with higher bias voltages.

The split-phase operation is achieved by programming a constant split-phase interval, $k = 0.4$, to achieve complete soft charging at the full load condition from (16). Cascaded bootstrap-driven and gate-driven switch gate drive circuits are employed to drive multiple floating switches from a grounded voltage supply [29]. The component selections and specifications are given in Table II.

The key operation waveforms of the prototype at the 48–1.8 V/10 A condition are shown in Fig. 12. Comparable to the operation described in Section II and depicted in Figs. 4 and 5, the experimental waveforms of the prototype confirm the desirable operation and characteristics. In Fig. 12(a), the two interleaved inductor currents are naturally balanced by the inherent capacitor charge balance with no need for an additional current balancing method. Fig. 12(b) captures the flying capacitor voltages in steady-state operation. As expected from the analysis, all capacitors are soft charged by the inductor currents and split-phase operation. No significant voltage jump, indicating hard charging, is visible in the capacitor voltage waveforms.

Fig. 13 displays the measured efficiency of the prototype converter with different output voltages, 1–2 V, from a 48 V

TABLE III
COMPARISON OF THE DIH CONVERTER TO DIFFERENT SOLUTIONS FOR DATA CENTERS

	This work	Dartmouth [13]	VICOR	CPES [9]	CPES [4]	LMG5200POLEVM
Topology	DIHC	FCML	PRM+VTM	Sigma (DCX|Buck)	LLC+Buck	HB+Current Doubler
Input-Output	48V-1~2V/10A	48V-2V/10A	48V-1.5V/115A	48V-1V/80A	48V-1.8V/120A	48V-1V/50A
Peak efficiency	95.02% at 5.5A	85% at 5A	94% at 57.5A	93.5% at ~40A	91% at ~40A	90.7% at 20A
# Switches/type	8 (6-to-1) / GaN	13 (7-Level) / GaN	4+6 / MOSFET	12(DCX)+2(Buck) / GaN	8(DCX)+2x2(Buck) / GaN	2(Pri)+4(Sec) / GaN
Capacitors	5(flying)+1(out)	5(flying)+1	1(Cr)+2(HB)+1(out)	1(Cr)+2(output)	1+1(LLC)+2(Output)	2(HB)+1(output)
Inductors/TR	2	1	1(BB)+1(Lr)+1(TR)	1(DCX)+1(Buck)	1(LLC)+N(Buck)	1(TR)+2(Sec)
Passive vol. (mm^3)	1345	2422	-	-	-	1343
Frequency (f_{sw})	300 kHz	83.3 kHz	1 MHz/1.4 MHz	1 MHz/600 kHz	1.6 MHz/1 MHz	600 kHz
Power density	225 W/in^3	-	-	420 W/in^3	-	-

input and different input voltages, 40–54 V, for 1.8 V output, respectively. Owing to the superior output resistance by reasonable on-time and excellent switch utilization, soft charging for all capacitors, and interleaving benefits, the converter achieves 95.02% peak efficiency, and 225 W/in^3 power density considering the power conversion components. It is also beneficial that the converter efficiency is kept higher than 90% down to 20% load in data center applications where light load efficiency is also important for energy savings.

Table III compares the state-of-the art technologies for the 48 V core application highlighting the DIH converter in superior efficiency, and relatively simple structure (number of active components). Simple operations and increased duty cycle promise high potential to further increase the converter power density with optimized and/or integrated design, e.g., integrated circuit implementation to incorporate switch, control, and drive circuits into a chip.

VI. CONCLUSION

This article presented a new hybrid converter using a switched-capacitor network and two interleaved inductors for high efficiency and high power density. By streamlining the power conversion structure and, as a result, eliminating two freewheeling switches, the converter achieves an approximate two times improved output resistance in conduction losses compared with the recently proposed hybrid Dickson converter counterpart. Interleaved dual output inductors bring the benefits of the multiphase interleaving architecture for high-current applications with inductor currents naturally balanced by the flying capacitors' charge balance. Based on the detailed analyses of the converter operation and design considerations for converter realization, a 20 W proof-of-concept prototype verified the converter's desirable operations and characteristics, achieving 95.02% peak efficiency and 225 W/in^3 power density.

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REFERENCES

[1] S. Arman *et al.*, United States data center energy usage report. Lawrence Berkeley Nat. Lab., Berkeley, CA, USA, 2016.

[2] D. Salomonsson, L. Soder, and A. Sannino, "An adaptive control system for a DC microgrid for data centers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1910–1917, Nov./Dec. 2008.

[3] A. Pratt, P. Kumar, and T. V. Aldridge, "Evaluation of 400 V DC distribution in telco and data centers to improve energy efficiency," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2007, pp. 32–39.

[4] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "48-V voltage regulator module with PCB winding matrix transformer for future data centers," *IEEE Trans. Ind. Electron.*, vol. 64, no. 12, pp. 9302–9310, Dec. 2017.

[5] C. Wang and P. Jain, "A quantitative comparison and evaluation of 48V DC and 380V DC distribution systems for datacenters," in *Proc. IEEE 36th Int. Telecommun. Energy Conf.* , 2014, pp. 1–7.

[6] Z. Yanjun, X. Dehong, C. Min, H. Yu, and D. Zhoong, "LLC resonant converter for 48 V to 0.9 V VRM," in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, vol. 3, pp. 1848–1854.

[7] M. Ye, P. Xu, B. Yang, and F. C. Lee, "Investigation of topology candidates for 48 V VRM," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2002, vol. 2, pp. 699–705.

[8] S. Oliver, "From 48 V direct to Intel VR12. 0: Saving 'Big Data' $500,000 per data center, per year," Vicor White Paper (Online), Jul. 2012.

[9] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density 48/1V sigma converter voltage regulator module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2207–2212.

[10] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5048–5062, Jun. 2019.

[11] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, "A 98.55% efficiency switched-tank converter for data center application," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6205–6222, Nov./Dec. 2018.

[12] Y. He, S. Jiang, and C. Nan, "Switched tank converter based partial power architecture for voltage regulation applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 91–97.

[13] J. S. Rentmeister and J. T. Stauth, "A 48V:2V flying capacitor multilevel converter using current-limit control for flying capacitor balance," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 367–372.

[14] Y. Lei, R. May, and R. P.-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a Dickson switched-capacitor converter," *IEEE Trans. Power Electronics*, vol. 31, no. 1, pp. 770–782, Jan. 2016.

[15] G.-S. Seo, R. Das, and H.-P. Le, "A 95%-Efficient 48V-to-1V/10A VRM hybrid converter using interleaved dual inductors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 3825–3830.

[16] D. Baba, "Benefits of a multiphase buck converter," Texas Instrum. Incorporated, Dallas, TX, USA, 2012.

[17] R. Das, S. Gab-Su, and H.-P. Le, "A 120 V-to-1.8 V 91.5%-Efficient 36-W dual-inductor hybrid converter with natural soft-charging operations for direct extreme conversion ratios," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1266–1271.

[18] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA, USA: Kluwer, 2001, pp. 331–347.

[19] A. C. Schittler, D. Pappis, A. Campos, M. A. D. Costa, and J. M. Alonso, "Interleaved buck converter applied to high-power HID lamps supply: Design, modeling and control," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1844–1853, Jul./Aug. 2013.

[20] P.-L. Wong, P. Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 499–507, Jul. 2001.

[21] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[22] W. Qian *et al.*, "A switched-capacitor DC–DC converter with high voltage gain and reduced component rating and count," *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1397–1406, Jul./Aug. 2012.
[23] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc–dc converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.
[24] H. P. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32 nm fully integrated reconfigurable switched-capacitor dc–dc converter delivering 0.55 W/mm2 at 81% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2010, pp. 210–211.
[25] G. S. Seo and H.-P. Le, "An inductor-less hybrid step-down DC–DC converter architecture for future smart power cable," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 247–253.
[26] B. P. McGrath, C. A. Teixeira, and D. G. Holmes, "Optimized phase disposition (PD) modulation of a modular multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4624–4633, Sep./Oct. 2017.
[27] "Dead-time optimization for maximum efficiency" Efficient Power Convers., El Segundo, CA, USA, Jun. 2014, [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/papers/Dead-Time%20Optimization%20for%20Maximum%20Efficiency.pdf
[28] B. Choi and D. Maksimovic, "Loss modeling and optimization for monolithic implementation of the three-level buck converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 5574–5579.
[29] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2925–2931.

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