

Efficient Heterojunction Thin Film CdSe Solar Cells Deposited Using Thermal Evaporation

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Abstract — CdSe is potentially an important material for making tandem junction solar cells with Si and CIGS. Thermodynamic calculations reveal the potential Shockley-Queisser efficiency of such a tandem cell to be in the 45% range. CdSe has the optimum bandgap (1.72eV) for a tandem cell with Si. In this paper, we show that this material system is indeed capable of achieving good electronic properties and reasonable devices can be made in the material. We report on fabricating CdSe materials and heterojunction CdSe solar cells in both superstrate and substrate configurations on FTO/glass and metal substrates. CdSe layer was deposited using thermal evaporation and then was post-treated with CdCl₂ to enhance the grain size and passivate grain boundaries. The device was an ideal heterojunction structure consisting of glass/FTO/n⁺CdS/ n-CdSe/p organic layer/NiO/ITO. The n⁺ CdS layer acted to prevent hole recombination at the n⁺/n interface, and the p organic layer (such as PEDOT:PSS or P3HT) acted to prevent electron recombination at the p⁺/n interface. The NiO layer was deposited on top of the organic layer to prevent decomposition of the organic layer during ITO deposition. World-record open-circuit voltages exceeding 800 mV and currents of ~15 mA/cm² were obtained in devices. Detailed material measurements such as SEM revealed large grain sizes approaching 8 micrometer in some of the films after grain enhancement. Optical measurements and QE measurements show the bandgap to be 1.72 eV. XPS measurements showed the CdSe film to be n type. Space-charge limited current was used to measure electron mobilities which were in the range of 1-2 cm²/V-s. Capacitance spectroscopy showed the doping densities to be in the range of a few $\times 10^{15}$ /cm³. For substrate devices, the quantum efficiency obtained was in the 90% range.

I. INTRODUCTION

Photovoltaic energy conversion is now a major energy technology. Si technology dominates the PV production today, with the conversion efficiencies of commercial products reaching 20+%, and of laboratory cells reaching 26+%. Since balance of system costs dominate the overall cost of PV energy, a technology for increasing the efficiency of Si panels by 50% would lead to significant reduction in the cost of PV energy. In this paper, we investigate a thin film material system (CdSe), which in a tandem junction combination with Si, can achieve such a large increase in the efficiency of Si based panels. CdSe is a direct gap material with the right bandgap (~1.72 eV) to match with Si in a tandem cell configuration. In Fig. 1 we show the projected Shockley-Queisser efficiency of a CdSe/Si system, showing that efficiencies approaching 45% are possible[1]. This means that

actual production efficiencies of 35-38% should be possible for PV panels based on such a technology. In spite of the enormous potential of this material system, there is little work on PV devices in this material[2-5]. In this paper, we present the first ever systematic study of structure, electronic properties and device properties of this material, including using a novel heterojunction structure to optimize QE and chemical annealing techniques to improve the grain size and reduce grain boundary recombination.

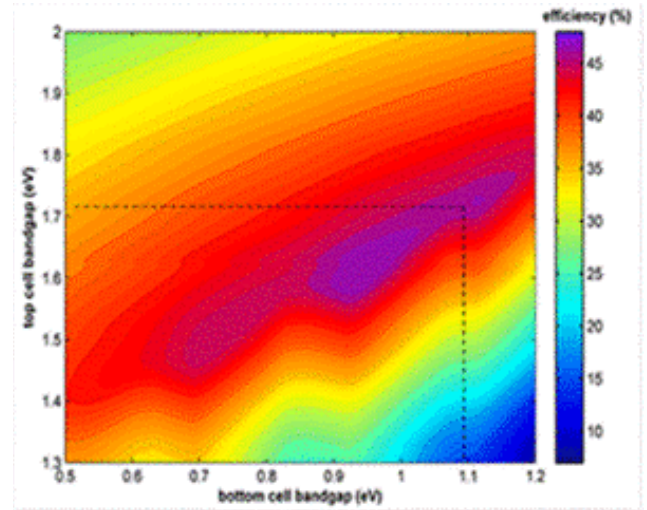


Fig. 1 Projected thermodynamic PV efficiencies in a tandem cell as a function of top cell bandgap(vertical axis) and bottom cell bandgap (horizontal axis). CdSe has the right bandgap (~1.72eV) for the top cell and Si has the right bandgap (1.12 eV) as the bottom cell for achieving ~45% SQ efficiency[1]

II. PROPERTIES OF CDSE

CdSe is a direct gap material. In Fig. 2 we show the absorption data on one of our CdSe films showing a bandgap of 1.72 eV. The film was deposited using thermal evaporation from CdSe chunks using a Luxel furnace. Typical substrate temperatures during growth were in the range of 400- 500°C. We discovered that the grain size can be significantly increased by using a post-deposition CdCl₂ heat treatment at 450 °C. See Fig. 3 for SEM data on grain enhancement. XPS measurements showed that the film was n-type with the valence band being 1.2 eV below the Fermi level. Electron

mobility was measured using space charge limited current techniques and was found to be in the range of 3.5 cm²/V-s.

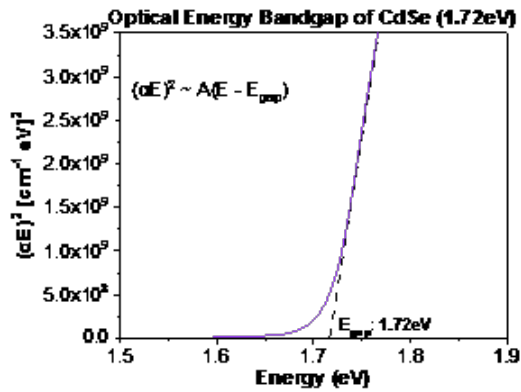


Fig. 2 $(\alpha E)^2$ vs. E curve showing intercept at ~1.72 eV

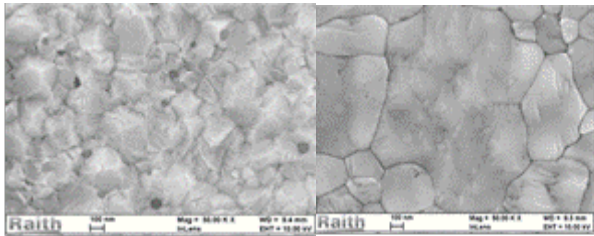


Fig. 3 SEM of grains before(left)and after(right) CdCl₂ treatment for samples deposited on FTO/glass

Drift mobilities were measured using space-charge limited current techniques [6] in both annealed and un-annealed films. The results are shown in Fig.4 and 5 below.

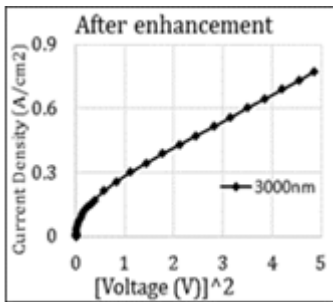


Fig.4 Current vs. Voltage relationship for CdSe films

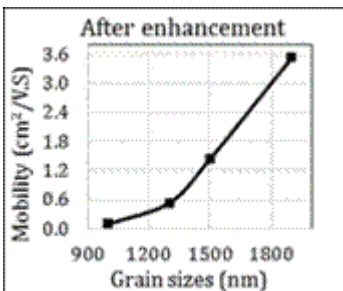


Fig. 5 Mobility vs. grain size after CdCl₂ treatment

III. DEVICE STRUCTURE

Heterojunction devices were made by using n⁺CdS as the n heterojunction layer and an organic semiconductor as p-layer. Three different organic semiconductors were used: P3HT, PTAA and PEDOT:PSS. The reason for using these heterojunction layers was to provide the optimum heterojunction to prevent recombination at the p-n and n⁺-n interfaces. For superstrate devices, we used FTO coated glass and for substrate devices, we used either FTO/glass or a metal. See Fig. 6 for the basic device structure and Fig. 7 for the band diagram of the heterojunction.

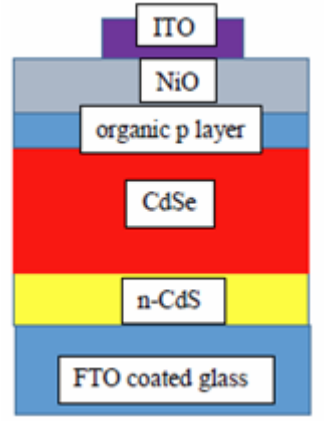


Fig. 6 Heterojunction Device structure for a substrate device

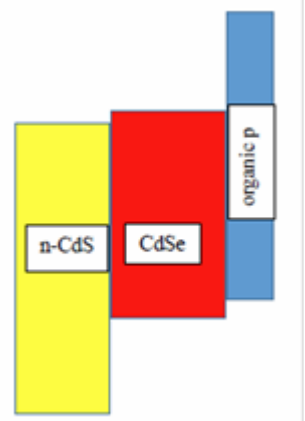


Fig. 7 Band alignments for the n⁺CdS-n CdSe and p-organic layers

IV. DEVICE RESULTS AND INFLUENCE OF POST-DEPOSITION ANNEALING

A major discovery we made was that the performance of the devices could be improved significantly upon annealing the CdSe films after deposition using a CdCl₂ heat treatment. A thin film of CdCl₂ solution in water was deposited on the film after growth and annealed in a nitrogen atmosphere at various temperatures. It was found that the optimum anneal temperature was 450 C. The film was annealed for 10 hours. Higher temperatures anneals led to loss of Se and poorer device performance.

In Fig. 8 we show the I-V curve for a superstrate n⁺/n/p device with light from the n⁺ side. This is obviously the wrong direction for light- for an optimum device it should be entering from the p side; this structure was used to optimize the grain enhancement and Chlorine passivation technique. Note how the current increases significantly upon annealing.

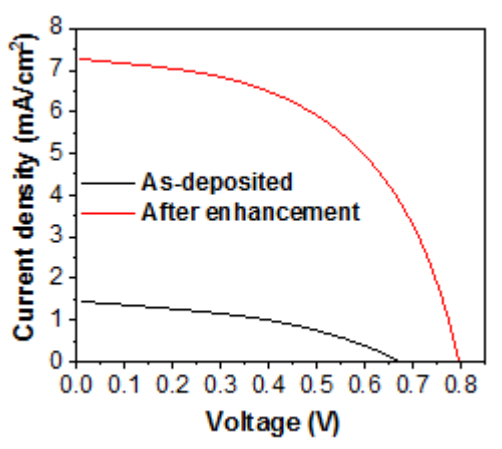


Fig. 8 I-V curve for a superstrate n+/n/p device with light incident from the n+ side. Note how the curve improves significantly upon chemical annealing with CdCl₂. The open circuit voltage achieved is the highest ever in this material.

In Fig. 9 we show the influence of the grain enhancement technique on quantum efficiency—notice the exceptional increase in QE upon grain enhancement, indicating a significant increase in diffusion length of holes.

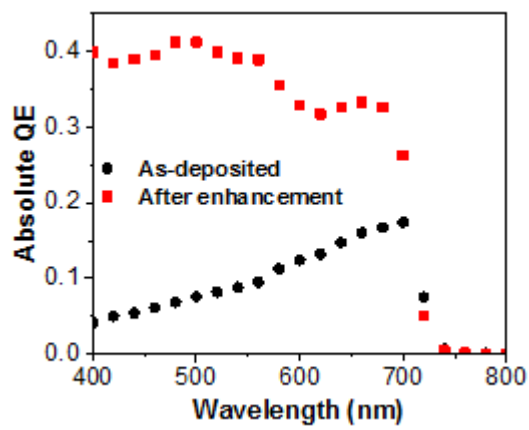


Fig. 9 Influence of CdCl₂ treatment on quantum efficiency of superstrate devices with light incident from bottom n-side. Note the significant increase in QE upon CdCl₂ treatment, particularly for short wavelength photons which are absorbed far away from the p-n junctions. This fact indicates that the diffusion length of holes has increased significantly upon CdCl₂ treatment.

We next proceeded to make substrate devices (light coming from the top). To do this, we had to develop a process for depositing ITO on top of an organic material (PTAA or PEDOT:PSS). We discovered that one could directly deposit ITO on top of PEDOT:PSS without damaging PEDOT:PSS. After the deposition of ITO dots, one had to do dry air plasma passivation of the remaining PEDOT to prevent it from

degrading due to moisture and causing shorts. In Fig.10, we show I-V curve of one of the substrate devices showing an excellent current (~ 10 mA/cm²) and a decent voltage (0.56V), much higher than the previously reported 0.2-0.3V [3]. We need to significantly reduce the shunt conductance in substrate devices to improve the performance.

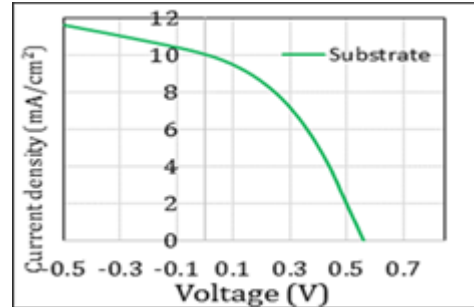


Fig. 10 I-V curve of a substrate device in CdSe, with a top ITO contact on top of the organic heterojunction p layer. Light is incident from the top. Note the excellent current (>10 mA/cm²) and reasonable open-circuit voltage, 0.56V.

V. CONCLUSIONS

In summary, we have shown how one can significantly improve the photovoltaic properties of CdSe solar cells by using post-deposition annealing using a CdCl₂ overlayer at temperatures of 450 °C. Such annealing increases the grain size, the drift mobility and also significantly improves quantum efficiency in devices. We also show that by using appropriate heterojunctions, including the use of inorganic n+ CdS as the n type layer and organic layers (P3HT,PTAA,PEDOT:PSS etc.) as a p-type heterojunction layers. We made both substrate and superstrate type of cells, with light coming either from the top or bottom. A world-record 0.8 V of open circuit voltage was achieved in superstrate cell. We have solved the problem of depositing a transparent contact on top of the organic layer by using an appropriate organic heterojunction layer (PEDOT:PSS) and following it with ITO deposition, which is followed by plasma annealing in a dry air plasma to reduce shunt and to passivate PEDOT.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

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