

GaN/AlN Schottky-gate p-channel HFETs with InGaN contacts and 100 mA/mm on-current

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Abstract — High-performance wide-bandgap p-channel devices which can be monolithically integrated with established wide-bandgap n-channel devices are broadly desirable to expand the design topologies available in power/RF electronics. This work advances the GaN-on-AlN platform as the most promising p-channel contender to enable wide-bandgap complementary electronics. Toward that end, a new generation of GaN-on-AlN p-channel HFETs is fabricated with on-currents exceeding 100 mA/mm at room temperature under moderate drain bias. Key fabrication ingredients to this success are discussed, low-temperature characterization is shared, and new results are benchmarked against the broader literature.

I. INTRODUCTION

A broad range of applications, including consumer and industrial power electronics, high-bandwidth communications, automotive components and critical defense solutions, drive the need for power devices based on wide-gap materials [1]. Gallium Nitride has for years been the leading contender in many applications, spurred on by its combination of high electron mobility, wide bandgap, and built-in polarization, which enable high-frequency, high-voltage, and low on-resistance devices. However, *hole*-based devices in GaN (and more generally among wide-gap platforms) have been largely sidelined in this push. Their lower mobilities, inefficient doping, and poor contacts harshly constrain performance, stifling the emergence of p-channel transistors and the potential use of complementary circuit techniques in GaN-based design [1]. As n-channel devices march toward ever higher frequencies, the lack of monolithically integrable p-channel devices limits the topologies for on-chip control, and thus forces systems engineers to accept painful penalties in the form of parasitic-rich connections to external driving circuitry [2].

Though acceptor doping in the channel leads to disadvantageous electrostatics [3], III-Nitride heterostructures may employ spontaneous/piezoelectric polarization to induce holes. Several such prototypes have been demonstrated: InGaN/GaN [4,5], GaN/AlGaIn [2,6-10], GaN/AlInGaIn [11-13], and GaN/AlN [14-16], with three reporting CMOS operation [2,8,13]. Among these options, the GaN/AlN structure incorporates the maximal all-binary polarization discontinuity, inducing the highest hole densities and lowest sheet resistances for minimal R_{ON} contribution from access parasitics. Leveraging the large bandgap and high thermal conductivity of the AlN buffer as a backbarrier, as well as potential integration with high-voltage AlN/GaN/AlN HEMTs

[17], this structure is one of the most promising p-channel candidates [16].

II. METHODS

The first p-channel transistors on the GaN/AlN platform [14], produced by Li in 2013, came in two varieties: (1) a high-current D-mode device which hit -100 mA/mm when aggressively forced at $V_D = -50$ V, however, it could only be modulated by a factor of ~ 2 - $3\times$, and (2) a low-current E-mode device which was depleted everywhere by epitaxial design and thus required an excessive $V_D = -40$ V to extract only -4 mA/mm (with space-charge limited transport providing essentially no current below that voltage). In 2018, Bader et al [16] interpolated the two designs via a gate recess process to enable E-mode devices with on-currents of -10 mA/mm at a more accessible $V_D = -10$ V and with more conventional output characteristics. In this report, multiple advances have been combined to enable devices which can finally break the -100 mA/mm mark, but at reasonable biases with non-trivial modulation.

First, the heterostructures were grown using Plasma-assisted Molecular Beam Epitaxy (PAMBE) on an MOCVD-grown, C-plane, AlN-on-Sapphire 2-inch template. Epitaxy begins with a 500 nm AlN buffer, then continues through 15 nm of nominally-undoped GaN to form a channel, followed by 15 nm of heavily Mg-doped 5% InGaIn for a contact cap. The Mg concentration is expected to exceed 5×10^{19} /cm³ in this layer. In-situ RHEED monitoring ensured a metal-rich growth regime throughout the entire recipe. Thereafter, the wafer was diced into 8x8 mm pieces and characterized, as shown in **Fig. 1**. X-Ray Diffraction analysis confirmed the intended thicknesses, and Hall effect measurements confirmed a p-type sheet resistivity of ~ 8 - 20 kOhm/sq across the surface of the wafer. When optimized, GaN/AlN heterojunctions provide the highest p-type sheet conductivities among the (single-interface) hole gases in the III-Nitrides [15].

Fig. 2 summarizes the process flow. First, Palladium-based contacts are deposited by e-beam evaporation. As compared with previous demonstrations employing only p-GaN caps, the p-InGaIn cap provides substantial reduction of contact resistance down to the $R_c \sim 5$ Ω mm range as shown in **Figs. 3-4**, and while the contacts are imperfectly linear, they do maintain outstanding low-resistance over a vast current span. With specific resistivities in the low 10^{-5} Ω cm² range, these are on-par with the highest-quality GaN p-contact literature [18]. Further, the use of unalloyed Pd/Ni contacts instead of Ni/Au

contacts allows for greater process flexibility in fabrication facilities where etching tools are often incompatible with the presence of gold. Second, devices are mesa isolated by a high-rate BCl_3/Cl_2 plasma etch. Then a timed, low-damage BCl_3 two-step plasma etch refines the active region dimensions. The first step, a global recess, is masked by only the contacts, stripping the InGaN cap away to reduce gate leakage. The second step, a gate-specific recess to enable full pinchoff, is masked by a thin low-plasma-power PECVD SiO_2 , which is itself patterned only by wet etch, in order to ensure no unintended overetch into the epi-layers. Throughout the process, a UV/Ozone descum is employed wherever possible to clean the surface instead of typical O_2 plasma cleanings. Finally, a Molybdenum-based gate stack is e-beam evaporated. As dielectrics are still relatively unoptimized for p-channel work in this platform, this Schottky gate approach enables much more aggressive characterization and measurement without the hysteresis and breakdown constraints typical in immature MOS devices. The resulting structure is clarified in **Fig. 5**.

III. RESULTS

Output curves in **Figs. 6-7** show on-currents at the scale of ~ 100 mA/mm for the smallest device, with one full order of modulation, and peak transconductance up to 19 mS/mm for a slightly larger device with two orders on/off modulation. Gate leakage is visible in **Figs. 6a/7a** when the gate is driven well beyond the drain. In fact, as seen in **Figs. 6b/7b**, gate leakage limits the turn-off of both devices. However, as this is the first Schottky generation, it is important to note that this limitation is unlikely to be intrinsic: techniques such as (1) reducing the micron-scale overlap of the gate metal beyond the recess by self-aligned or e-beam lithographic processes or (2) surface treatments such as oxidation or chemical preparation prior to gate deposition may strongly affect the diode characteristics. Application of a scaled-EOT dielectric can further reduce the off-currents [16].

Cryogenic measurements, as in **Fig. 8a**, reveal dramatic current improvement up to ~ 300 mA/mm at 77 K, far exceeding previous reports on this platform [14], and also (quite slightly) improve the modulation as shown in **Fig. 8b**. Since degenerate gas densities are roughly constant versus temperature [15], this can be explained in terms of an enhancement of mobility as acoustic phonon populations dwindle [19], only partially mitigated by an increase in contact resistance from the diminished Mg dopant ionization. Both effects are visible in the contact measurements of **Fig. 8c**, and the increased Schottky curvature can also be seen in the low-bias output characteristics of **Fig. 8a** at 77 K. Dramatic performance improvement at low-temperature signals the quality of the polarization-induced hole gas, as compared to dopant-centric approaches which favor high-temperature [3].

Returning to room-temperature characterization, the maximum reported on-current (at $V_D = -5$ V) and best-shown on/off ratio for a collection of p-channel III-Nitride devices in the literature are benchmarked together in **Fig. 9**. It is readily seen that the on-currents here surpass the literature, and, any of

the methods suggested above to enhance the on/off ratio, without detriment to the current, will yield a uniquely well-positioned p-channel option. For a broader comparison, high-voltage Extended-Drain pFETs in 65nm Si CMOS technology generally reach ~ 200 mA/mm [20, 21], so it is exciting that GaN p-HFETs are—despite significantly longer source-drain separations, unscaled gates, and more resistive contacts—now within striking distance. Stepping back, the fundamental material parameters which predict optimal high-voltage operation are plotted in terms of the Baliga Figure of Merit [22] in **Fig. 10**. The high polarization-induced sheet charge combined with large bandgaps suggests a strong ultimate power limit. Finally, **Fig. 11** shows the $k \cdot p$ calculated band structure of the hole gas, which is dominated by heavy holes. This suggests an interesting avenue for strain engineering, which has recently been proposed for this structure [19] to further enhance performance.

IV. CONCLUSION

This work has demonstrated the strongest on-current performance of any significantly modulating p-channel transistor in the III-Nitrides, characterized the devices across multiple temperatures, and discussed directions for further advancement in the field, encouraging further study of the GaN/AlN platform to power a wide-bandgap CMOS technology.

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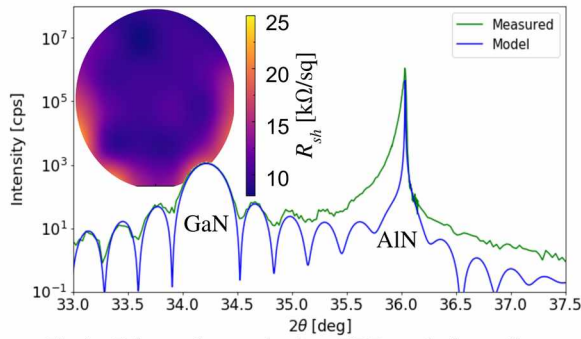


Fig 1. Epitaxy characterization: XRD analysis confirms layer thicknesses and, on inset, a sheet resistance map reveals a conductive hole gas across nearly the entire 2'' wafer.

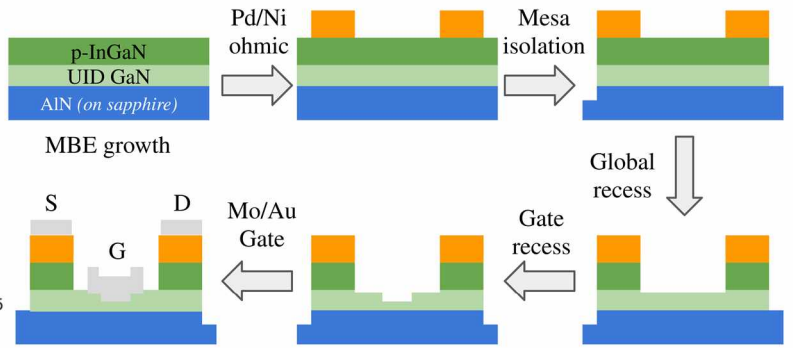


Fig 2. Process overview including (1) gold-free ohmics, (2) two recess steps, one to remove leaky p-InGaN, one to thin the gate-channel distance, and (3) Schottky gate.

Fig 3. CTLM measurements [inner diameter 50μm] of unalloyed Pd-based contacts on 2DHG structures with various p-cap layers show that moving to a finite Indium composition allows for reduced contact resistances to the 2DHG. (a) Direct I-V measurements showing the improved linearity (b) Total resistance [V/I] vs spacing curves showing diminished contact resistance at similar sheet resistance. [p+ and p++ indicate growth conditions leading to GaN:Mg concentrations of approximately $1 \times 10^{19}/\text{cm}^2$ and approximately $4 \times 10^{19}/\text{cm}^2$ respectively. p++ InGaN contacts in the 5-10 Ωmm range, similar to the green data points, are typical of our process.]

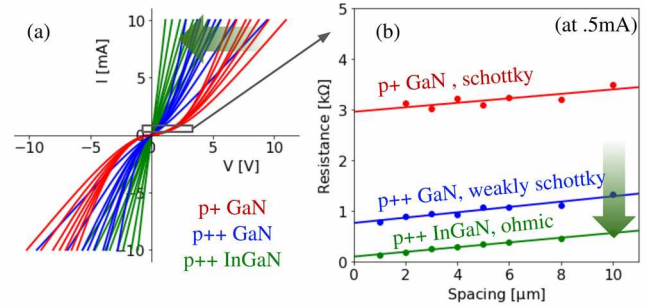


Fig 4. (a) Linear TLM I-Vs of representative unalloyed Pd/Ni contacts on the reported sample, (b) total resistance versus spacing curve extracted at high current levels, and (c) resistances versus current level showing highly conductive but imperfectly ohmic behavior.

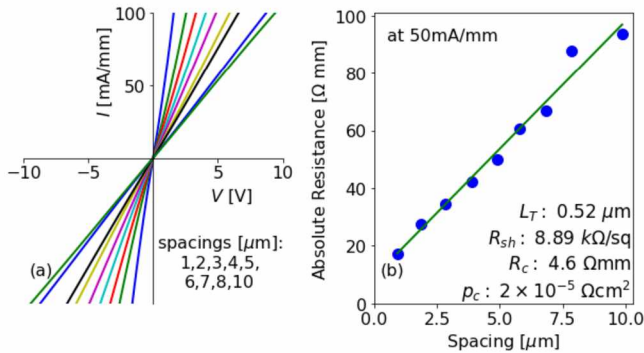
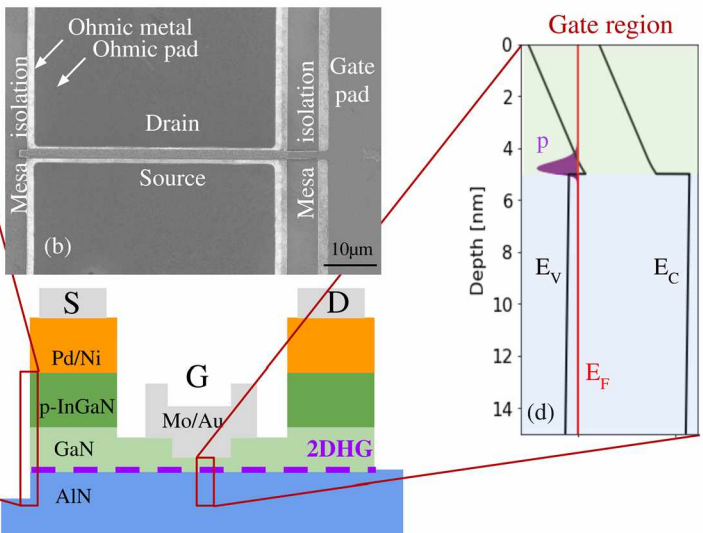
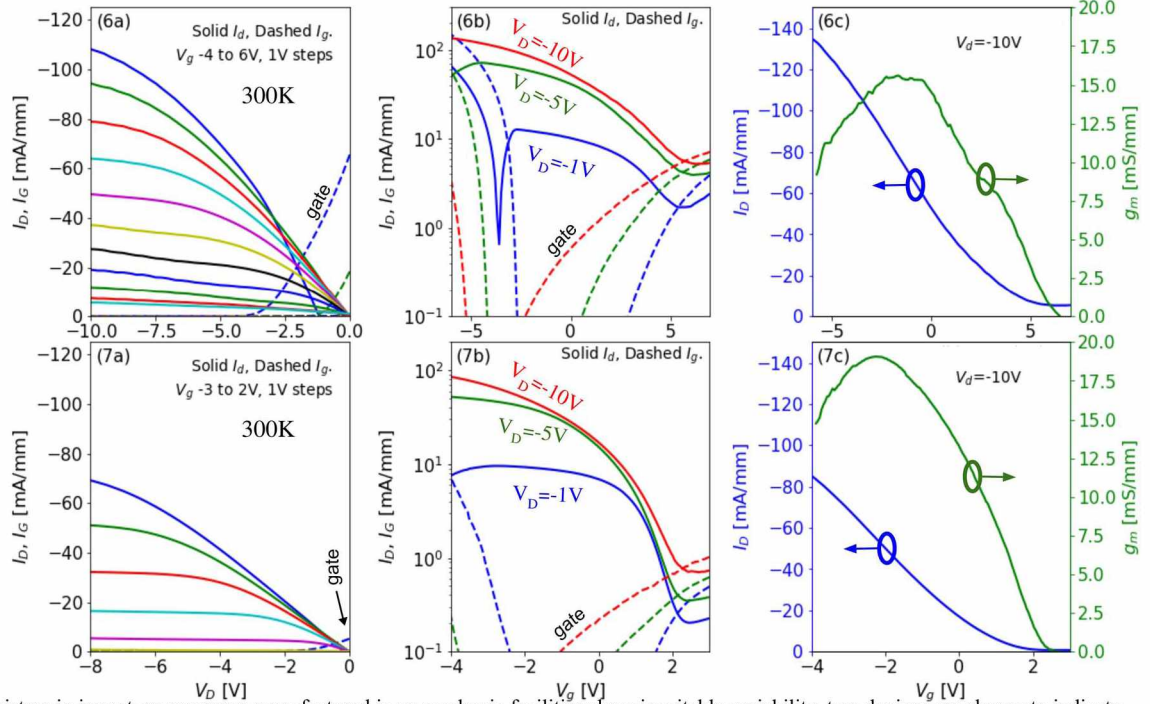


Fig 5. (a) Cross-section cartoon and (b) post-fabrication top-view SEM of the Schottky-gated device. The gate lengths given for specific devices in other figures are defined by the intended recess widths rather than the gate metal which overlaps past the recess boundaries. Band diagrams are provided for the (c) contact regions and (d) gated region at equilibrium showing the confined 2D hole gas.



$L_G/L_{SD} = 0.6 \mu\text{m} / 3.5 \mu\text{m}$
High current device

$L_G/L_{SD} = 0.8 \mu\text{m} / 4 \mu\text{m}$
High gain device



Figs 6 & 7. While transistors in immature processes manufactured in an academic facilities show inevitable variability, two devices are chosen to indicate the breadth of observed characteristics. The $L_G/L_{SD}=6/3.5\mu\text{m}$ device in (6a-c) is marked by a high on-current (a,c), exceeding .1 A/mm, and shows about 1 order on/off ratio limited by Schottky gate leakage. The $L_G/L_{SD}=8/4\mu\text{m}$ device in (7a-c) has on-currents which, while not as high as the first, still stand above the literature. This device also holds 2 orders on/off ratio, limited by Schottky leakage, and modulates more efficiently as a function of voltage [note different x-axes in Figs 6 vs 7], resulting in an even higher peak transconductance of $\sim 19\text{mS/mm}$. Either device alone, or any interpolation between them, marks a domain (see Fig 9) never before reached in the III-Nitride pFET literature.

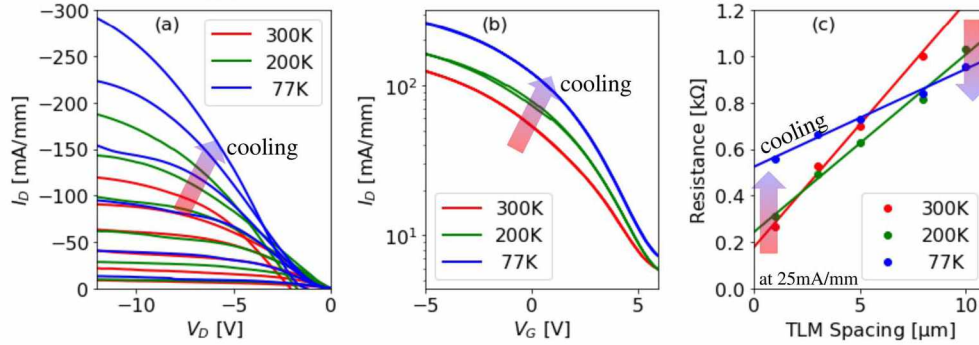


Fig 8. (a) Output characteristics and (b) transfer characteristics of the same device from Fig. 6, at reduced temperature, showing on-currents enhanced nearly 3x. As can be seen in (c) T-dependent TLMs, this correlates with a reduction of sheet resistance (enhanced mobility), partially countered by an increased contact resistance.

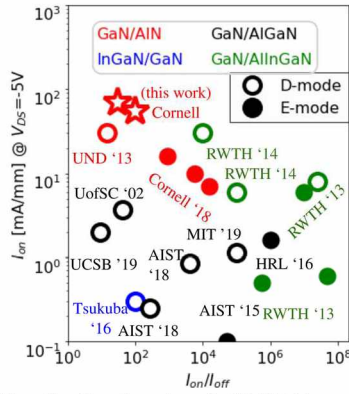


Fig 9. Benchmark of III-Nitride p-channel devices contextualizing the impressive on-currents. Noting that this is a rapidly advancing field, it is critical to timestamp this benchmark as drawn from only the publicly available literature as of July 2019.

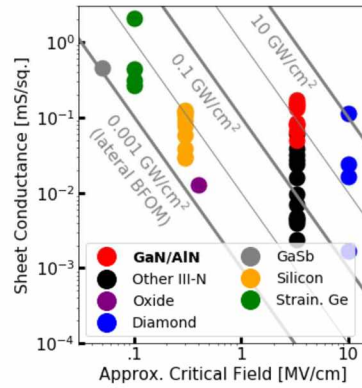


Fig 10. Baliga FOM plot for various 2DHG p-channel platforms, showing the material advantage of the GaN/AlN system. References for the various conductivity values can be found in Chaudhuri [15], while the critical fields are estimated by reports for the critical field of the smaller material at any interface, neglecting alloy effects. The only listed material with a higher FOM than III-Nitrides is Diamond, where it happens that n -channel devices are the difficulty. (Reports of SiC pMOS do not provide a sheet conductance, however both the interface hole mobility thus far [23] and critical field are smaller than GaN.)

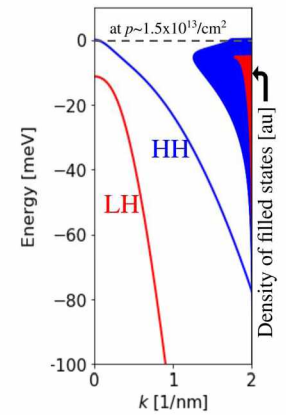


Fig 11. Valence band structure of a gated 2DHG, dominated by Heavy Holes. See [19] for discussion of how strain can resculpt the bands.