Fault Recovery in Micro-Electrode-Dot-Array Digital Microfluidic Biochips Using an IJTAG Network*

Zhanwei Zhong and Krishnendu Chakrabarty
Duke University, Durham, NC

***Abstract*—A digital microfluidic biochip (DMFB) is an attractive platform for immunoassays, point-of-care clinical diagnostics, DNA sequencing, and other laboratory procedures in biochemistry. A recent generation of biochips uses a micro-electrode-dot-array (MEDA) architecture, which provides fine-grained controllability of droplets and seamlessly integrates microelectronics and microfluidics using CMOS technology. In order to ensure robust fluidic operations and high confidence in the outcome of biochemical experiments, chip testing, fault diagnosis and fault recovery are critical for MEDA biochips. In this paper, we present an effective fault-recovery solution based on the homogeneous structure of MEDA. Since the microelectrode cell (MCs) in a MEDA biochip are identical, we add multiplexers for reconfigurability, whereby an MC with faulty components can use the hardware resources in a neighboring MC. In addition, we use the IEEE 1687 (a.k.a. IJTAG) network to reduce the number of control signals need for the multiplexers, and to provide flexible sub-scan chain access for the fault-recovery control flow. A comprehensive set of simulation results demonstrates the effectiveness of the proposed fault-recovery solution for MEDA biochips.**

I. Introduction

A digital microfluidic biochip (DMFB) is an example of a lab-on-a-chip that is capable of performing biochemical experiments. Over the past decade, DMFBs have been demonstrated for high-throughput DNA sequencing, point-of-care clinical diagnostics, and protein crystallization for drug discovery [1], [2]. A DMFB manipulates liquids as discrete droplets of nanoliter and picoliter volumes based on the principle of electrowetting-on-dielectric (EWOD). Compared with continuous-flow biochips, which use permanently etched microchannels, a DMFB offers the advantages of simple instrumentation, flexible device geometry, reconfigurability, and ease of coupling with other technologies [2]. Illumina, a market leader in DNA sequencing, has transitioned digital microfluidics to the marketplace for sample preparation [3]. This technology has also been deployed by Genmark for infectious disease testing [4] and by Baebies to detect lysosomal enzymes in newborns [5]. These milestones highlight the emergence of DMFB technology for commercial exploitation.

However, DMFBs available in the marketplace today suffer from several limitations: (i) constraints on droplet size and the inability to vary droplet volume in a fine-grained manner, (ii) the lack of integrated sensors for real-time detection, and (iii) the need for special fabrication processes and the associated reliability/yield concerns. To overcome the above limitations, a micro-electrode dot array (MEDA) architecture has been proposed [6]. Unlike conventional digital microfluidics, where electrodes of equal size are arranged in a regular pattern, the MEDA architecture is based on the concept of a sea-of-micro-electrodes. Each microelectrode cell (MC) consists of a microelectrode, an activation circuit, and a sensing circuit. MEDA allows microelectrodes to be dynamically grouped to perform different microfluidic operations on the chip. Prototypes of MEDA biochips have been fabricated using TSMC 0.35 μm CMOS technology [7], and these devices can use a power-supply voltage of only 3.3 V [8]. MEDA also incorporates real-time capacitive sensing on every microelectrode to detect the property and the location of a droplet. The sensing map derived in this manner allows MEDA biochips to dynamically respond to bioassay outcomes, perform realtime error recovery, and execute if-then-else protocols from biochemistry [9], [10].

While the above benefits continue to drive research in MEDA biochips, fabrication defects, imperfections, and wear-out are major concerns on an emerging technology platform [11], [12]. Testing and fault tolerance are therefore key for technology maturation [13], [14]. According to [15], there are two typical defect types in MEDA biochips, namely intra-MC defects (e.g., transistors in the MC are stuck-on) and inter-MC defects (e.g., hard- and resistive-shorts between two microelectrodes). Defects may eventually result in errors, which can adversely impact the correctness of the entire experiment [16]. In order to ensure an adequate quality level before being used for bioassay execution, MEDA biochips need to be tested and diagnosed for defects. Moreover, many biochips are expected to be used for healthcare and medical diagnostics.. Therefore, these biochips must be designed to be fault-tolerant such that they can continue to operate reliably in the presence of faults.

There has been some early work on test methods and fault-tolerance strategies for MEDA biochips. Oscillation-based test methods for offline error detection have been proposed in [17]. The work in [18] presents the first MEDA biochip design with a built-in-self-test (BIST) test structure. The BIST structure is based on on-chip capacitance sensing circuits, and it can effectively detect malfunctioned microelectrodes based on the capacitance sensing result. A more advanced BIST architecture that targets on both intra-MC and inter-MC testing for MEDA biochips is presented in [16].

The above methods addressed defect detection and diagnosis; however, they did not attempt to tolerate or recover from defects. Test methods for MEDA must also consider the scan-chain (daisy chain) design, in which D flip-flops (DFFs) under the MCs are serially connected (see Section II.A). A built-in-self-diagnosis and fault-tolerant scan-chain design specific to MEDA biochips was proposed in [19]. This design aims to detect and locate one or multiple faults in the D flip-flops (DFFs), and ensures recovery from these faults. However, faults are not limited to DFFs; they can also occur in the activation and

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sensing circuits in the MEDA platform. detect and tolerate defects in the activation Moreover, [19] does not consider defects between two neighboring MCs; the oper transmission in the scan chain, and the bi anymore. Finally, this design added a by each MC (1800 in total for a fabricated M but it did not discuss how to generate th these multiplexers.

In order to overcome these drawbacks, recovery solution for MEDA biochips. The this paper are as follows:

- We propose a fault-recovery design for an MC contains a defect, it can use th of a neighboring MC to operate correc approach is based on the homogeneous biochip (e.g., a prototype fabricated at identical MCs).
- Suppose the ith MC is used as a bac which is faulty. In such a scenario, due the ith MC cannot concurrently perfor fault-free ith MC and as a backup for j we present a fault-recovery control flow, a schedule for faulty and healthy MCs sc conflict occurs.
- In our design, five multiplexers are add which introduces the problem of how to c plexers efficiently. In order to reduce the signals, we first divide the scan chain in length sub-scan chains, and then utilize th (IJTAG) network to provide individual acce sub-scan chain. In this way, the sub-scan ch same control signals, which reduces the signals that are needed.

The remainder of the paper is organized a II describes the basics of microelectrode cell and the IJTAG network. Section III describes design for each MC. Section IV presents th used in our design and discusses the cont recovery. Section V presents simulation resu effectiveness of the proposed technique. Finally, Section VI concludes the paper.

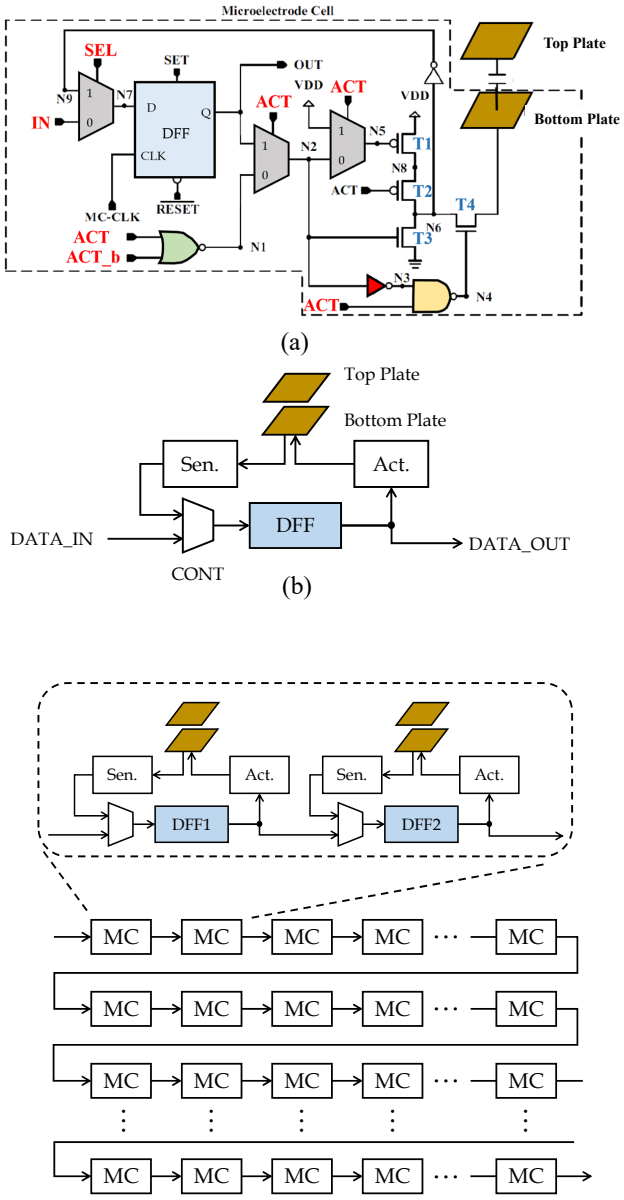


Fig. 2. An illustration of the scan-chain structure in MEDA.

II. Background

A. Microelectrode Cell and Scan Chain

A MEDA biochip consists of repeated instances of a basic unit called the microelectrode cell (MC). A typical MC includes four parts: a microelectrode (a top plate + a bottom plate), a DFF, an activation circuit, and a sensing circuit. The schematic and the logic abstraction of an MC is shown in Fig. 1.

In order to perform droplet operations on MEDA, we need to activate a group of MCs to form a micro-component (e.g., splitter or mixer). When an MC is activated, a high voltage of 25 V [18] is applied to the top plate, and the bottom plate is connected to the ground (0V). Because there is a potential difference, it will generate a force that can drag a droplet towards itself. When an MC is de-activated, the high voltage of 25 V is still applied to the top plate, however, the bottom plate is floating and an induced voltage of 17 V is generated. In this case, the potential difference between the top plate and the bottom plate is too small to generate a force. The electrical connection to the bottom plate is controlled by the activation circuit and the DFF. A value "0" in the DFF indicates MC de-activation; otherwise, the MC is activated.

Besides MC activation, the sensing circuit in each MC can also measure the capacitance between the top plate and bottom plate. By comparing the sensed capacitance to a preset value, it can determine whether a droplet is present between the top plate and bottom plate. A value of "0" indicates that no droplet is present; otherwise, a droplet is present. This "0/1" sensing result generated by the sensing circuit is then be stored in the DFF for readout.

In order to write an activation pattern to each MC and read out the sensing results, MCs are connected using a single scan-chain

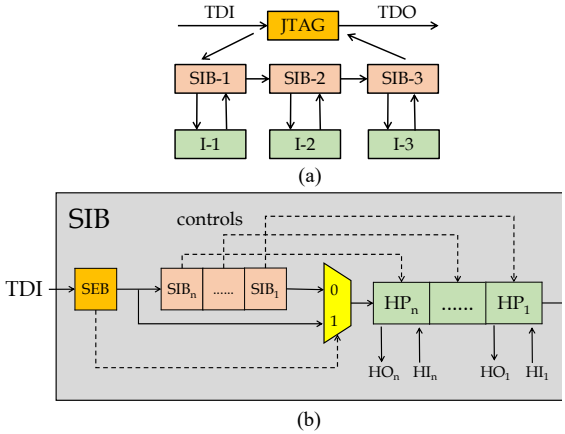


Fig. 3. (a) An example of an IJTAG network and (b) a simplified SIB design.

structure, i.e., the output of one MC is connected to of the next MC (see Fig. 2). Using the scan chain, an a pattern can be sequentially shifted into each individual the sensing result stored in each DFF can also be sec shifted out for readout. The scan chain achieves 100% of every MC with only seven control pins, i.e., CO RESET, ACT,ACT b, IN, and OUT, as shown in Fig.

B. The IJTAG Network

The IEEE Std. 1687 (a.k.a. IJTAG) [20] provides flexible access to on-chip instruments through the IEEE 1149 JTAG test access port (TAP) [21]. It is now being increasingly used for post-silicon validation, production test, fault diagnosis, and fault monitoring [22]. To provide flexibility of instrument access, a hardware component called the Segment Insertion Bit (SIB) has been introduced [20]. The SIBs in the 1687 network are used to select or unselect multiple network segments for the scan chain. It operates in two states: (1) if it is open, it includes the segment in the scan path; (2) if it is closed, it excludes the segment from the scan path. The state of the SIB is configured by first shifting in a control bit ("0" for close and "1" for open) into its register, and then updating its register on capture, shift, and update (CSU) cycles [23].

As shown in Fig. 3(a), the JTAG interface is a doorway that controls and manages SIB-1, SIB-2, and SIB-3. In addition, three instruments (e.g., sub-scan chain) I-1, I-2 and I-3 are connected to SIB-1, SIB-2, and SIB-3, respectively. Suppose we need to access the instruments I-1 and I-3, in this case, we only need to configure the control bits of SIB-1, SIB-2 and SIB-3 as "1", "0" and "1", respectively. As a result, I-1 and I-3 are selected while I-2 is unselected.

As shown in Fig. 3, a SIB component primarily includes three parts:

1) Hierarchial Port (*HB*): Each HB is connected to a lower level of the IJTAG network segment.

2) SIB Bits: When $SIB = 1(0)$, the corresponding HP is open (close), and the segment on this HP is included (excluded) in (from) the primary scan path.

3) SIB Exclusion Bit (*SEB*): When $SEB = 1$, the SIB bits are not included into the scan path (i.e., they are bypassed). This feature can be utilized to reduce the SIB overhead [24]. When $SEB = 0$, the SIB components are included in the primary scan path.

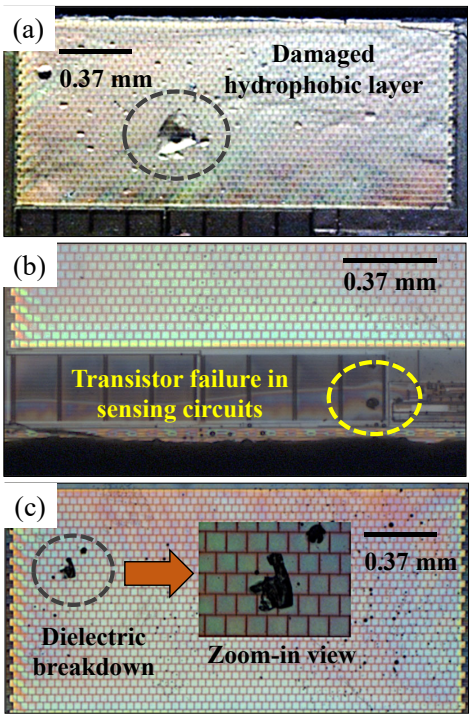


Fig. 4. Images of some typical visible defects in a fabricated MEDA biochip. (a) Defect in the hydrophobic layer. (b) Defective transistors in peripheral circuits. (c) Defect in the dielectric layer.

C. Defects in MEDA

As feature sizes scale down in MEDA biochips, the sizes of microelectrodes and distances between microelectrodes are also reduced to achieve higher levels of integration. This increasing density increases the likelihood of defects. Some typical defects and the corresponding fault models are listed below:

1) Defects in the hydrophobic layer. A hydrophobic layer is used to increase the electrowetting force for transporting droplets [2]. This layer can be damaged by chemical reactions and physical scratches. A damaged hydrophobic layer, as shown in Fig. 4(a) for a fabricated chip, cannot provide adequate electrowetting force when electrodes are actuated.

2) Transistor failures. These failures in control and sensing circuits can result in incorrect droplet actuation, maintenance, and sensing. An example of a transistor failure in the capacitive-sensing circuit of a fabricated chip [18] is shown in Fig. 4(b). Traditional fault models, such as stuck-at faults and bridging faults, can be utilized in these cases.

3) Dielectric breakdown. High voltages applied to electrodes can cause dielectric breakdown, which leads to the direct exposure of a droplet to high voltage and results in droplet electrolysis. Dielectric breakdown is illustrated in Fig. 4(c) for a fabricated chip. In this case, droplet electrolysis occurs, and the droplet cannot be controlled.

4) Short-circuited microelectrodes. A short between two adjacent electrodes leads to a "larger" macro-electrode and the two electrodes cannot be controlled independently. Moreover, once a droplet resides on this macro-electrode, it is no longer

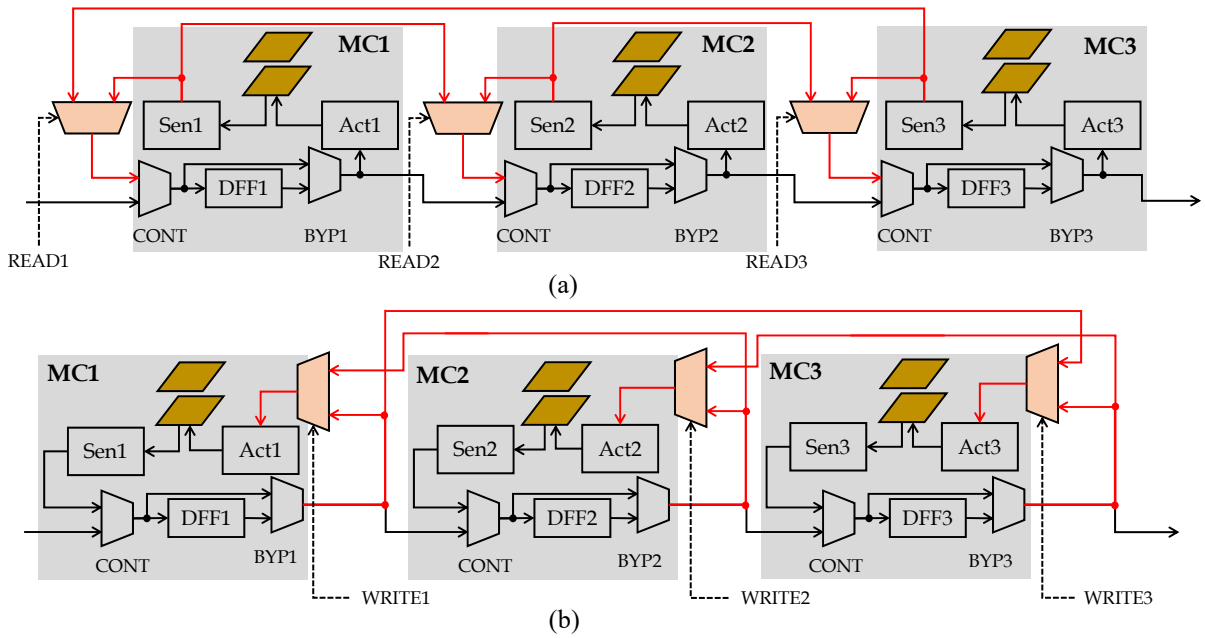


Fig. 5. Fault-recovery designs for (a) DFF read, and (b) DFF write with one backup MC.

possible to create the interfacial surface tension along the droplet transportation path.

III. Fault-recovery Design

In this section, we introduce the fault-recovery design for each MC. The main idea is as follows: because the MCs are identical, when a fault occurs in a certain MC, it can use the hardware resources in a neighboring MC to operate correctly. We present four fault-recovery designs for the DFFs as well as for the activation and sensing circuits.

A. Designs for DFF Read and DFF Write

Recall that on the MEDA biochip, some of the MCs need to be activated to perform droplet operations. In order to do that, a "0/1" activation pattern is serially shifted in each of the DFF through the scan chain to control the activation status of each MC. On the other hand, when the sensing circuit in each MC obtains the "0/1" sensing result, it will be stored into the DFF and then be serially shifted out.

However, if the DFF is faulty (e.g., the output is stuck at a fixed value), the activation status of an MC is not controllable and the sensing result will be discarded. More importantly, some of the DFFs in the scan chain will receive an incorrect sequence due to the faulty DFF. Therefore, it is important to recover from any DFF fault.

Before presenting the fault-recovery design, we introduce some definitions. In our design, each faulty MC will use the hardware resources of neighboring MCs. We define these neighboring MCs as the *backup MCs*. Note that there can be many choices for backup MCs; in this paper, we simply select the downstream MCs as the backup MCs, and do it in a cyclic way. For example, if we have three DFFs (DFF1 $\rightarrow$ DFF2 $\rightarrow$ DFF3) and the number of backup MCs is equal to 1, then DFF2 is the backup MC for DFF1, DFF3 is the backup MC for DFF2, and finally DFF1 is the backup MC for DFF3. However, if the number of backup MCs is equal to 2, then DFF2 and DFF3 are the backup MCs for DFF1, DFF3 and DFF1 are the backup MCs for DFF2, and finally DFF1 and DFF2 are the backup MCs for DFF3.

The fault-recovery designs for DFF read (read sensing result) and DFF write (write activation pattern) are shown in Fig. 5. In order to simplify the illustration, we only show the design for three MCs, and the number of backup MCs is set to 1. For the DFF read circuit, a multiplexer (in pink color) is added on the left side of each MC, so that each DFF can receive the sensing results from one of the two sensing circuits: one from a local MC and the other from a potentially faulty MC. For example, as shown in Fig. 5(a), DFF2 receives the sensing result from Sen1 and Sen2. If DFF1 is faulty and cannot store the sensing result from Sen1, DFF2 can be used to store the sensing result from Sen1. In this case, if there is a fault in DFF1, we can recover from it by using the DFF2 in MC2.

For the DFF write circuit, a multiplexer (in pink color) is added on the right side of each MC, such that the activation circuit can be controlled by one of the two DFFs: one from a local MC and the other from a backup MC. For example, as shown in Fig. 5(b), Act1 receives the control signals either from DFF1 or from DFF2. If DFF1 is faulty (i.e., stuck at 1) and cannot change the control signal, then DFF2 can be used to send the correct control signal to Act1.

Finally, in both designs, a multiplexer on the right of each DFF is added to create a bypass path, such that even if a DFF is faulty, data shifting is still possible through the bypassing of the faulty DFF. Note that in order to perform fault-recovery on DFFs, individual control signals for all added multiplexers are needed. READ1-READ3 are used for the DFF read, WRITE1-WRITE3 are used for the DFF write, and BYP1-BYP3 are used to create the bypass paths in case of DFF failures.

B. Designs for MC Activation and Capacitance Sensing

The fault-recovery designs for MC activation and capacitance sensing are shown in Fig. 6. For simplicity, we only show the

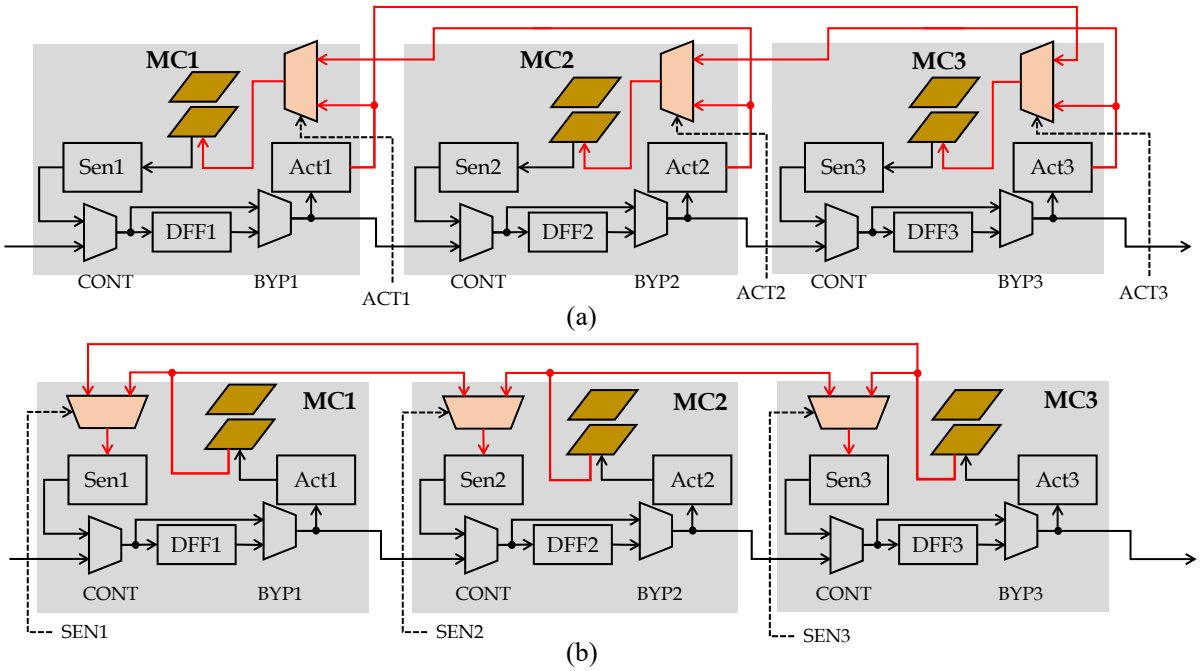


Fig. 6. Fault-recovery designs for (a) MC activation, and (b) capacitive sensing with one backup MC.

designs for three MCs, and the number of backup MCs is set to 1. For MC activation, a multiplexer (in pink color) is added on the right side of each MC, so that each bottom plate can be driven by one of the two activation circuits: one from a local MC and the other from a backup MC. For example, as shown in Fig. 6(a), the bottom plate in MC1 can be driven either by Act1 or by Act2. If Act1 is faulty (i.e., cannot be grounded), then Act2 can be used to drive the bottom plate in MC1. In this case, even if there is a fault in Act1, we can recover from it using the Act2 in MC2.

For capacitance sensing, a multiplexer (shown in pink) is added on the left side of each MC, such that the sensing circuit can measure the capacitance of one of the two MCs: one is a local MC and the other is a potentially faulty MC. For example, as shown in Fig. 6(b), Sen2 can measure the capacitance of either MC1 or MC2. If Sen1 is faulty and cannot measure the capacitance of MC1, we can use Sen2 instead.

In order to perform fault-recovery for MC activation and capacitive sensing, individual control signals for all the added multiplexers are also needed. The ACT1-ACT3 signals are used for MC activation, the SEN1-SEN3 signals are used for capacitance sensing, and finally, the BYP1-BYP3 signals are used to create the bypass paths in case of DFF failures.

C. Discussion

In the previous subsections, we introduced fault-recovery designs for DFF read, DFF write, MC activation and capacitance sensing, respectively. Fig. 7 shows the design that integrates all the four fault-recovery circuits into each MC. Note that in order to simplify the illustration, we show only two MCs in the figure.

The fault-recovery designs in Fig. 5 and Fig. 6 all assume that the number of backup MCs to be 1. For example, if DFF1 is faulty, we can attempt to recover from this fault using only DFF2. However, if DFF2 is also faulty, it is impossible to recover from this fault. An easy way to improve the recoverability of faults in an MC is to increase the number of backup MCs, because multiple backup MCs can be used for fault-recovery purpose, and the likelihood that all these backup MCs are faulty is relatively low. Returning to the previous example, suppose that the number of backup MCs is increased from 1 to 2, and DFF2 and DFF3 are the backup MCs for DFF1. Even if DFF2 is faulty, we can still use DFF3 as a backup. In this case, the recoverability of a faulty MC is increased.

However, increasing the number of backup MCs leads to more control inputs for multiplexers and thus more control signals. Considering the circuit in Fig. 7, suppose the number of backup MCs is equal to N; then four $(N+1)$-input and one 2-input multiplexers are needed for each MC, and each $(N+1)$-input multiplexer needs at least $\lceil \log_2(N+1) \rceil$ control bits. Therefore, if there are M MCs on MEDA, a total of $M \times (4 \times \lceil \log_2(N+1) \rceil + 1)$ control signals are needed.

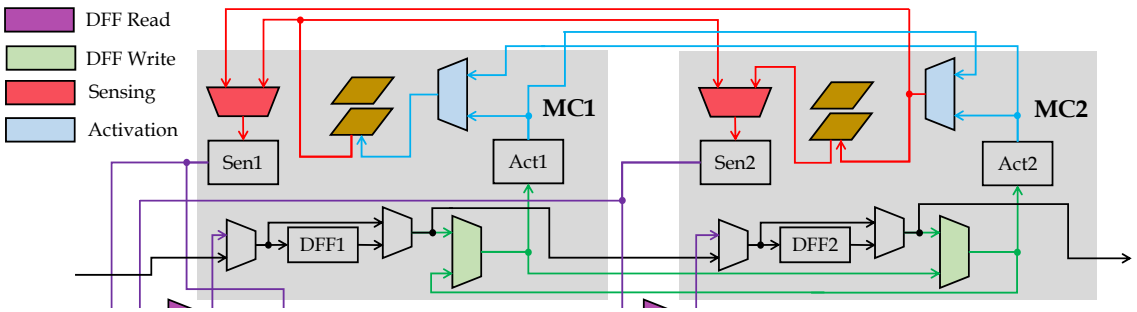
For example, suppose the number of backup MCs is equal to 1. For a fabricated MEDA biochip with 1800 MCs, we will need to generate $1800 \times 5 = 9000$ control signals for the multiplexers, which is not practical and hard to implement. In order to reduce the number of control signals, we utilize the IJTAG network.

IV. Overall Fault-Recovery Design

In the previous section, we introduced fault-recovery design for each MC. When a fault occurs in a certain MC, it can use the hardware resources in a backup MC to operate correctly. However, due to hardware sharing, an MC cannot be used for normal operation and fault recovery at the same time. Therefore, in this section, we present a fault-recovery control flow, which determines a schedule for faulty and healthy MCs so that no hardware conflict occurs.

A. IJTAG Network for Fault Recovery

Fig. 8 shows the IJTAG network that we are proposing for the fault-recovery design. It primarily includes three parts:



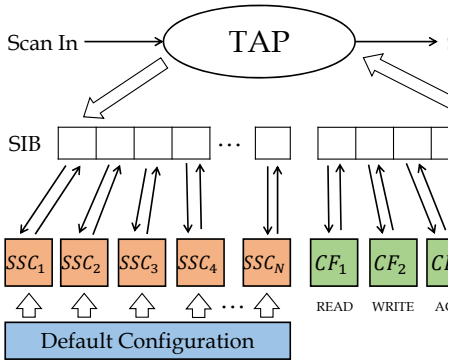


Fig. 8. Illustration of the IJTAG network used fo

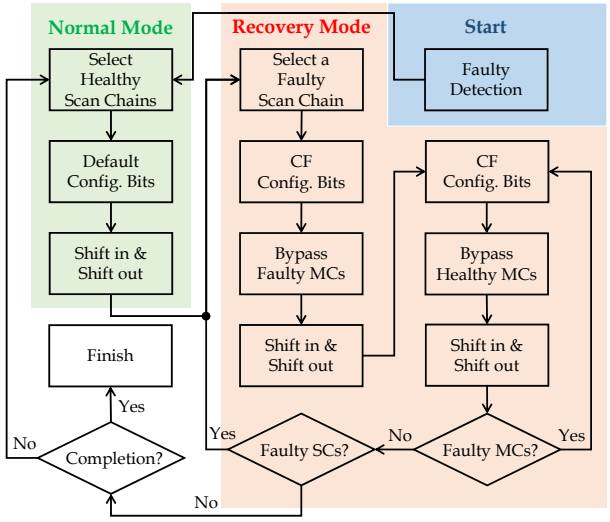


Fig. 9. A fine-grained control flow for fault recovery.

1) Sub-Scan Chain (SSC). In the original all the MCs are sequentially connected togetl scan chain. However, this design is not robu connection between two MCs is open, data sl in this case. Therefore, in the IJTAG netwo the scan chain into multiple equal-length SSCs, and then assign each to a SIB register. In this case, even if a connection between two MCs is open, we just need to bypass the non-functional SSC instead of discarding the biochip. As shown in Fig. 8, the red blocks indicate the SSCs, and the subscript represent the index of each SSC. If we have N SSCs, the subscripts will range from 1 to N.

2) Configuration Registers (CF). In addition to a more robust scan chain design, the IJTAG network also provides us with access flexibility for SSCs (i.e., each of them can be accessed individually). Rather than recovering from all the faults in the scan chain at the same time, we can do it in a time-multiplexed manner (i.e., recover from the faults in one SSC at a time). Because fault recovery is performed in different SSCs at different times, the SSCs can share the control signals for the multiplexers without any conflict. Therefore, instead of $M \times (4 \times \lceil log_2(N+1) \rceil + 1)$ control signals in the original design, we now need to generate $M^* \times (4 \times \lceil log_2(N+1) \rceil + 1)$ control signals, where M is the number of MC in MEDA and M^* is the number of MCs in an SSC.

As shown in Fig. 8, CF_1 to CF_5 (in green color) are the configuration registers. They generate the control signals of READ, WRITE, ACT, SEN and BYP for a SSC, respectively. Each of these configuration registers is connected to a SIB register; therefore, we can easily change the control signals for multiplexers by shifting the configuration patterns into these configuration registers.

3) Default Configuration. In the fault-recovery design, each MC can use the hardware resources of a backup MC. However, if an MC is fault-free (healthy), it will not use any of the backup MCs to operate correctly. In this case, we define the control signals (i.e., READ, WRITE, ACT, SEN and BYP) set up for a healthy MC as the *default configuration*. In the IJTAG network, the default values of READ, WRITE, ACT, SEN and BYP are provided to the corresponding multiplexers in the design. For a single SSC, we can choose to configure the multiplexers using either the *default configuration* or a *customized configuration* from the configuration registers (i.e., CF_1 to CF_5).

B. Control Flow for Multiplexing

Based on the above IJTAG network, we propose a fine-grained control flow to ensure correct operation of each MC; see Fig. 9. First, we detect and locate the faulty components in a MEDA biochip using the methods presented in [16], [19]. In this case, the types and locations of defects are known *a priori*. Next, the remaining part of the control flow can be described in terms of two working modes:

1) Normal Mode. In this mode, all healthy SSCs are selected by the IJTAG network (faulty SSCs are not selected), and we configure MCs in healthy SSCs using the default configuration.

Next, an activation pattern is shifted into the healthy
the sensing results from these SSCs are then shifted

2) Recovery Mode. In this mode, fault recovery is
sequentially for each faulty SSC. First, a faulty
is selected by the IJTAG network. Next, we cor
multiplexers in the selected faulty SSC using the co
registers such that all the faulty MCs are bypassed,
healthy MCs use the default configuration. In this ca
perform activation-pattern shift-in and sensing-resul
for these healthy MCs.

Next, we again configure the multiplexers of the
using the configuration registers such that all the he
are bypassed, and each faulty MC uses the appropri
hardware resources. In this case, we can perform
pattern shift-in and sensing-result shift-out for these f
However, if there are many faults, it is likely that
recover all faulty MCs in only one configuration.
we need to check whether all the faulty MCs operat
using backup MCs. If this is the case, we repeat the
for the next faulty SSC; otherwise, we continue fault recovery until all the *recoverable* faulty MCs perform their functionality correctly using backup MCs.

Here, a *recoverable* faulty MC is an MC that can recover from faults using backup MCs. However, in some cases, an MC is *not recoverable*. For example, suppose the sensing circuit in MC_1 is faulty, and MC_2 is the only backup MC for MC_1. If MC-activation is performed, fault recovery is not needed. However, if capacitance-sensing is performed, fault recovery is needed for MC_1. In this case, if the sensing circuit in MC_2 is fault-free, MC_1 is recoverable. Otherwise, MC1 is not recoverable.

From the above example, we can see that the set of *recoverable* MCs in a faulty SSC can be different for an MC-activation operation and a capacitance-sensing operation. Here, suppose the number of *recoverable* MCs in a faulty SSC are N_{act} and N_{sen} for a MC-activation operation and a capacitance-sensing operation, respectively. Then, the number of multiplexer configurations for this SSC is $N_{act} + N_{sen}$ in the worst case (i.e., fault recovery for one faulty MC in one configuration).

C. An Illustrative Example

In order to make the control flow easier to understand, we use an illustrative example; see Fig. 10. We consider a fabricated MEDA biochip with 1800 MCs [16]. Suppose the scan chain is divided into 60 SSCs; then we have 30 MCs in for each SSC. We also assume that a fault occurs in the sensing circuit of MC1 in SC3. The following three steps need to be carried out for the control flow in Fig. 9:

Step 0: . We detect and locate the faults using the methods presented in [16], [19]. Therefore, the types and locations of defects are known in advance.

Step 1: All healthy SSCs (except for SSC_3) are selected by the IJTAG network, and all the healthy sub scan chains use the default configuration. Next, activation pattern shift-in and sensing result shift-out are performed.

Step 2: The faulty SSC_3 is selected by the IJTAG network, and the configuration registers are used such that the faulty MC1 is bypassed; the rest of the MCs use the default configuration.

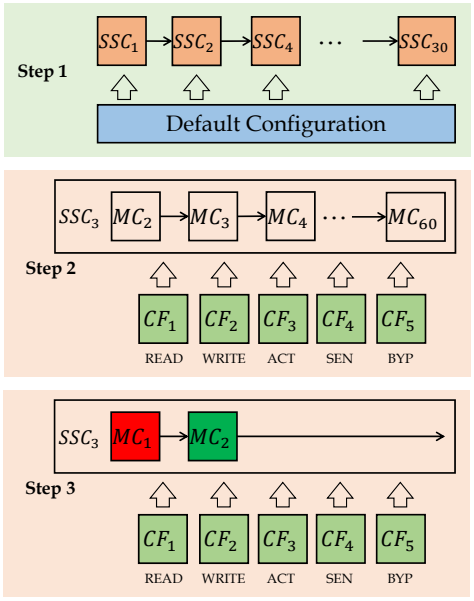


Fig. 10. An illustrative example for the fault-recovery control flow.

TABLE I
THE AREAS FOR DIFFERENT COMPONENTS IN AN MC.

Component	Area (μm^2)	Component	Area (μm^2)
T1	15	T2	15
T3	4	T4	40
NAND/NOR	100	MUX2	200
INV	70	DFF	400
Sen. & Act. Cir.	814	Con. Wire	17.5
DFF	400	Byp. MUX	200
Act. MUX	$200 \times N_b$	Sen. MUX	$200 \times N_b$
Write MUX	$200 \times N_b$	Read MUX	$200 \times N_b$

Note: N_b is the number of backup for each MC.

Next, activation-pattern shift-in and sensing-result shift-out are performed.

Step 3: The faulty SSC_3 is still selected by the IJTAG network, but the configuration registers are used such that only MC_1 (which is faulty) and its backup (MC_2) is selected. Next, MC-activation and capacitance-sensing operations are performed correctly in MC_1 with the help of MC_2.

Note that for every single activation pattern in a bioassay, the MEDA biochip should go through these three steps until the completion of bioassay execution.

V. EXPERIMENTAL RESULTS

In this section, we first analyze the area and time overhead of the fault-recovery design. Next, we introduce two evaluation metrics and the simulation setup for the proposed fault-recovery design. Then, we evaluate the benefits of the fault-recovery multiplexer-based design and the IJTAG network. Finally, the optimization of two design parameters is presented.

A. Area and Time Overhead Analysis

According to [16], [23], major concerns for test-circuit insertion and IJTAG network design are area overhead and access-time overhead, respectively. In the case of the IJTAG network,

because we need to configure the SIB registers, additional clock cycles are needed, and the total access time is increased. However, in a MEDA biochip, these two concerns do not arise.

In MEDA, the total area under each MC is $50 \times 50 = 2500$ μm^2 [19]. Using an AMI 0.35 μm PDK [25], we obtain the areas for different standard cells (e.g., INV, MUX and DFF), and the areas corresponding to the components used in an MC are listed in Table I. The dimensions of the standard cells can be viewed and downloaded from [26].

We can see that the areas of T1, T2, T3 and T4 are different. T3 is an NMOS transistor used to connect the bottom plate to the ground, therefore the smallest possible size is used. However, T1 and T2 are used to charge the bottom plate to 3.3V in the capacitance-sensing process. In order to increase the resolution of capacitance sensing, T1 and T2 are intentionally stretched (the length is several times longer than usual) in fabricated MEDA chips to obtain a small capacitor-charing current [27]. Finally, T4 is an NMOS transistor that need to endure a voltage of up to 17 V when the MC is activated [18], therefore it specially designed, and its area is much larger than a minimum-size NMOS.

Referring back to Fig. 1(a), when the MC-activation operation or capacitance-sensing operation is performed, transistors T1, T2, T3, T4, two MUXs (connected to N2 and N5), one NAND gate, one NOR gate, and two inverters are used; the total area for the activation circuit adds up to 814 μm^2. Because the activation and the sensing circuits share the same set of hardware, we combine these two functional blocks into one (i.e., Sen. & Act. Cir.) in Table I. It also indicates that the activation circuit and the sensing circuit will be either fault-free or faulty at the same time.

According to [25], the minimum trace width is 0.7 μm. Suppose the interconnect between two neighboring MCs is 25 μm (i.e., 1/2 of the MC width). The area of the interconnect wire (denoted as Con. Wire) is 17.5 μm^2. In addition, the area of a bypass mux is 200 μm^2, and the area of the another fault-recovery multiplexers is $200 \times N_b$ μm^2, where N_b is the number of backup MCs for each MC.

As shown in Fig. 7, each MC needs a set of one bypass mux and four fault-recovery muxes, and the area overhead is $(200 + 4 \times 200 \times N_b)$ μm^2. The area of the original circuit (see Fig. 1(a)) in an MC adds up to 1414 μm^2, and an area of $2500 - 1414 = 1086$ μm^2 can be used for fault-recovery circuit. When $N_b = 1$, the fault-recovery multiplexers can fit in the remaining area. However, if $N_b \geq 2$, there is not enough available area for the full set of fault-recovery multiplexers, and some of them have to be place at the peripheral area of the biochip. Nevertheless, in Section V.E, we find that $N_b = 1$ is the optimum value of N_b, therefore area overhead is not a concern.

In an IJTAG network, extra clock cycles (a.k.a retargeting time) to configure the SIB registers are needed. However, because the clock signal in MEDA has a frequency of 1 MHz, the time to shift in activation patterns (1800 bits) and shift out sensing results (1800 bits) is only 3.6 ms, and this data-shift process is needed only once per second. Therefore, access-time overhead is also not a concern, and sufficient time is available for fault recovery.

B. Evaluation Metrics

Therefore, rather than focusing on area overhead and access-time overhead, we introduce two metrics that can be used to evaluate the effectiveness of fault-recovery design, namely *fault-recovery rate* (FR) and *normalized data-shift* (DS).

The first evaluation metric FR is defined as follows:

$$FR = \frac{N_{ar} + N_{sr}}{N_{af} + N_{sf}} \tag{1}$$

The major functionalities of an MC include MC activation and capacitance sensing. If a fault occurs either in the activation circuit or in the DFF, we refer to this situation as an MC-activation fault. On the other hand, if a fault occurs either in the sensing circuit or in the DFF, this situation is referred to as a capacitance-sensing fault. Referring back to Equation (1), N_{af} and N_{sf} indicate the number of MCs that have MC-activation fault and capacitance-sensing fault, respectively. In addition, N_{ar} and N_{sr} represent the number of MCs that can recover from MC-activation fault and capacitance-sensing fault, respectively. The FR metric can be used to evaluate the fault recoverability of the proposed design.

The second evaluation metric DS is defined as follows:

$$DS = \frac{N_s}{3600} \tag{2}$$

where N_s is the number of bits shifted per second in the fault-recovery design, and "3600" represents 3600 bits are shifted are shifted in the scan chain per second in the original MEDA design (1800 bits for activation pattern and 1800 bits for capacitance-sensing results). The value of N_s can be approximately calculated as follows:

$$\begin{aligned} N_s \approx\ & 3600 + (1 + N_{fs}) \times N_s \\ & + \sum_{N_{fs}}^{i} N_{fm}(i) \times (4 \times \log_2(N_b) + 2) \end{aligned} \tag{3}$$

where N_{fs} is the number of faulty SSCs, N_s is the total number of SSCs, $N_{fm}(i)$ is the number of faulty MCs that can be recovered in the ith SSC, and N_b is the number of backup MCs for each MC.

The evaluation metric DS is important, because a higher value of DS indicates higher power consumption in MEDA, which is likely to heat up the biochip, and adversely impact the execution of temperature-sensitive bioassays. In addition, a higher value of DS also indicates more frequent use of DFFs, which is likely to reduce hardware reliability and lead to performance degradation.

C. Fault Simulation Setup

In this subsection, we first describe how to inject faults in an MC, and then describe how to determine whether a faulty MC can be recovered.

In order to evaluate the proposed fault-recovery design, we randomly inject multiple faults into the MEDA biochip, then we count the total number of faulty MCs, and also the numbers of faulty MCs that can be recovered from the injected faults. As a result, we can compute the two evaluation metrics (FR and DS) based on Equation (1) and Equation (2). To make the

TABLE II
THE CRITERIA TO DETERMINE THE TYPE OF FAULT FOR

Types of Faults	Act. Cir.	Sen. Cir.	DFF	Byp. Mux	Con. Wire	Act. Mux	Sen. Mux	W M
MC Activation	F		F	F-2		F-2 F-3		I I
Capacitance Sensing		F	F	F-2			F-2 F-3	
Broken Scan Chain				F-3	F			

Note: F indicate a failure in the functional block.

simulation more realistic, faults injected into the MC only the original circuit, but also the multiplexers us recovery.

In this paper, we assume that faults are injected in a spatially uniform manner. Therefore, the probability that a functional block has this fault is proportional to the area it occupies. As shown in Fig. 1(a), the transistors/gates for the circuit under each MC include transistors T1, T2, T3 and T4, three 2-input muxes, one DFF, one NAND gate, one NOR gate, and two inverters. For example, if we want to inject a fault into the original circuit, because the area of the DFF and the original circuit are 400 μm^2 and 1414 μm^2, the probability that the fault is injected into the DFF is $400/1414 = 0.282$.

When a fault is injected into a functional block in the original design, such as the activation circuit, sensing circuit or DFF, we assume that the functional block fails. However, when a fault is injected into one of the fault-recovery multiplexers, we assume the following three types of faults: (**F-1**) The multiplexer cannot select a component from a backup MC; (**F-2**) The multiplexer cannot select a component from a local MC (the MC where the multiplexer is located); (**F-3**) The multiplexer is faulty, and it cannot select any component. In the simulation, when a fault appears in a fault-recovery multiplexer, we randomly select a fault type from the three of them.

After faults are injected into the MCs in MEDA, we determine whether an MC has an MC-activation fault or a capacitance-sensing fault in order to compute the value of FR and DS. The criteria to determine the type of fault for an MC is listed in Table II. Note that if any one of the faults listed in the columns occurs, then an MC is deemed to have the corresponding fault. The third row in Table II (i.e., broken scan-chain fault) is a special case. If this fault occurs, an MC is deemed to have both an MC-activation and a capacitance-sensing faults, because the MC cannot be accessed in this case.

The method to determine whether an MC can be recovered from these two faults is simple. For an MC with an MC-activation fault, if both a fault-free activation circuit and a fault-free DFF can be selected from its own or from its backup MCs, this MC is able to recover from an MC-activation fault. Otherwise, recovery is not possible. A similar procedure can be used for an MC with a capacitance-sensing fault.

D. Benefits of the Proposed Design

In this subsection, we quantify the benefits introduced by the fault-recovery design and the IJTAG network. In order to do that, we compare the following three designs:

D-1: The fault-recovery design presented in [19]. In this design, three redundant DFFs are added to each MC, and it can recover only from faulty DFFs.

D-2: The proposed fault-recovery design with one backup MC for each MC, but without the IJTAG network.

D-3: The proposed fault-recovery design with one backup MC for each MC, and with an IJTAG network. The complete MEDA scan chain is divided into 60 SSCs.

Two simulations are needed to quantify the benefits — In the first simulation (Sim-1), no fault is injected in the connection wire, and no F-3 fault is injected into the bypass mux, so that broken scan-chain fault will not occur in MEDA. In this simulation, we compare the average FRs of D-1 and D-2 to see the benefit introduced by the fault-recovery design. In the second simulation (Sim-2), faults can be freely injected into any functional blocks. In this simulation, we compare the average FRs of D-2 and D-3 to see the benefit introduced by the IJTAG network.

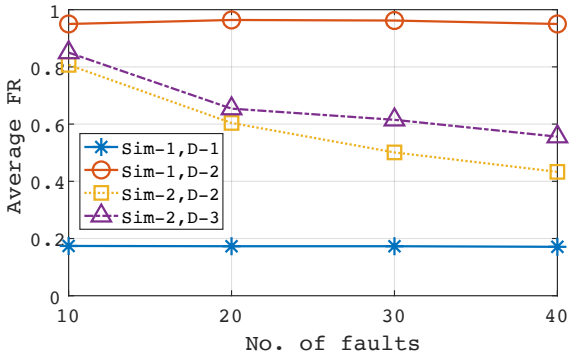


Fig. 11. The average FRs for D-1, D-2 and D-3 in the two simulations.

The simulation results are shown in Fig. 11. We can see that when no broken scan-chain fault occurs (Sim-1), D-2 achieves an FR value as high as 0.95, while the FR value for D-1 is less than 0.2. This indicates that the proposed fault-recovery design can enable recovery from most of the injected faults; however, it is not possible for D-1 because it can enable recovery only from faulty DFFs. In the second simulation (Sim-2), because of broken scan-chain fault, the FR value is lower than that of Sim-1, D-2. However, because of the IJTAG network, when a broken scan-chain fault occurs, we only need to bypass the faulty SSCs, and can still access the remaining SSCs. In this case, D-3 achieve a higher FR value than D-2 because of the use of the IJTAG network.

E. Design Optimization

In this subsection, we optimize two design parameters in the fault-recovery design, namely the number of SSCs (N_s) and the number of backups for each MC (N_b). First, we increase the number of SSCs from 50 to 200, and set the number of backup MC for each MC to 1. Changes in the number of SSCs will not affect the functionalities in the MEDA biochip. Then, we obtain the simulation results as shown in Fig. 12. We can see that a curve with a higher N_s obtains a higher average FR because with a shorter SSC, fewer MCs will be affected by a broken scan-chain fault. However, an increase in the number of SSCs also implies that more SIB registers are needed. In order

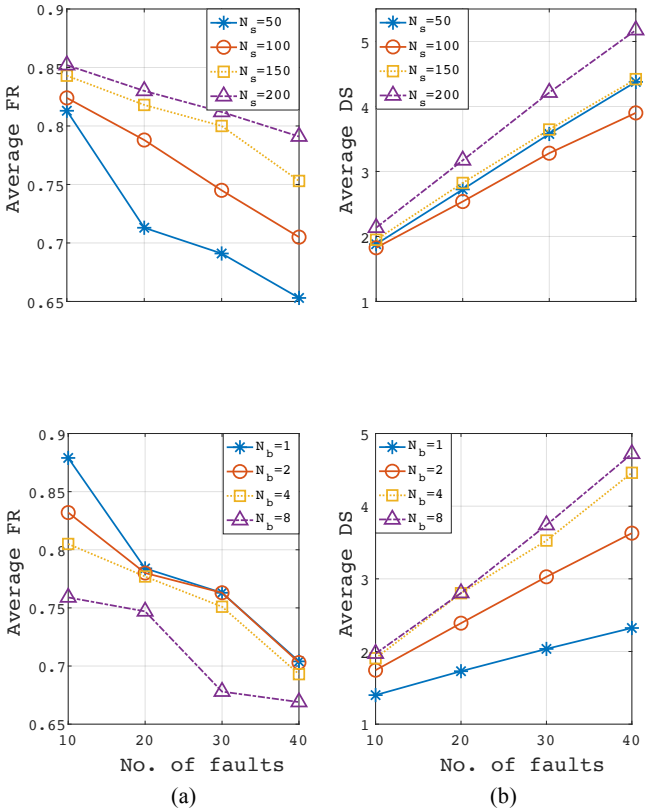


Fig. 13. The FR and DS values for different number of backup MCs.

to configure these SIBs, we need to shift in more configuration bits; this overhead is referred to as the *retargeting cost*. As a result, it will increase the value of DS. According to Fig. 12, the best choice for the number of SSCs is 150, because the curve with $N_s = 150$ achieves a relatively high value of FR (see Fig. 12(a)), and with a relatively low value of DS (see Fig. 12(b)).

Next, we increase the number of backups for each MC from 1 to 8, and set the number of SSCs to 150. Then, we obtain the simulation results shown in Fig. 13. We can see that when the number of backup MCs for each MC increases, the average FR decreases. The reason is that faults can also occur in the fault-recovery design. If more backup MCs are used, more inputs are needed for the multiplexer and thus the area increases as well. In this case, faults are more likely to appear in the fault-recovery design rather than in the original functional circuit. The values of DS also go up because more configuration bits are needed for multiplexers with more inputs. According to Fig. 13, one backup for each MC is a good choice because it achieves the highest value of FR and also the lowest value of DS.

VI. Conclusion

In this paper, we have presented an efficient fault-recovery solution for emerging MEDA biochips. Since the microelectrode cell (MCs) in a MEDA biochip are identical, we have added multiplexers for reconfigurability, such that an MC with faulty components can use the hardware resources in a neighboring MC. In addition, we use the IEEE 1687 (a.k.a. IJTAG) network to reduce the number of control signals needed for the multiplexers, and to provide flexible sub-scan chain access for the fault-recovery control flow. A comprehensive set of simulation results demonstrates the benefits of the proposed fault-recovery design and the IJTAG network. Finally, two design parameters have been optimized based on two evaluation metrics.

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