Cascaded H-Bridge MLI based Grid Connected Cell Level Battery Energy Storage System

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***Abstract*— This paper proposes a combination of cell-level energy processing and a Cascaded H-Bridge Multilevel Inverter (CHBMLI) for medium voltage, grid connected, battery energy storage systems. One isolated converter (Dual Active Bridge DC-DC Converter) manages each cell in the Battery Module, and the combination of Battery module and converter modules are cascaded to get the multi-level ac output voltage. The operating principle and control design of cell level isolated converter with double frequency ripple power, and the control strategy of the CHBMLI are presented. The performance of the battery cell level CHBMLI system with a 9-level inverter at small scale power level is validated through the simulations in MATLAB®/SIMULINK® software. The configuration holds promise for improving the performance and reliability of the battery modules at the cell level while also providing cell level galvanic isolation and high ac voltage.**

Keywords*— Battery cell level, energy storage system, dual active bridge dc-dc converter, cascaded H-bridge multi-level inverter.

I. INTRODUCTION

Nowadays, Battery Energy Storage Systems (BESS) play a significant role in integrating variable renewable energy sources, i.e., Solar Photovoltaic and Wind, and improving the stability of the grid [1] [2]. A Power Conditioning Unit (PCU) is required for the connection of BESS to the medium voltage (MV) grid and for controlling bi-directional power flow (i.e. discharging and charging). Multi-Level Inverter (MLI) based topologies, i.e., Diode clamped MLI and Flying Capacitor MLI [3] are suitable for the MV and high power application, and with input as the BESS. For these topologies, many battery modules need to be connected in series to get the high DC link voltage which compromises lifetime, efficiency and safety. A Battery Module (BM) is a series and parallel connected array of battery cells to get the required power/current and voltage ratings. Cells in the BM suffers from a various manufacturing defect, aging, and alter the internal impedance which eventually causes issues including lower reliability, low efficiency, and reduced lifetime [7]. The Cascaded H-Bridge MLI topology for the BESS [4][5][6], in contrast, offers modularity, redundancy, lower filter requirement and the connection of battery modules (different technologies can be used) in a distributed manner. This paper proposes to mitigate the aforementioned issues of BM by using the distributed power processing based Power Electronic converter technique at the cell level [8], by connecting one isolated converter across each cell of BM. A state-of-the-art battery module integrated energy storage system DC-DC converter has been presented in [9] where a non-isolated converter (DC/DC) is connected across each battery cell. A Cascaded H-Bridge Multilevel Inverter based grid connected Battery Cell level Energy Storage System (CHBMLI-BCESS) is proposed in this paper to overcome the drawbacks associated with battery module based CHBMLI. The main features of the CHBMLI-BCESS system are: galvanic isolation at the battery cell level, monitoring the SOC and Temp of the cell, and potential improvement in the efficiency and reliability of the system. Double frequency component (i.e. twice the ac fundamental frequency) is incurred across the dc capacitor voltage in the CHBMLI [10], and it is reflected on each of the voltage across the cell level. This issue is considered in the design of the cell level isolated converter.

The rest of the paper is organized as follows: proposed system description of Cascaded H-Bridge Multi-Level Inverter based Battery Cell level Energy Storage system is explained in Section II. The control strategies of battery cell level galvanic isolated converter and cascaded H-Bridge MLI are explained in Section III, whereas in Section IV the simulation validations of proposed system with 9-level MLI are provided. Conclusions are provided in Section V.

II. CASCADED H-BRIDGE MLI BASED CELL LEVELBATTERY ENERGY STORAGE SYSTEM

This section describes the operating principle of Cascaded H-Bridge MLI based Battery Cell level Energy Storage System and Battery cell Level isolated Converter.

A. CHBMLI-BESS

Fig. 1 shows the proposed system configuration of CHBMLI based BESS. The CHB-MLI includes *n*-series connected Converter Modules (H-Bridges), *CM1-a*, *CM2-a,…*, *CMn-a* and *n* Battery Modules in a distributed manner, *BM1-a*, *BM2-a,…*, *BMn-a* as input to the individual converter modules. An LC filter is used to interface between CHBMLI to the MV grid and filter the high switching frequency components in the current waveform. The Phase-a output voltage equation of CHBMLI [[5]] is as follows:

$$v_{ao} = \sum_{i=1}^{n} v_{ai} = \sum_{i=1}^{n} SF_{ia} V_{BMi-a} \tag{1}$$

where v_{ai} is the output voltage of i^{th} CM, SF_{ia} is the switching function of i^{th} CM with discrete values 0, ±1. V_{BMi-a} is the i^{th} Battery Module voltage. The CHBMLI is controlled by using the Phase Shift unipolar PWM (PS-PWM) technique, and the switching frequency of CM is f_s. The frequency of the v_{ai} is $2f_s$, and the equivalent frequency of v_{ao} is $2nfs$. The resultant voltage waveform of v_{ao} is an *n*-level waveform, and thus significantly improves the Total Harmonic Distortion (THD) of the grid current and reduce the footprint of the filter.

B. Cell Level Isolated Converter

The bi-directional DC/DC converter is used in place of the cell of BM to improve the lifetime and efficiency. Dual Active Bridge Converter (DABC) is chosen for the DC/DC converter integration of battery cell level and is called Cell Level Isolated Converter (CLIC), and the typical diagram is shown in Fig. 1 (d). The circuit diagram of pq^{th} CLIC is shown in Fig. 1(d), and it consists of primary and secondary H-bridges, and a high-frequency transformer (HFT). Based on the turns ratio

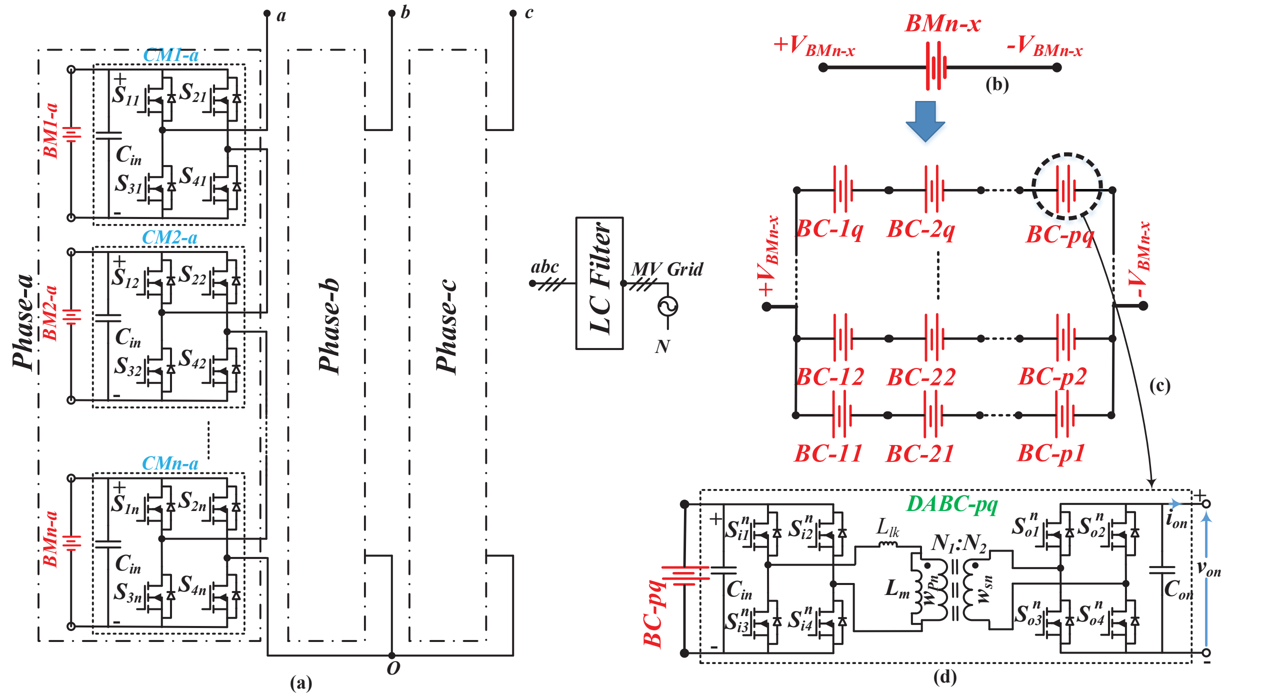

Fig. 1. (a) Cascaded H-Bridge MLI based Distributed Battery Module Energy Storage System; (b) Battery Module; (c) Cell Level Battery Module; (d) DAB based Cell Level isolated converter.

(N_1:N_2) of the HFT, the output voltage of the n^{th} CLIC is designed higher than the nominal voltage of the battery cell (>3.3V). Due to the symmetry property of the DABC, it is capable of control of bidirectional power flow by regulating the phase-shift between the primary and secondary H-bridges, called Phase Shift Modulation (PSM) technique. The main feature of the CLIC is the zero-voltage switching (ZVS) and providing path through the drain-source capacitance of power switch and leakage inductance of HFT. Double frequency ripple voltage component is exists across the CLIC due to the operation of CHB-MLI, and is taken into account for the design of CLIC output capacitance (i.e. C_{on} = 20mF) to limit the CLIC output voltage ripple to 2%. This will affect the voltage control design because the plant transfer function of CLIC depends on the value of the output capacitance and corresponding control design approach is in next section.

III. Control Strategy of CLIC

The control strategy of CHBMLI-CBESS is divided into parts: (a) Power Control between the BESS and MV grid [Fig. 2 (a)]; (b) voltage regulation of each CLIC [Fig. 3 (a)]. The power control strategy is implemented in abc reference frame and the unit grid voltage template is obtained by using Phase Locked Loop (PLL). This control generates the modulation index and then applied the PS-PWM to generate the switching gate pulses to the switches of module converters (i.e. CHB-MLI). The bode plots of current controller with unity gain controller and PI controller are shown in Fig. 2(b), and control design specifications are: Phase margin (P.M.) =70.4° and Gain cross over frequency (ω_{gc}) = 4.28×10^{3}rad/sec. By using the phase shift modulation (PSM) strategy, the output voltage of CLIC is regulating to its voltage reference ($V_{o_{ref}}$) value under load power variations during the charging/discharging process. The classical frequency domain approach is used to design the output voltage control of CLIC and Bode plots of voltage control loop with unity gain controller for the different output capacitance of CLIC, i.e. 200µF and 20mF are shown in Fig. 3 (b). It observes that drastically effects the Gain Margin and Phase Margin for the variation of C_{on}. The control design specifications of the voltage controller with 20mF are: P.M. = 82.8°, ω_{gc} = 71.7rad/sec and the Bode plot is shown in Fig. 3 (b). SOC (State Of Charge) balance of all battery cells in phase-a,b,c can be done by adding the charge control loop [11] to the primary voltage control loop of CLIC and is shown in Fig. 3(a), and improves the lifetime of the BESS. SOC_{pq_avg} is the global reference value to the charge balance control of each CLIC.

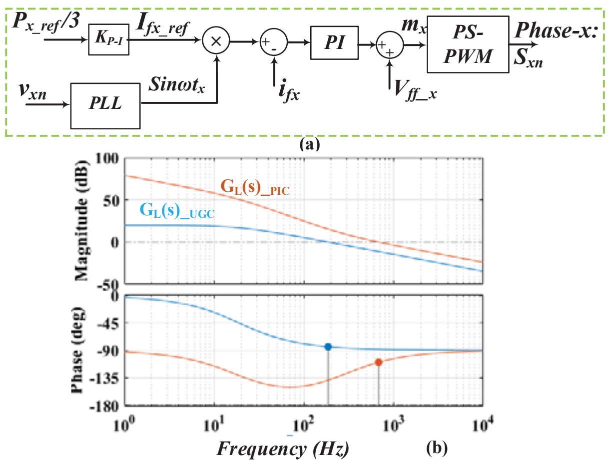

Fig. 2. (a) Power control strategy of CHB-MLI and 'x' refers to a, b, c; (b) Bode plots of current control of CHB-MLI with unity gain controller and PI controller.

IV. Validations of CHBMLI-CBESS

A. Simulation validations

The performance of the CHBMLI-CBESS and distributed control strategy of each CLIC are validated in MATLAB/SIMULINK. A CHB-9 level based CBESS using four CLIC of each Battery Module and four Converter modules are considered per phase of the MV 3-phase application and is simulated at a low power level for dynamic power changes during discharging process.

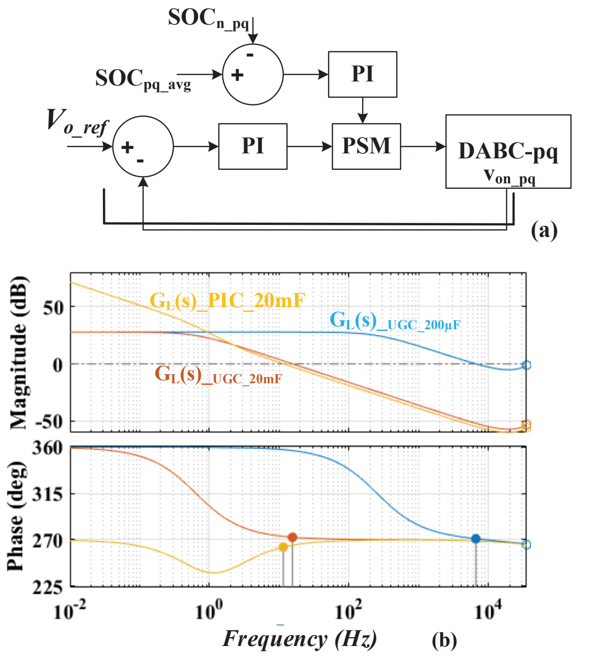

Fig. 3. (a) voltage control block diagram of Cell Level converter; (c) Bode plots of CLIC output voltage with unit gain controller with 200µF, 20mFand PI controller, $G_L(s)_{\_PIC\_20mF}$ with 20mF.

The battery cell level converter is operating in continuous conduction mode (CCM), and the switching frequency, f_s is 50 kHz. The electrical simulation parameters of CHB-MLI and CLIC are given in Table I.

Table-I: System specifications

S.No.	Cell Level Isolated Converter	
	Parameter	***Specifications***
1.	Battery cell (Li-ion technology)	Nominal voltage, V_{nom}: 3.3 V, Rated Capacity: 2.3AH,
2.	Leakage inductance, L_{lk}	3.1μH
3.	Switching frequency, f_s	50kHz
4.	Capacitors, C_{in} and C_{on}	220 µF and 20mF
5.	Kp and Ki	0.7265 and 9.524
	CHB-MLI	
6.	Switching frequency	10kHz
7.	Filter Inductor, L_f	0.85mH
8.	Converter Modules per phase	4
9.	Kp and Ki	3.393 and 5610
10.	AC grid voltage	110Vrms, 50Hz

The system is operating at its power rating of 100W during t<0.25sec and at t=0.25sec power reference decreased to 60% of rated power. Fig. 4 (a) shows the 9-level voltage waveform across cascaded converter modules, and grid voltages and filter inductor current waveforms are shown in Fig. 4(b). Fig. 5. (a) and (b) shows the CLIC input voltage, current, and output voltage waveforms. It is observed that these waveforms consisting of a double frequency ripple component with less than 2% of output voltage and able to regulate the voltage to its reference value (i.e. V_{o_ref} = 10V) and the settling time of 0.22sec under the changes in the load power.

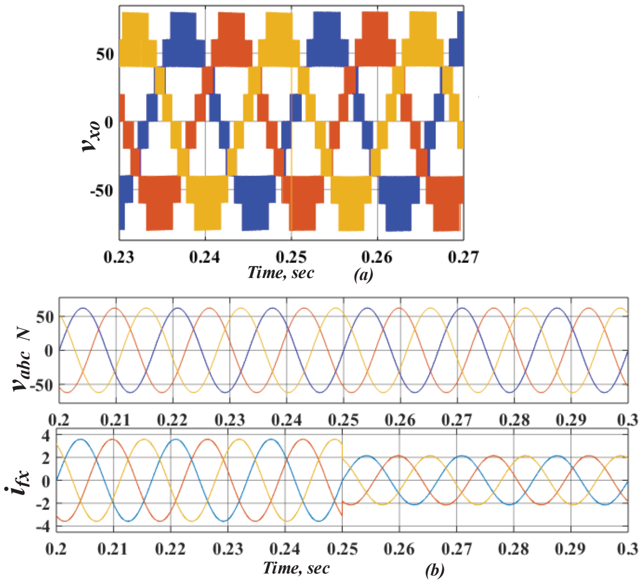

Fig. 4. Simulation results of CHBMLI under the dynamic power variations: (a) Output voltage of cascading of converter modules; (b) Grid voltages and filter inductor current waveforms.

Table-II: Hardware setup specifications

S.No.	Cell Level Isolated Converter	
	Parameter	***Specifications***
1.	Li-ion battery cell	3.6V, 2500mAH
2.	Primary bridge: GaN Mosfet devices	EPC2040
3.	Secondary bridge: GaN Mosfet devices	EPC2014
4.	HFT ferrite core: turns ratio	0.19:1
5.	Leakage inductance, L_{lk}	4μH
6.	Switching frequency, f_s	0.1MHz
7.	Capacitors, C_{in} and C_{on}	220 µF and 20mF
8.	DSP controller	TMS320F28377S Launchpad

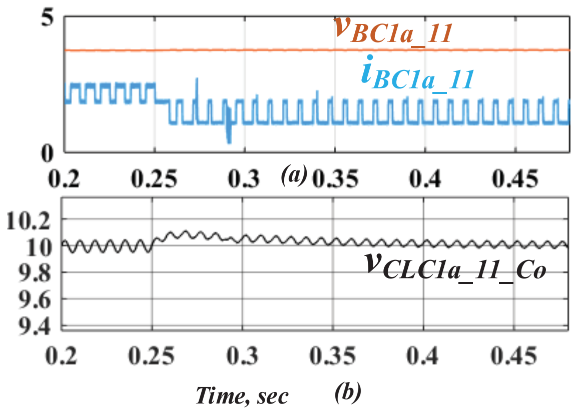

Fig. 5. (a) Simulations results of battery cell (BC1a_11) voltage current waveforms under a change in power conditions; (b) CLC output voltage waveform.

B. Preliminary Hardware experiments

A 7.5W Cell Level isolated Converter (i.e. dual active bridge converter) is selected to verify the performance of CHB-MLI system. The list of components of CLIC are given in Table-II. The lab prototype of GaN based CLIC is shown in Fig. 6 (a). The gate pulses to the primary and secondary active bridge of CLIC are shown in Fig. 6 (b). The voltage across secondary winding HFT of CLIC is shown in Fig. 6 (c).

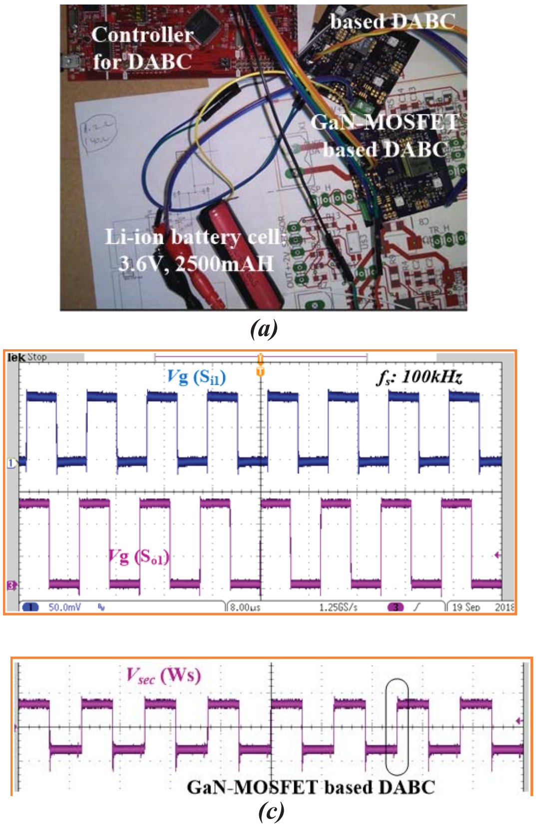

Fig. 6. (a) Lab prototype of GaN based CLIC; (b) Switching pulses to the H-bridges of CLIC (2V/div); (c) secondary voltage waveform of HFT in CLIC (10V/div).

V. CONCLUSIONS

In this paper, a Cascaded H-Bridge Multilevel Inverter based grid connected battery cell level energy storage system has been proposed for the medium voltage distributed grid applications. The system improves the performance of the Battery Modules/submodules at cell level through CHBMLI topology. The control design of the DAB based cell level isolated converter is presented with double frequency active power ripple. The system is considered with a 9-level inverter (4-converter modules) and 2x2 configuration of DAB based Cell level isolated converter per each battery module and validated through SIMULINK software. The lab prototype of GaN based cell level isolated converter is developed, and the implementation of CHBMLI is underway. The hardware experimental results and Hierarchical SOC balance control scheme will be presented in the future.

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