Silicon Degradation in Monolithic II–VI/Si Tandem Solar Cells

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***Abstract*—II–VI/Si tandem solar cells have strong potential for high efficiency at low cost by combining the two most widely used solar cell materials: silicon and cadmium telluride (CdTe). However, there are challenges with this merger, as loss of minority-carrier lifetime in the silicon bottom cell can be caused by growth of a II–VI cell on top. Silicon lifetime degradation in monolithic II–VI/Si structures is measured here on experimental samples for CdTe deposition temperatures between 400 and 500 °C, with variable In_2O_3:ZnO (IZO) thickness between the CdTe and silicon, and with and without $CdCl_2$ postdeposition treatment. Results indicate that the $CdCl_2$ treatment has the strongest effect on silicon lifetime reduction, followed by temperature and IZO thickness. Potential causes are discussed, and the effect on monolithic II–VI/Si two-junction solar cells is modeled. Remarkably, many silicon samples in the study were able to maintain >400 μs lifetimes, with some exceeding 1 ms, consistent with >30% projected efficiency in fully integrated II–VI/Si tandem solar cells.**

***Index Terms*—Cadmium telluride (CdTe), indium zinc oxide (IZO), lifetime degradation, silicon, tandem.**

I. Introduction

INCORPORATING the two most widely used solar cell materials, CdTe and silicon, in II–VI/Si tandem cells has the potential to achieve high energy conversion efficiency and low cost simultaneously. Two designs of monolithic, two-junction II–VI/Si tandem solar cells are shown schematically in Fig. 1, each with a MgCdTe top cell, having a modest fraction of Mg to increase the CdTe bandgap, and silicon bottom cell. Champion thin-film CdTe cells have reached 22.1% efficiency, while record silicon cells have reached 26.7% [1]. As single-junction solar cells move closer to their detailed-balance theoretical limit [2], there has been strong interest in low-cost tandem (two-junction) cells with a higher theoretical efficiency ceiling. Silicon is an attractive choice for the bottom cell in tandems because of its bandgap of 1.12 eV, low cost, high efficiency, and well-established industry infrastructure.

Manuscript received October 18, 2019; accepted December 2, 2019. Date of publication January 10, 2020; date of current version February 19, 2020. This work was supported by the National Science Foundation, Division of Electrical, Communications and Cyber Systems, EAGER Awards #1665299 and #1665508. *(Corresponding author: Kevin D. Tyler.)*

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Digital Object Identifier 10.1109/JPHOTOV.2019.2961607

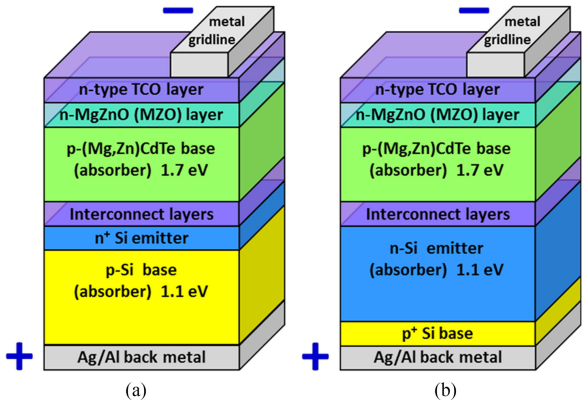

Fig. 1. Schematics of MgCdTe/Si tandem solar cells with (a) thin n^+ emitter and thick p-type base, and (b) thick n-type emitter and thin p^+ base in the silicon bottom cell.

Lifetime degradation in silicon has been seen by groups depositing III–V materials on Si, but less has been reported on the effect of II–VI deposition on silicon lifetime. For III–V growth on silicon, the effect of PH_3 exposure on Si surface morphology was studied, and Si lifetime was found to degrade by two orders of magnitude (from 432 to 6 μs) during growth of the first III–V GaP layer on the Si surface [3]–[5]. The drop in silicon lifetime after III–V growth has been attributed to unintentional fast-diffusing impurities in metal–organic chemical vapor deposition [6] and molecular beam epitaxy systems [7]. Several groups have found that a silicon nitride layer on the back can block impurity diffusion into the silicon substrate [7]–[10], and that long minority-carrier lifetimes in the silicon base can be recovered by gettering [6], [8], [9], for example, by a heavily doped n^+ diffused layer. Low temperature passivation methods can also help to mitigate lifetime degradation in Si [11].

While several potential solutions have been developed, the cause of silicon lifetime degradation during III–V growth across different III–V deposition systems is not yet fully understood. However, it seems likely that lifetime degradation in silicon will also occur in II–VI/Si solar cells. Here, the loss of silicon lifetime in II–VI/Si test structures is characterized and analyzed to predict its effect on II–VI/Si tandem cell performance.

II. Modeling

To determine trends in II–VI/Si tandem cell performance and establish threshold Si bulk lifetime values that give substantially

higher tandem cell efficiency than for Si cells alone, monolithic, two-terminal 1.72-eV MgCdTe/Si tandem cell efficiencies are modeled as a function of Si bottom cell bulk lifetime at 25 °C. Calculations were made using closed-form equations from Hovel [12] for the diode saturation current density J_o and short-circuit current density $J_{\rm sc}$ of the silicon cell, as functions of absorber layer bulk lifetime. The *J–V* curves of both the II–VI top cell and the Si bottom cell were combined point-by-point at the same current density *J* to model series-interconnected tandem cells.

Several different Si bottom cell architectures are considered for modeling, each with one thick layer and one thin layer that form the p–n junction. Both photogeneration and bulk recombination are strongest in the thick layer, referred to as the absorber. Fig. 1 shows schematic diagrams of two example II–VI/Si two-junction cell structures. In Fig. 1(a), the Si cell has a thin n^+ emitter on a thick p-type base (absorber), while Fig. 1(b) shows a configuration with a thick n-type emitter (absorber) on a thin p^+ base. Both of these are n-on-p configurations, with the same polarity as the II–VI top cell facilitating series interconnection. Note that the thick n-type emitter case in Fig. 1(b) has the p–n junction at the back of the cell, increasing sensitivity to minority-carrier diffusion length and lifetime in this configuration. In addition to these designs, three-terminal cells with top and bottom cells of opposite polarity, three-terminal cells with interdigitated, alternating + and – polarity contacts on the back of the Si substrate, and four-terminal configurations of II–VI/Si cells are possible.

In Fig. 1 and in each of the II–VI/Si cells modeled, a stack of optically transparent and electrically conductive interconnection layers (interlayers) is deposited on the emitter (on the sunward surface) of the Si cell, to connect top and bottom cells. Since the interface recombination velocity that can be achieved between the top surface of the Si emitter and the interlayers that connect top and bottom cells is still unknown, low (passivated emitter) and high (unpassivated emitter) bracketing values are modeled. The polycrystalline 1.72-eV p-type II–VI top cell base (MgCdTe is shown) is grown in a nonconventional substrate configuration, i.e., with the sunward surface grown last, followed by an n-type MgZnO window (heteroemitter) layer, transparent conductive oxide, and metal gridlines on the front.

The dependence of the calculated tandem cell efficiency on bulk lifetime in the Si bottom cell absorber is plotted in Fig. 2, for four cases of Si bottom cell structures.

1) An n^+ emitter on top of a thick p-type Si base (absorber) [see Fig. 1(a)], with emitter top surface recombination velocity (SRV) $s_{\rm emit}$ of 10 cm/s (passivated).
2) A thick n-type Si emitter (absorber) on top of a thin p-type base [see Fig. 1(b)], with $s_{\rm emit}$ of 10 cm/s (passivated).
3) A p^+ emitter on top of a thick n-type Si base (absorber), with $s_{\rm emit} = 10$ cm/s (passivated).
4) The same n+/p structure of Case 1 but with $s_{\rm emit} = 10^5$ cm/s (unpassivated).

The effective back SRV is assumed to be 10 cm/s in each case. In Case 3 alone, the Si cell has the opposite polarity as the top cell, requiring the interlayers to have high lateral conductance to act as a third terminal.

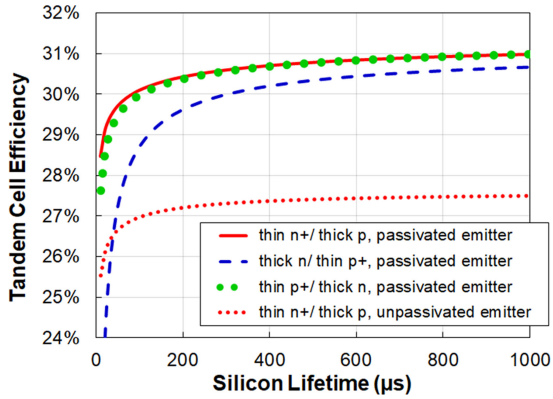

Fig. 2. Modeled II–VI/Si two-junction cell efficiency (AM1.5G, 0.100 W/cm^2, 25 °C), for four different Si bottom cell configurations: 1) p-type absorber (thick base); 2) n-type absorber (thick emitter); 3) n-type absorber (thick base); and 4) p-type absorber (thick base, with unpassivated emitter).

The cumulative photogenerated current density in the 1-sun (0.100 W/cm^2) ASTM G173-03 AM1.5G standard solar spectrum available to the top and bottom cells is determined by light absorption resulting in electron–hole pair generation and light trapping in the cell layers, and undesirable reflectance and absorptance at the front surface and in the interlayers. In this modeling, the cumulative photogenerated current density available from the combination of these effects is taken to be 90% of the photon flux above the 1.12-eV silicon bandgap, times the electronic charge q, or 39.5 mA/cm^2. The short-circuit current density $J_{\rm sc}$ of the Si cell was calculated for each modeled value of Si absorber bulk lifetime using the equations from Hovel [12] as noted above. The thickness and transmittance of the MgCdTe top cell and interlayers are taken to be adjustable in the tandem cell growth process, so that the collected short-circuit current density $J_{\rm sc}$ is equal in both top and bottom subcells, for example, varying from 19.7 to 19.6 mA/cm^2 for Si bulk lifetimes of 2 ms and 50 μs, respectively, for Case 1 with a thick p-type absorber and a passivated emitter. The doping profiles are taken to be constant within each layer of the Si cell for simplicity. In practice, the emitter could be formed by dopant diffusion in Si prior to interlayer and II–VI deposition. The diode saturation current density J_o of the 1.72-eV MgCdTe top cell is taken to be 6.0×10^{-21} A/cm^2, which gives a bandgap-voltage offset $W_{\rm oc} \equiv (E_g/q)$–$V_{\rm oc}$ of 0.600 V, similar to that of high-performing polycrystalline CdTe cells [1]. The J_o of the Si cell varies with the value of bulk lifetime that is modeled, for example, from 2.6×10^{-14} A/cm^2 at 2 ms bulk lifetime, to 3.3×10^{-13} A/cm^2 at a bulk lifetime of 50 μs, again for Case 1 with a thick p-type Si absorber and a passivated emitter. Diode ideality factors are taken to be unity.

As seen in Fig. 2, for the passivated emitter cases with $s_{\rm emit} =$ 10 cm/s and a thick base in the Si cell so that the p–n junction is toward the sunward surface, the modeled tandem cell efficiency is greater than 30.6% for absorber lifetime >400 μs, and over 30% for absorber lifetime >120 μs, for both the n^+/p and p^+/n Si cell structures. Even for the thick n-type emitter case with the p-n junction at the back of the cell, the modeled tandem efficiency is over 30% for >400 μs absorber lifetime.

III. Experimental Method

To measure the effect of II–VI semiconductor deposition on minority-carrier lifetime in silicon, CdTe was deposited on Si substrates by close-spaced sublimation (CSS) in much the same way that MgCdTe or ZnCdTe is envisioned to be deposited on active Si solar cells to form II–VI/Si tandem cells. CdTe was used rather than 1.7-eV MgCdTe in this article for simplicity and to establish a baseline for II–VI materials. Similarly, experimental runs include the CSS $CdCl_2$ treatment that is vital to most II–VI solar cells [13], as well as the conductive and transparent interlayers used to connect the II–VI and Si cells, since these are features anticipated in the tandem cells. Varying thicknesses of indium zinc oxide (IZO, specifically 90% In_2O_3:10% ZnO) are used as the interlayers in this article.

Czochralski (CZ) n-type, (1 0 0) silicon wafers were used in these experiments, with typical doping of approximately 1×10^{16} cm^{-3}, because typical initial bulk lifetimes are ~2 ms in n-type compared with ~0.3 ms for p-type CZ wafers. The longer lifetime n-type Si wafers thus tend to be more sensitive to changes in recombination rate, while those changes may be masked in the lower lifetime p-type wafers. With reasonable assumptions, lifetime results in n-type may be extrapolated to p-type.

The experimental protocols, additional samples, and analyses used to minimize experimental variance in this lifetime study are described in [14]. Every full n-type silicon wafer in the study was cleaned in the same cassette holder at the same time, using piranha (3:1 H_2SO_4:H_2O_2), KOH, and 1:1:6 HCl:H_2O_2:H_2O (RCA-B) [15] solutions, with a 10 min deionized (DI) water rinse between each step. The KOH was a nontexturing solution, resulting in roughly planar Si surfaces. The chemical oxides on the Si surface were removed in 6:1 NH_4F:HF buffered oxide etch (BOE) for 5 min, before dc sputter deposition of 0 (none), 20, 40, or 60 nm of IZO.

CdTe was uniformly deposited on one side of the Si substrates by CSS at 40 mTorr in an N_2 ambient, at temperatures of 400, 450, and 500 °C, bracketing the typical CdTe deposition temperature of 480 °C. Approximately 2.5 μm of CdTe was sublimated onto the Si substrates with IZO coatings for 3 min in a first chamber. For the samples that were to have $CdCl_2$ treatment, a $CdCl_2$ layer was sublimated onto the Si samples for 3 min in a second chamber, which were then moved to a third chamber for annealing at 400 °C for another 3 min. Samples were rinsed with DI water to remove residual $CdCl_2$. The baseline process used for single-junction CdTe cells can be found in Swanson [16].

To prepare for lifetime testing, the CdTe and IZO layers were removed in a nitric-phosphoric acid etch (7:3:1 H_3PO_4:H_2O:HNO_3), followed by piranha and RCA-B cleans. The silicon sample surfaces were passivated with hydrogenated amorphous silicon (a-Si:H) to minimize surface recombination, increasing the sensitivity of the measured lifetime to bulk recombination. Surface oxides were removed in a BOE etch for 5 min, immediately before passivating both front and back Si surfaces with 50 nm of undoped a-Si:H deposited by plasma enhanced chemical vapor deposition at 250 °C for 40 s. Baseline control Si samples with no CdTe or $CdCl_2$ deposition also received this BOE etch immediately prior to a-Si:H passivation on both sides with the same conditions.

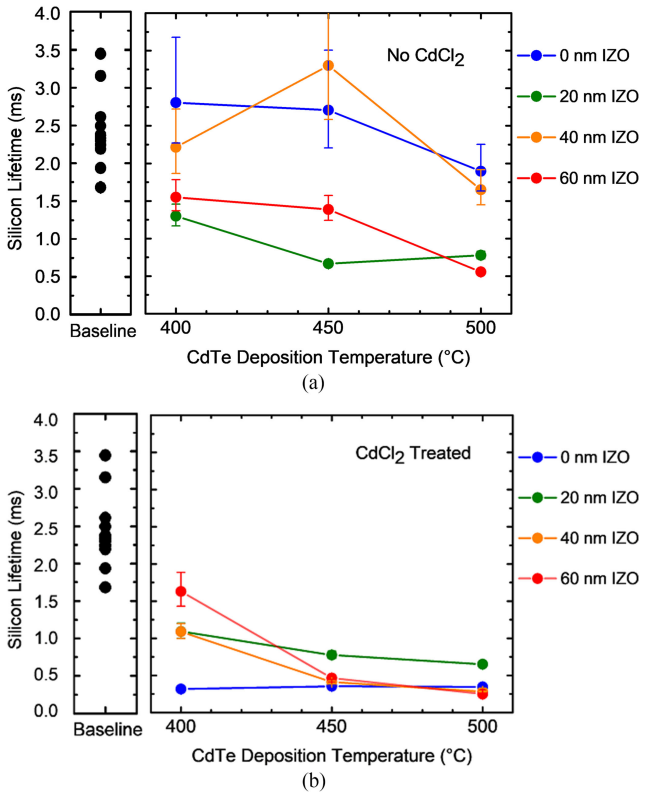

Fig. 3. Measured minority-carrier lifetime in experimental Si samples after CdTe deposition at 400, 450, and 500 °C, for samples with IZO thicknesses of 0 (no IZO), 20, 40, and 60 nm: (a) with no $CdCl_2$ treatment and (b) with $CdCl_2$ treatment. Lifetime measurements are also shown for baseline control samples with no CdTe or $CdCl_2$ exposure.

Secondary ion mass spectroscopy (SIMS) was conducted at Eurofins EAG Laboratories to detect whether suspected impurities were present in Si samples at large concentrations, using O_2^+ sputtering ions for a survey analysis of positive impurity ions, and Cs^+ sputtering ions for a survey of negative impurities.

IV. Results and Discussion

The minority-carrier lifetimes measured in silicon wafers after CdTe deposition at temperatures from 400 to 500 °C, IZO thicknesses between 0 and 60 nm, and for both the $CdCl_2$ treated and non-$CdCl_2$-treated cases are shown in Fig. 3. Measured lifetimes of baseline, control Si samples, taken from the same wafers as the experimental samples are also plotted in Fig. 3. These measurements show the initial level of recombination in the Si wafers, because of both surface and bulk recombination components, before CdTe and $CdCl_2$ exposure. If all recombination in these control samples is assumed to be in the bulk, these measurements provide a baseline for initial bulk lifetimes. Alternatively, if all recombination is assumed to be at the intrinsic a-Si:H passivated surface of these ~160-μm-thick samples, they show that this surface passivation method has an upper limit of SRV between 2 and 5 cm/s.

The variation in the baseline control Si samples gives a measure of the experimental uncertainty in 1) initial Si bulk recombination; 2) passivated SRV; and 3) reproducibility of the photoconductance decay (PCD) measurement itself. The physical parameter of interest is the recombination rate, proportional to the diode saturation current density J_o and to the inverse lifetime, $1/\tau$. We thus find the variation in $1/\tau$ for the control samples, and apply this to find the error bars in Fig. 3. The very low recombination rates in the control samples introduce low uncertainty for experimental samples with high recombination (short lifetime), but greater uncertainty for the experimental samples with low recombination (long lifetime). It should be noted that the error bars in Fig. 3 represent only the variation because of initial Si sample bulk lifetime, passivated SRV, and PCD measurement reproducibility as listed above, and not the experimental variation in the effect of the CdTe and $CdCl_2$ processes themselves on Si lifetime.

Fig. 3(a) shows the Si wafer lifetime after CdTe deposition, and before $CdCl_2$ treatment. This can be considered as a lower limit of the Si bulk lifetime, because the small SRV after a-Si:H passivation can only add to the overall measured recombination rate. Remarkably, before $CdCl_2$ treatment, all samples retained lifetimes above the 400 μs threshold identified in the cell modeling section as capable of supporting II–VI/Si tandem cell efficiencies above 30%. All of the Si samples retained lifetimes in excess of 1 ms at CdTe deposition temperature of 400 °C, and many were higher than 1 ms even at temperatures of 450 and 500 °C.

The strongest effect on the degradation of silicon lifetimes comes from the $CdCl_2$ treatment. While the non-$CdCl_2$ treated silicon samples were able to maintain lifetimes above 1 ms in most cases, only a few of the $CdCl_2$-treated samples retained lifetimes above 1 ms. Lifetimes averaged across all IZO thicknesses dropped from 2.0, 2.0, and 1.2 ms at 400, 450, and 500 °C CdTe deposition temperatures with no $CdCl_2$ treatment, respectively, to 1.0, 0.5, and 0.4 ms for these CdTe temperatures, with $CdCl_2$ treatment. While this is cause for concern, as the $CdCl_2$ is necessary for the passivation of polycrystalline CdTe [15], it is encouraging that any lifetimes above 1 ms were retained after $CdCl_2$ in this preliminary study. It is interesting to note that at 400 °C CdTe deposition temperature, all samples with a nonzero IZO interlayer thickness had lifetimes above 1 ms even after $CdCl_2$ treatment.

Si wafers subjected to higher CdTe deposition temperatures tended to have lower lifetimes on average. This effect is particularly evident after $CdCl_2$ treatment, when comparing samples with CdTe deposition temperature of 400 °C with higher deposition temperatures. For all samples with an IZO interlayer, the decrease in lifetime was monotonic with increasing CdTe temperature. Since the lifetime of IZO samples after $CdCl_2$ treatment depends on the CdTe deposition temperature prior to the $CdCl_2$ step, one possible explanation is that more impurities diffuse into the Si wafer at the higher CdTe deposition temperatures, but these are not activated or diffused deeply enough into the Si to see their full effect on lifetime degradation until after the $CdCl_2$ step. In this scenario, the presence of an IZO layer on the Si surface could extend the time it takes for impurities in the CdTe deposition step to reach the Si substrate, acting as a diffusion barrier. In contrast, for samples with no IZO interlayer, relatively low lifetimes were observed in the 310–360 μs range with little dependence on CdTe deposition temperature. All of the samples in the study were well above the calculated threshold of 120 μs to achieve >30% efficiency for tandem II–VI/Si cells with a passivated Si emitter and p-n junction toward the front of the Si substrate.

SIMS was used to do a survey scan for a wide range of impurity elements that could possibly have been introduced into the Si substrates. A sample that showed significant lifetime degradation was chosen, with 40-nm IZO, 500 °C CdTe temperature, and $CdCl_2$ processing, and the SIMS analysis was carried out to a depth of 1 μm. The elements K, Na, Li, Ca, Al, Cd, Mg, Ti, Zr, Mn, Cr, In, Fe, Ni, Cu, B, and Zn, which form positive ions, were measured using O^+ sputtering ions, and are listed in order of increasing detection limit from 10^{14} to 10^{17} cm^{-3}. Elements Au, As, F, S, Te, Cl, Br, C, Sb, Pt, P, Ge, O, and H, which form negative ions, were measured using Cs^+ sputtering ions, and are listed in order of increasing detection limit from 10^{16} to 10^{18} cm^{-3}. Cd, Te, and Zn especially are causes for concern since they are present in the CdTe and IZO device layers, and introduce energy levels deep in the Si bandgap. Cd was analyzed in a separate SIMS scan, in order to lower its detection limit to 2×10^{15} cm^{-3}. In spite of the broad range of elements surveyed, none of the above elements were detected in SIMS measurements of the Si wafer after CdTe + $CdCl_2$ processing at concentrations above their detection limit. It is likely that impurity concentrations below the detection threshold are able to cause the observed loss in Si minority-carrier lifetime, but it is unknown which specific impurities may be responsible.

The measured lifetimes in the Si samples can be used to calculate recombination rate and component of the diode saturation current density J_o that results from exposure to CdTe and $CdCl_2$. The recombination rate is proportional to the inverse lifetime $1/\tau$, and with the simplifying assumption of a uniform excess minority-carrier concentration across the thickness of the Si wafer, the J_o because of Si bulk recombination can be written

$$J_o = \frac{qw}{\tau}\frac{n_i^2}{N_{\rm dop}} \tag{1}$$

where w is the Si wafer thickness, τ is the Si bulk lifetime, $N_{\rm dop}$ is the n- or p-type doping level, and n_i is the Si intrinsic carrier concentration.

Diode saturation current density J_o values calculated from the measured Si lifetimes are plotted in Fig. 4, for samples both before and after CdTe + $CdCl_2$ treatment, and for all IZO thicknesses and CdTe deposition temperatures studied, using example values of $w = 100$ μm and $N_{\rm dop} = 10^{16}$ cm^{-3}. The measured lifetimes are assumed to be the bulk Si value, with negligible recombination compared with the bulk at the passivated sample surfaces. The samples before and after CdTe + $CdCl_2$ treatment in each column of Fig. 4 were taken from the same Si wafer. The upper (green) portion of each column is the change in J_o for each sample, and the total height of each column is the overall J_o of the sample including recombination in the initial, baseline

TABLE I
CALCULATION OF J_o, V_{oc}, AND TANDEM CELL EFFICIENCY η FROM MEASURED MINORITY-CARRIER LIFETIME AS DESCRIBED IN THE TEXT

Absorber doping type	Process		τ (μs)	$\frac{1}{\tau}$ (s^{-1})	J_o Si absorber recomb. only (fA cm^{-2})	V_{oc} Si absorber recomb. only (V)	η tandem cell, Si absorber recomb. only (%)	η tandem cell, all recomb. (%)
n-type absorber		**initial**	**2446**	**409**	**6.5**	**0.743**	**31.82**	**30.91**
(thick emitter)	450°C CdTe	**final**	**1382**	**724**	**11.6**	**0.728**	**31.49**	**30.78**
(measured PCD	no $CdCl_2$	Δ	-1064	315	5.0	-0.015	-0.33	-0.13
lifetime τ)	450°C CdTe	**final**	**461**	**2171**	**34.7**	**0.700**	**30.75**	**30.30**
	w. $CdCl_2$	Δ	-1986	1762	28.2	-0.043	-1.07	-0.61
estimated for:		**initial**	***~400***	***2500***	***40***	***0.696***	***30.96***	***30.71***
p-type absorber	450°C CdTe	**final**	***347***	***2880***	***46***	***0.692***	***30.89***	***30.65***
(thick base)	no $CdCl_2$	Δ	*-53*	*380*	*6*	*-0.004*	*-0.07*	*-0.06*
(projected from n-type	450°C CdTe	**final**	***216***	***4630***	***74***	***0.680***	***30.64***	***30.46***
data, using ~400 μs τ_{init})	w. $CdCl_2$	Δ	*-184*	*2130*	*34*	*-0.016*	*-0.32*	*-0.25*

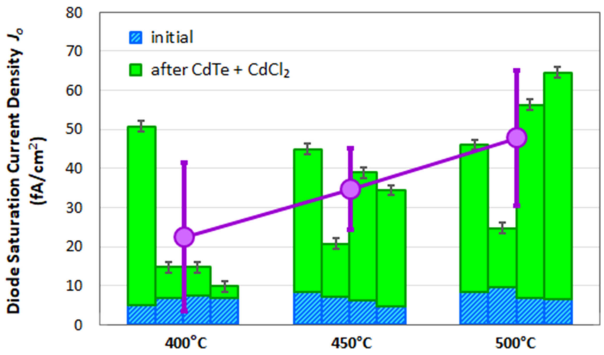

Fig. 4. J_o values calculated from measured lifetime τ in experimental Si samples with 0 (no IZO), 20, 40, and 60 nm IZO thicknesses, 400, 450, and 500 °C CdTe deposition temperatures, all treated with $CdCl_2$, as described in the text.

samples. The substantial increase in J_o because of the CdTe + $CdCl_2$ exposure is evident in Fig. 4.

The error bars on each column are calculated from the measured range of $1/\tau$ in the baseline control samples, as described earlier. Since trends in lifetime with IZO thickness are difficult to discern in these samples, the average J_o for all four IZO thicknesses is also plotted (purple) at each CdTe deposition temperature. The purple error bars on these average values represent both the scatter in data at each CdTe temperature, as well as the scatter in initial $1/\tau$ measured on the baseline control samples. Although the scatter in the data for different IZO thicknesses at each CdTe temperature is large, the J_o shows an increasing trend with higher CdTe deposition temperature.

Table I shows average values of measured minority-carrier lifetime and values of J_o, open-circuit voltage V_{oc}, and tandem cell efficiency η calculated from them, for Si samples before II–VI exposure (initial), after CdTe deposition, and after CdTe + $CdCl_2$ treatment. The change Δ before and after exposure is also tabulated. The V_{oc} for the Si cell due solely to the measured lifetime in the Si bulk can be calculated from the J_o and the photogenerated current density J_{ph}

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{J_{ph}}{J_o}\right) \tag{2}$$

and is shown in Table I. Tandem cell efficiencies based on the J_o found from measured Si sample lifetimes are also included in Table I, calculated using the methods described earlier: 1) for the measured Si absorber bulk recombination only; and 2) for measured Si absorber bulk recombination, plus the same emitter bulk, emitter front surface, and absorber back surface recombination components used in the modeling section. These results quantify the modest loss in Si cell V_{oc} and tandem cell efficiency because of the drop in Si absorber lifetime, and indicate that with well-passivated front and back surfaces in cells with an n-type Si absorber, the measured lifetimes in n-type Si wafers after II–VI growth on top are capable of supporting II–VI/Si tandem efficiencies above 30%.

In addition to parameters calculated from the measured lifetime in n-type Si absorbers, solar cell parameters are also calculated for cells with p-type absorbers using p-type absorber lifetimes predicted from the n-type data. For defect or impurity states that are not near the band edges, $1/\tau = N_t\, \sigma\, v_{th}$, where N_t is the density of defect or impurity states, σ is the capture cross section for minority carriers, and v_{th} is the thermal velocity of minority carriers. We expect the density of impurities diffusing into p-type wafers to be the same as in the measured n-type wafers; therefore, we expect p- and n-type lifetimes to be related according to

$$\frac{\tau_{e,p-type}}{\tau_{h,n-type}} = \frac{\sigma_h v_{th,h}}{\sigma_e v_{th,e}} \tag{3}$$

where e and h designate electrons and holes, respectively. In Table I, the lifetime degradation in p-type Si is estimated, based on the measured lifetime degradation in n-type Si, with the simplifying assumption of equal electron and hole capture cross sections, and literature values of $v_{th,h} = 1.68 \times 10^7$ cm/s and $v_{th,e} = 2.03 \times 10^7$ cm/s [17], These estimates indicate that greater than 30% efficiency can be supported in II–VI/Si tandem solar cells with a p-type Si absorber as well.

V. CONCLUSION

To investigate the integration of active Si cells in II–VI/Si tandem solar cells, we experimentally determined the

minority-carrier lifetime in n-type Si substrates after polycrystalline CdTe growth on Si. Lifetimes were measured for Si samples with 0–60 nm thick IZO interlayers simulating the layers that optically and electrically connect top and bottom cells in tandems, 400–500 °C CdTe deposition temperatures bracketing typical temperatures for CdTe growth, and both before and after the $CdCl_2$ treatment that is typically needed to achieve polycrystalline CdTe solar cells with high efficiency.

In spite of the presence of Cd, Te, Cu, and other impurities that can strongly degrade minority-carrier lifetime in the chambers used for CdTe cell fabrication—a setting far removed from the largely metal-free environment typically used for processing high-lifetime Si solar cells—lifetimes over 1 ms could be maintained under many conditions. At 400 °C CdTe deposition, Si lifetimes ranged from 1.3 to 2.8 ms with no $CdCl_2$ treatment. The $CdCl_2$ treatment had a pronounced effect on recombination, dropping the lifetime range to 0.3–1.6 ms at this same temperature of 400 °C. Higher temperatures also tended to increase recombination. The effect of increasing IZO thickness on lifetime was not monotonic, although the presence of IZO versus its absence may have conferred a protective effect in Si samples that had $CdCl_2$ treatment.

Measured lifetimes of samples with 450 °C CdTe deposition and with $CdCl_2$ were used to calculate values of diode saturation current density J_o because of recombination in the Si solar cell absorber, and II–VI/Si tandem solar cell efficiencies based on them. For cell architectures with the p-n junction near the front of the Si bottom cell and a passivated (10 cm/s) Si emitter front surface, these J_o values from measured Si lifetimes are consistent with II–VI/Si tandem cell efficiencies over 30% under the 1-sun AM1.5G solar spectrum.

Modeling highlights the importance of cell structure on the tandem cell performance that can be reached. Achievement of Si emitter front surface passivation is crucial to achieve the potential efficiency of the tandem cell design. For passivated (10 cm/s) emitters, over 30% tandem efficiency can be achieved for Si absorber lifetimes >120 μs, in both n^+/p and p^+/n thin emitter, thick base (absorber) designs, while in n/p^+ thick emitter (absorber), thin base designs over 350 μs absorber lifetime is required for the cell parameters considered here.

Important technological barriers exist for the realization of cost-effective II–VI/Si two-junction solar cells, including the development of 1.7-eV top cell absorbers with low W_{oc}; highly transparent and conductive interlayers; low recombination at the interface between the interlayers and the front surface of the Si bottom cell; and maintaining minority-carrier lifetime in the Si bottom cell bulk. While significant challenges remain, this experimental study indicates that long bulk lifetime in the Si bottom cell is one necessary step toward high efficiency II–VI/Si tandems that can be achieved.

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