A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier

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***Abstract*— This article presents a multi-subharmonic switching (SHS) digital power amplifier (PA) architecture for enhancing power back-off (PBO) efficiency while achieving watt-level output power. The proposed phase-interleaved architecture provides the inherent cancellation of the subharmonic components in the PBO region, alleviating the burden of the matching network. The proposed multi-SHS scheme can be further combined with a class-G operation to create a greater number of efficiency peaks in the PBO region. A transformer-based, three-way power combiner and a triple-stacking class-D driver are utilized to obtain watt-level output power. The proof-of-concept PA prototype is implemented with a switched-capacitor PA (SCPA) architecture in 65-nm CMOS and achieved 30-dBm peak power at 1.9 GHz, with 45.9%/41.3%/35.3%/32.2%/24.2% drain efficiency located at 0-, −3.5-, −7.0-, −9.5-, and −12-dB PBO, respectively. The average efficiency was 31.4% in real-time operation with a 7.2-dB peak-to-average power ratio (PAPR) modulated signal.**

***Index Terms*— Class-G, CMOS PA, efficiency enhancement, efficiency, high power, multi-subharmonic switching (multi-SHS), phase-interleaved, polar transmitter, power amplifier (PA), power back-off (PBO), switched-capacitor PA (SCPA), subharmonic switching (SHS), subharmonic.**

I. Introduction

DRIVEN by the increasing demand for data capacity, modern wireless communication standards employ high spectrum density modulations, given the finite bandwidth. This type of modulation scheme often leads to a large peak-to-average power ratio (PAPR) [1]–[5]. Transmitting a large PAPR signal suggests that the power amplifiers (PAs) operate in the power back-off (PBO) region most of the time. Conventional PAs usually yield the highest efficiency at peak output power but provide poor efficiency in the PBO region. The PA average efficiency is the integration of the power density function multiplied by the efficiency at different power levels. Given existing communication schemes, such as the 5G communication system, the PAPR can be larger than 12 dB [6]–[8]. As the most power-hungry block in the transmitter, enhancing the average power efficiency of the PA plays a critical role in reducing the overall energy consumption of communication systems [9]–[12].

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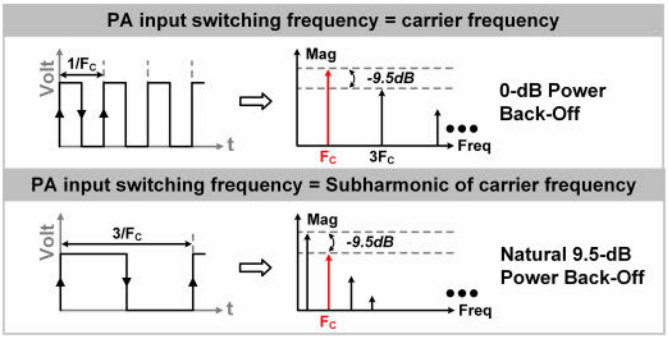

Fig. 1. SHS digital PA input waveform.

However, many techniques for enhancing PBO efficiency typically enhance the efficiency down to the 6-dB back-off point. An envelope-tracking PA can enhance the efficiency in the deep PBO region [13], [14]. Based on the transmitted signal envelope, the supply modulator changes the PA supply instantaneously, which leads to high back-off efficiency. However, a supply modulator with large bandwidth and dynamic range could be a design challenge. Load modulation is another alternative for achieving deep enhancement of PBO efficiency [15], [16]. This technique can always provide maximum efficiency at different output power levels by tuning a matching network. However, making a wideband tunable matching network that can sustain large voltage stress continues to be a design challenge. Recently, a subharmonic switching (SHS) digital PA architecture was proposed in [17]–[19]. It naturally achieves PBO by toggling the switching PA cells at the subharmonic of the carrier frequency (Fc), e.g., one-third of the Fc (see Fig. 1). This operation can reduce the conduction loss of the PA, switched capacitance dynamic loss, and provide better impedance matching. However, to eliminate the unwanted subharmonic tones, additional notch filtering is required to remove those spurs, which potentially increases the order of the matching network. Although the sharp notch response may be achieved with high-Q off-chip components, doing so limits the PA bandwidth at the carrier frequency. Therefore, we propose a phase-interleaved architecture that inherently cancels the undesired spurs. Meanwhile, this architecture can be used to increase the peak output power of the PA, achieving watt-level output power. Moreover, based on the SHS concept, a multi-SHS technique is proposed to create a larger number of efficiency peaks over a deeper PBO region, which enhances the PA average efficiency as well as supports a higher PAPR signal. Finally, the proposed

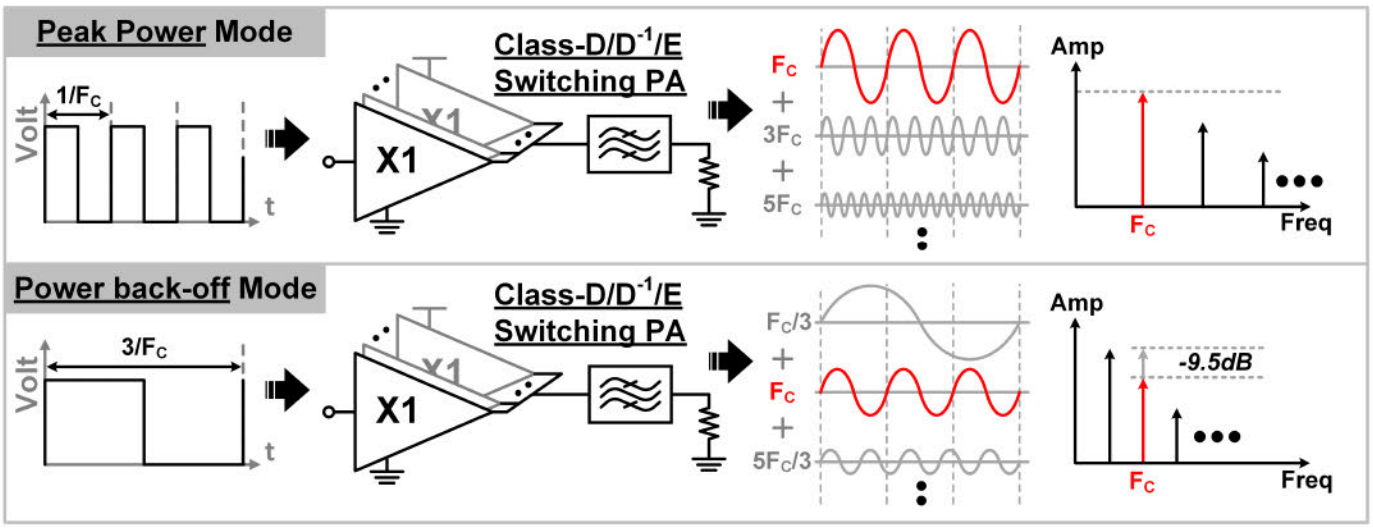

Fig. 2. SHS digital PA operation.

architecture can be further combined with other efficiency-enhancement techniques to improve the average efficiency.

This article is organized as follows. Section II introduces the operation principle and efficiency enhancement of the proposed multi-SHS techniques and the phase-interleaved architecture for the inherent subharmonic cancellation. Section III shows the combination of multi-SHS with the class-G operation. The optimization of intra-peaks efficiency is also shown. Section IV describes the block diagram and the implementation of the key building blocks in this prototype. The static and dynamic measurement results are given in Section V, followed by conclusions in Section VI.

II. Proposed Multi-Subharmonic Switching Technique

A. Proposed Multi-SHS Operation

We first briefly review the concept of the SHS PA, as shown in Fig. 2. In the peak power mode, the PA switching frequency equals the carrier frequency. The matching network picks up the fundamental of the square waveform as the carrier frequency. As we notice here, the input switching waveform is a square wave, and it contains odd-harmonic components, assuming it is a 50% duty cycle. The power profile of the harmonics is in the descending order (i.e., the third harmonic is lower than the fundamental tone, and the fifth harmonic is even lower).

The PA works in the SHS region when the PA toggles at a subharmonic of the carrier frequency and chooses the harmonic as the carrier frequency. It naturally achieves PBO without turning off the PA cells or reducing the power supply. For example, if we use the third subharmonic, Fc/3, to toggle the PA cells, its third-harmonic component, i.e., Fc, equates the carrier frequency. In this case, the output power at Fc is $10 \cdot \log10((^1/_3)^2)$ dB lower due to the square switching waveform and, hence, achieves PBO. Extending from the SHS PA concept, we propose a multi-SHS scheme by using multiple SHS waveforms, that is, there are multiple toggling frequency

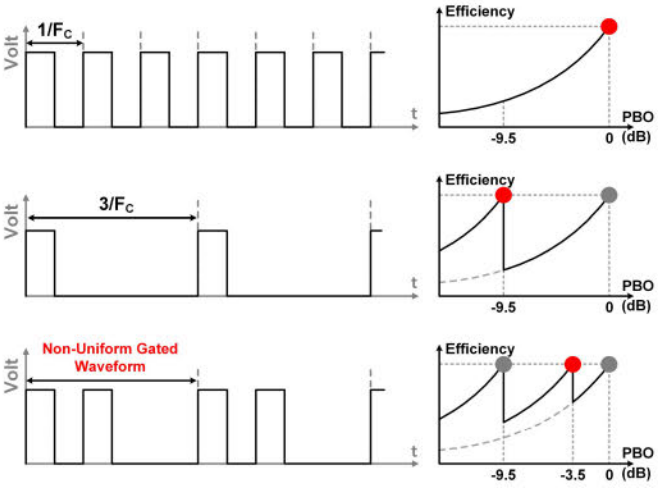

Fig. 3. Switching waveforms of the proposed multi-subharmonic operation.

candidates for each PA driver cell. The selection of the actual toggling frequency depends on the intended PBO level. In other words, each PA driver cell can toggle at Fc/3, 2Fc/3, or Fc. In the SHS PA, we have shown that Fc/3 waveform can be generated via a divide-by-three circuit.

To generate 2Fc/3 for a multi-SHS PA, we propose a non-uniform gating scheme to create the switching waveform. As shown in Fig. 3, if we non-uniformly gate off one of the pulses at Fc, it naturally derives the frequency of 2Fc/3. All the PA driver cells simultaneously toggle twice every three cycles. The output power possesses $10 \cdot \log10((^2/_3)^2)$ less power compared to peak power mode. Assuming the PA unit cell is lossless, the whole PA architecture can lead to an efficiency peak at the −3.5-dB PBO point. More details of the efficiency peak will be addressed in Section II.B. Note that the proposed non-uniform gating scheme allows a simple implementation, as a window function can be directly gated with the original waveform at the carrier frequency (Fc), avoiding the need for a fractional-N frequency synthesizer.

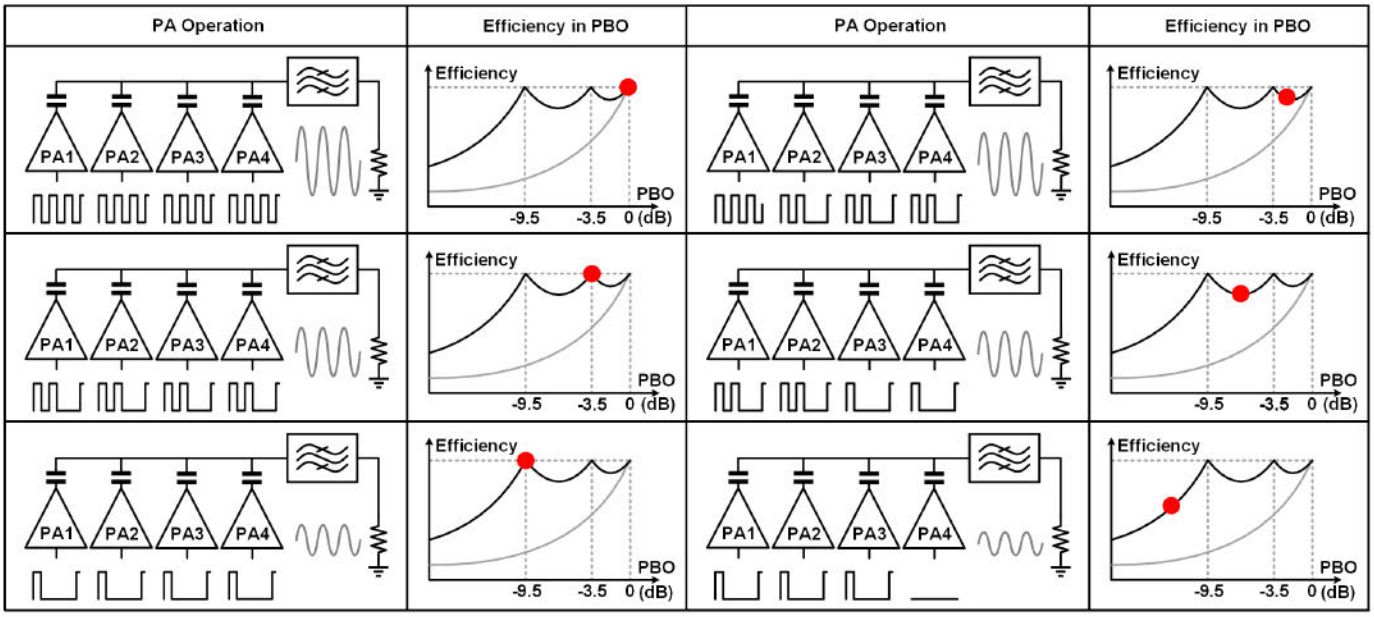

Fig. 4. Multi-SHS digital PA at different output power levels.

In addition, the same scheme can be easily extended to use deeper subharmonics, such as Fc/5, 2Fc/5, and 3Fc/5, and creates even more efficiency peaks.

B. Efficiency Enhancement in a Multi-SHS Digital PA

In this section, we analyze the efficiency enhancement using a multi-SHS PA. There are three efficiency-enhancement mechanisms in an SHS digital PA, including PA conduction loss, impedance matching, and dynamic loss in a switched capacitor bank. More detailed derivations can be found in [18]. A multi-SHS PA has the same efficiency-enhancement mechanism for PA conduction loss and impedance matching. The switched capacitor dynamic loss is different compared to the SHS digital PA. We focus on the dynamic loss savings to validate the multiple efficiency peaks created by the multi-SHS scheme.

Fig. 4 shows the multi-SHS switched-capacitor PA (SCPA) in different power regions. The efficiency can be improved by operating different subharmonics between the efficiency peaks. To derive the power and efficiency equations under a multi-SHS scheme, the conventional SCPA output power and drain efficiency (DE) equations considering the switched capacitor dynamic loss are repeated here [20]

$$\begin{cases} P_{\text{SC}} = \dfrac{n(N-n)}{N^2} C V_{DD}^2 F_C \\ P_{\text{out}} = \dfrac{2}{\pi^2}\left(\dfrac{n}{N}\right)^2 \dfrac{V_{DD}^2}{R_L} \\ \eta_D = \dfrac{P_{\text{out}}}{P_{\text{out}} + P_{\text{SC}}} = \dfrac{1}{1 + \frac{\pi}{4}\frac{(N-n)}{n}\frac{1}{Q_{\text{LOAD}}}} \\ Q_{\text{LOAD}} = \dfrac{2\pi F_C L}{R_L} = \dfrac{1}{2\pi F_C C R_L} \end{cases} \tag{1}$$

where N is the total number of digital PA branches. Assuming the number of toggling PA cells is n, dynamic power loss P_{SC} and output power P_{out} are shown in equation (1).

Here, we will derive theoretical efficiency and dynamic loss of multi-SHS in the representative PBO. We assume that $(N - M)$ and M of the PA cells will toggle at the frequency of F_{SH1} and F_{SH2}, respectively. By design, $\{F_{\text{SH1}}$ and $F_{\text{SH2}}\}$ is the subset of adjacent frequency candidates, namely, fundamental, subharmonic frequencies, and 0, where $F_{\text{SH1}} > F_{\text{SH2}}$. Note that when the toggling frequency is zero, it indicates that the PA cell does not toggle. Next, a generalized multi-SHS PA dynamic loss, output power, and efficiency can be derived as

$$\begin{cases} P_{\text{SC}} = \dfrac{M(N-M)}{N^2} C V_{\text{DD}}^2 (F_{\text{SH1}} - F_{\text{SH2}}) \\ P_{\text{out}} = \dfrac{2}{\pi^2}\left(\dfrac{N-M}{N}\dfrac{F_{\text{SH1}}}{F_C} + \dfrac{M}{N}\dfrac{F_{\text{SH2}}}{F_C}\right)^2 \dfrac{V_{\text{DD}}^2}{R_L} \\ \eta_D = \dfrac{P_{\text{out}}}{P_{\text{out}} + P_{\text{SC}}} \\ = \dfrac{1}{1 + \frac{\pi}{4}\frac{M(N-M)F_C(F_{\text{SH1}}-F_{\text{SH2}})}{[(N-M)F_{SM1}+MF_{SM2}]^2}\frac{1}{Q_{\text{LOAD}}}}. \end{cases} \tag{2}$$

While (2) describes a general case of multi-SHS PA, our silicon prototype uses the third-subharmonic frequencies, i.e., the toggling frequency candidates include Fc, 2Fc/3, Fc/3, and 0. As shown in Fig. 4, when the PA operates between 0- and −3.5-dB PBO, a portion of the PA cells starts to toggle at 2Fc/3, while the rest toggle at Fc. The frequency difference results in some charge redistribution and, thus, introduces some energy loss in the capacitor bank. When the PA operates between −3.5- and −9.5-dB PBO, the PA cells toggle at either 2Fc/3 or Fc/3. The dynamic loss is smaller compared to that of the conventional SHS PA. When the PA operates at the $<$ −9.5-dB PBO region, a portion of PA cells starts to turn off, resulting in efficiency roll-off. The PA efficiency and output

Code	PBO(dB)	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15
0000	OFF															
0001	23.5	Fc/3	Fc/3	Fc/3												
0010	17.5	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3									
0011	14	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3						
0100	11.5	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3			
0101	9.5	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	2Fc/3	2Fc/3	2Fc/3
0110	8	2Fc/3	2Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	2Fc/3	2Fc/3	2Fc/3
0111	6.6	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	Fc/3	2Fc/3	2Fc/3	2Fc/3
1000	5.5	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	Fc/3	Fc/3	Fc/3	2Fc/3	2Fc/3	2Fc/3
1001	4.4	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3
1010	3.5	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	Fc	Fc	Fc
1011	2.7	Fc	Fc	Fc	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	Fc	Fc	Fc
1100	1.9	Fc	Fc	Fc	Fc	Fc	Fc	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	2Fc/3	Fc	Fc	Fc
1101	1.2	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	2Fc/3	2Fc/3	2Fc/3	Fc	Fc	Fc
1110	0.6	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	2Fc/3	2Fc/3	2Fc/3
1111	0	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc	Fc

Cell OFF
Fc/3
2Fc/3
Fc

Fig. 5. Example of a multi-SHS digital PA operation table.

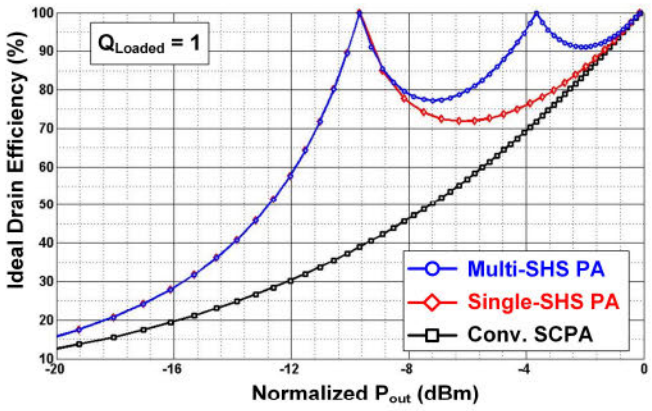

Fig. 6. Ideal efficiency of multi-SHS PA architecture versus P_{out} and for single-SHS PA and conventional SCPA.

power follow those of the SHS PA [18]. The ideal efficiency under different PBO regions can be expressed as

$$\begin{cases} \eta_D = \dfrac{1}{1+\frac{\pi}{4}\frac{n(N-M)}{(N-M/3)^2}\frac{1}{Q_{\text{LOAD}}}}, & P_{\text{out}} \in 0 \sim -3.5 \text{ dB} \\ \eta_D = \dfrac{1}{1+\frac{\pi}{4}\frac{3M(N-M)}{(2N-M)^2}\frac{1}{Q_{\text{LOAD}}}}, & P_{\text{out}} \in -3.5 \sim -9.5 \text{ dB} \\ \eta_D = \dfrac{1}{1+\frac{\pi}{4}\frac{(N-M)}{M/3}\frac{1}{Q_{\text{LOAD}}}}, & P_{\text{out}} \in -9.5 \sim -13 \text{ dB}. \end{cases} \quad (3)$$

Fig. 5 shows the 4-bit multi-SHS lookup table (LUT) to illustrate the operation, while the actual implementation is 8-bit with class-G. The general LUT design guideline is to minimize the equivalent capacitance, which requires more PA unit cells to be turned on simultaneously. Note that at certain output power level, the PA cells can operate with different subharmonics. With this hybrid operation, efficiency between the peaks can be optimized as well.

The efficiency tradeoffs with P_{out} for multi-SHS, single-SHS digital PA, and conventional SCPA are plotted in Fig. 6. In this comparison, the loaded quality factor Q_{Loaded} is fixed to 1. The PBO efficiency curve indicates that the multi-SHS PA PBO efficiency is always higher than other alternative architectures. Note that the multi-SHS can further combine with other efficiency-enhancement techniques to improve the deep PBO efficiency.

C. Phase-Interleaved Subharmonics Inherent Cancellation

Unwanted subharmonics can violate the mask and degrade the PA efficiency if they appear at the transmitter output waveform. These spurs can cause reciprocal mixing or violate the emission mask [21]. Notch filtering embedded in the matching network is required, which inevitably increases the matching order and complexity. It becomes worse when we use the multi-SHS scheme, as there are multiple subharmonic frequencies to be notched. We propose the phase-interleaved PA architecture to cancel the undesired subharmonics before the power combiner without introducing additional power loss.

Fig. 7 shows the phase-interleaved power combining under two different input switching waveforms. Assuming the PA voltage signal is $V_{\text{PA},i}$ ($i = 1, 2, 3$) and the PA output impedance is $R_{\text{PA},i}$, the current in the primary winding of the transformers can be calculated by using the superposition theorem [22]. The primary current of the three-way transformer-based combiner can be written as

$$I_{p,i} = \frac{n_i(n_1 V_{\text{PA},1} + n_2 V_{\text{PA},2} + n_3 V_{\text{PA},3})}{R_L + (n_1^2 R_{\text{PA},1} + n_2^2 R_{\text{PA},2} + n_3^2 R_{\text{PA},3})}. \quad (4)$$

The output impedance is R_L, and the transformer turn ratio is n_i. The transformer impedance seen by each PA becomes

$$Z_i = \frac{(R_L + (n_1^2 R_{\text{PA},1} + n_2^2 R_{\text{PA},2} + n_3^2 R_{\text{PA},3}))V_{\text{PA},i}}{n_i(n_1 V_{\text{PA},1} + n_2 V_{\text{PA},2} + n_3 V_{\text{PA},3})} - R_{\text{PA},i}. \quad (5)$$

It is clear that the transformer impedance seen by each PA is related to load impedance R_L and the output voltage signal (the magnitude and the phase) of all the PA cells. Based on the observation, if the summation of the three voltage signals becomes zero, then the impedance seen by each PA is infinity, which can potentially reject the unwanted subharmonics. Assuming the turn ratio n_i of the three coils is equal to n, three PAs have the same output impedance R_{PA}; when the three PA voltage signals are in phase, the primary current of each PA cell can be written as

$$I_p = \frac{n^2(A_{\text{PA},1} + A_{\text{PA},2} + A_{\text{PA},3})\sin(\omega t)}{R_L + 3n^2 R_{\text{PA}}}. \quad (6)$$

The transformer impedance can be written as

$$Z_i = \frac{(R_L + 3n^2 R_{\text{PA}})A_{\text{PA},i}\sin(\omega t)}{n^2(A_{\text{PA},1} + A_{\text{PA},2} + A_{\text{PA},3})\sin(\omega t)} - R_{\text{PA}}. \quad (7)$$

The current waveform and the voltage waveform are in phase. The transformer impedance seen by each PA is identical. The power is combined at the secondary winding side. If the three PA voltage signals are 120° apart, then the primary current becomes

$$I_p = \frac{n^2}{R_L + 3n^2 R_{\text{PA}}}\left(A_{\text{PA},1}\sin(\omega t) + A_{\text{PA},2}\sin\left(\omega t + \frac{2\pi}{3}\right) + A_{\text{PA},3}\sin\left(\omega t + \frac{4\pi}{3}\right)\right). \quad (8)$$

As observed in (11), if three PAs present the same magnitude A, the primary current becomes zero in this condition. In other words, output impedance Z_i seen by the PA is infinity,

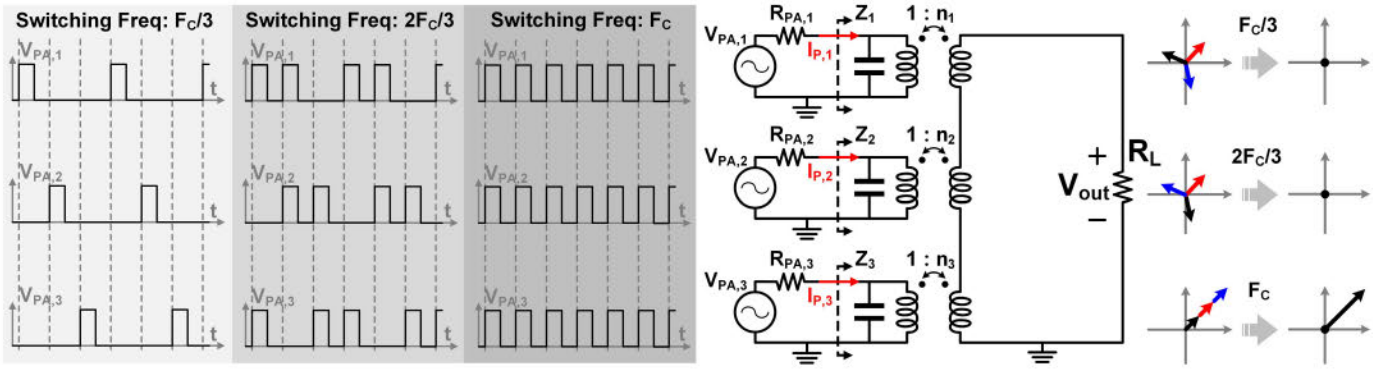

Fig. 7. Equivalent circuit model of ideal three-way phase-interleaved multi-SHS PA with different input switching waveforms.

and the unwanted signal gets rejected from the primary side with a certain phase difference. Although the voltage signal is non-zero, the power loss, which equals the integration of the voltage multiplied by the current, becomes zero due to zero primary current. More importantly, as long as the summation of the three PA voltage signals becomes zero, the R_L value will not affect the results of the cancellation. In other words, the cancellation of the subharmonic component is effective over different voltage standing wave ratios (VSWRs).

Based on the discussions in this section, if the desired carrier frequency component is in phase and the subharmonic frequencies are out of phase, we can combine the output power at the desired frequency and inherently cancel the unwanted subharmonics. The phasors in Fig. 7 show inherent cancellation in Fc/3 and 2Fc/3 frequency components, while the Fc frequency components are added coherently. The phase-interleaved Fc/3 and 2Fc/3 square waves contain Fc/3 components 120° apart and 2Fc/3 components 240° apart, where the Fc components are combined in phase. In conclusion, all the unwanted subharmonics components are nullified, except for the residual errors due to magnitude and phase mismatches, which will be discussed in the following.

1) Amplitude Mismatch: So far, we assume all three PA banks are identical. However, in a real implementation, there will be mismatches between different PA banks. PA magnitude and phase errors can degrade the effectiveness of the inherent cancellation, as we can observe from the measurement results. Here, we first analyze the impact of magnitude mismatches on the PA output spectrum. Considering one of the PA magnitudes now becomes $(A+\Delta A)$, the corresponding current and voltage at Fc/3 derived from (7) can be written as

$$\begin{cases} I_p\left(\frac{\omega_C}{3}t\right) = \dfrac{n^2}{R_L + 3n^2 R_{\mathrm{PA}}} \displaystyle\sum_{i=1}^{3} V_{\mathrm{PA},i}\left(\frac{\omega_C}{3}t\right) \\ V_{\mathrm{PA},1}\left(\frac{\omega_C}{3}t\right) = (A+\Delta A)\sin\left(\frac{\omega_C}{3}t\right) \\ V_{\mathrm{PA},2}\left(\frac{\omega_C}{3}t\right) = A\sin\left(\frac{\omega_C}{3}t + \frac{2\pi}{3}\right) \\ V_{\mathrm{PA},3}\left(\frac{\omega_C}{3}t\right) = A\sin\left(\frac{\omega_C}{3}t + \frac{4\pi}{3}\right). \end{cases} \tag{9}$$

The subharmonic power, $P_{\mathrm{SH},i}$, is the integration of the product of the voltage and current at subharmonic

$$\begin{cases} P_{\mathrm{SH},1} = \displaystyle\int_0^{2\pi} I_p\left(\frac{\omega_C}{3}t\right) V_{\mathrm{PA},1}\left(\frac{\omega_C}{3}t\right) = \frac{\pi\,\Delta A(A+\Delta A)n^2}{R_L + 3n^2 R_{\mathrm{PA}}} \\ P_{\mathrm{SH},2} = \displaystyle\int_0^{2\pi} I_p\left(\frac{\omega_C}{3}t\right) V_{\mathrm{PA},2}\left(\frac{\omega_C}{3}t\right) = -\frac{\pi}{2}\frac{\Delta A \cdot An^2}{R_L + 3n^2 R_{\mathrm{PA}}} \\ P_{\mathrm{SH},3} = \displaystyle\int_0^{2\pi} I_p\left(\frac{\omega_C}{3}t\right) V_{\mathrm{PA},3}\left(\frac{\omega_C}{3}t\right) = -\frac{\pi}{2}\frac{\Delta A \cdot An^2}{R_L + 3n^2 R_{\mathrm{PA}}}. \end{cases} \tag{10}$$

Assuming the transformer is lossless, the total subharmonic power P_{SH} at the undesired subharmonic can be written as

$$P_{\mathrm{SH}} = \sum_{i=1}^{3} P_{\mathrm{SH},i} = \frac{\pi \cdot \Delta A^2 \cdot n^2}{R_L + 3n^2 R_{\mathrm{PA}}}. \tag{11}$$

We can observe that the undesired power due to gain mismatch is proportional to ΔA^2. The corresponding current and voltage amplitudes at Fc are three times smaller than the subharmonic

$$\begin{cases} I_p(\omega_C t) = \dfrac{n^2}{R_L + 3n^2 R_{\mathrm{PA}}} \dfrac{\Delta A}{3} \sin(\omega_C t) \\ V_{\mathrm{PA},1}(\omega_C t) = \dfrac{A+\Delta A}{3} \sin(\omega_C t) \\ V_{\mathrm{PA},2}(\omega_C t) = \dfrac{A}{3} \sin(\omega_C t) \\ V_{\mathrm{PA},3}(\omega_C t) = \dfrac{A}{3} \sin(\omega_C t). \end{cases} \tag{12}$$

Similar to (10), the total output power considering the amplitude mismatch at Fc becomes

$$P_{\mathrm{out}} = \sum_{i=1}^{3} P_{\mathrm{PA}i} = \frac{\pi \cdot (3A + \Delta A)^2 \cdot n^2}{9 \cdot (R_L + 3n^2 R_{\mathrm{PA}})}. \tag{13}$$

Therefore, the amplitude mismatch-induced SFDR becomes

$$\mathrm{SFDR} = 10\lg\frac{P_{\mathrm{out}}}{P_{\mathrm{SH}}} = 20\lg\frac{3A + \Delta A}{3 \cdot \Delta A}. \tag{14}$$

From (14), one can calculate the amplitude mismatch requirement for this PA architecture. As an example, when $\Delta A/A \sim 1\%$, SFDR is roughly 40 dB. To meet the mask and

EMI/EMC requirement, the proposed non-overlapping clock is utilized to calibrate the amplitude difference of each path.

2) Phase Mismatch: Next, we discuss the effect of the phase error. Assuming all the three PAs are matched, except that one PA presents a phase offset $\Delta\theta$, the current and voltage equations are

$$\begin{cases} I_p(\omega_C t) = \dfrac{An^2}{R_L + 3n^2 R_{\mathrm{PA}}} \displaystyle\sum_{i=1}^{3} V_{\mathrm{PA},i}(\omega_C t) \\ V_{\mathrm{PA},1}(\omega_C t) = A\sin(\omega t + \Delta\theta) \\ V_{\mathrm{PA},2}(\omega_C t) = A\sin\left(\omega t + \dfrac{2\pi}{3}\right) \\ V_{\mathrm{PA},3}(\omega_C t) = A\sin\left(\omega t + \dfrac{4\pi}{3}\right). \end{cases} \tag{15}$$

Similarly, the subharmonic power of each PA can be expressed as

$$\begin{cases} P_{\mathrm{SH},1} = \dfrac{n^2A^2\pi}{R_L + 3n^2R_{\mathrm{PA}}}(1 - \cos(\Delta\theta)) \\ P_{\mathrm{SH},2} = \dfrac{n^2A^2\pi}{R_L + 3n^2R_{\mathrm{PA}}}\left(\dfrac{1}{2} - \dfrac{1}{2}\cos(\Delta\theta) + \dfrac{\sqrt{3}}{2}\sin(\Delta\theta)\right) \\ P_{\mathrm{SH},3} = \dfrac{n^2A^2\pi}{R_L + 3n^2R_{\mathrm{PA}}}\left(\dfrac{1}{2} - \dfrac{1}{2}\cos(\Delta\theta) - \dfrac{\sqrt{3}}{2}\sin(\Delta\theta)\right). \end{cases} \tag{16}$$

As a result, the total subharmonic power P_{SH} becomes

$$P_{\mathrm{SH}} = \sum_{i=1}^{3} P_{\mathrm{SH},i} = \frac{2n^2A^2\pi}{R_L + 3n^2R_{\mathrm{PA}}}(1 - \cos(\Delta\theta)). \tag{17}$$

From (17), it shows that the power at the unwanted subharmonic frequency is a function of $\cos(\Delta\theta)$, which is relatively insensitive when the phase error is small.

Similar to the derivation of amplitude mismatch, the total output power considering the amplitude mismatch at Fc becomes

$$P_{\mathrm{out}} = \sum_{i=1}^{3} P_{\mathrm{PA}i} = \frac{\pi \cdot A^2 \cdot n^2 \cdot (5 + \cos(3\Delta\theta))}{9 \cdot (R_L + 3n^2R_{\mathrm{PA}})}. \tag{18}$$

Therefore, the amplitude mismatch-induced SFDR becomes

$$\mathrm{SFDR} = 10\log\frac{P_{\mathrm{out}}}{P_{\mathrm{SH}}} = 10\log\frac{5 + 4\cos(3\Delta\theta)}{18(1 - \cos(\Delta\theta))}. \tag{19}$$

From (19), when $\Delta\theta$ equals 1.8° at Fc, it yields roughly 40-dB SFDR. The phase detector and tunable delay cells are implemented on-chip to calibrate the phase mismatch between different channels. The delay cells have a 0.2-ps tuning resolution with 2-ns tuning range, i.e., 10-bit resolution.

Note that the calculated SFDR, since both amplitude mismatch and phase mismatch assume the matching network and antenna, presents an all-pass response. In reality, additional attenuation can be achieved via matching network and antenna's selectivity, which suggests better SFDR between fundamental and subharmonic components.

In the real implementation, there are more mismatch sources, such as PA output impedance R_{PA} and transformer coupling factor n_i, which can be analyzed in a similar analysis strategy. In addition, due to the associated parasitic inductance from the transformer, the current at the subharmonics is non-zero. Fortunately, the current waveform remains 90° out-of-phase with the voltage waveform, and thus, it still achieves the cancellation and zero power loss.

III. Multi-SHS and Hybrid Class-G Operation

The phase-interleaved multi-SHS operation can be further combined with other existing efficiency-enhancement techniques to further improve the average efficiency under different PAPRs. All three PA banks must maintain the same input switching pattern and the same supply configuration to guarantee that the output power of each PA bank is identical, which results in effective cancellation on all the subharmonics, as the equations shown in Section II.

In this section, we introduce a multi-SHS digital PA with the hybrid class-G operation to optimize efficiency for different PAPR signals. The class-G operation changes the power supply of each PA driver to create different output power levels. In the real implementation, we chose either $2V_{\mathrm{DD}}$ or $3V_{\mathrm{DD}}$ for class-G, and either Fc/3 or 2Fc/3 for multi-SHS, to achieve five ideal efficiency peaks located at 0, −3.5, −7.0, −9.5, and −13 dB (see Fig. 8). The efficiency between the peaks can be further improved by toggling the cells of each PA with different supplies and input switching frequencies.

In addition, the efficiency between the peaks can be further improved by toggling the cells of each PA with different supplies and input switching frequencies (see Fig. 8). To optimize the efficiency between the peaks, the general guideline is to reduce the equivalent capacitance from the capacitor bank and minimize the toggling overhead. From 0- to −3.5-dB PBO, the hybrid class-G operation is utilized to create the PBO and enhance efficiency. From −3.5- to −7-dB PBO, all the PA cells are tied to $2V_{\mathrm{DD}}$ but with different input switching frequencies. As an example, shown in Fig. 8, two PA cells toggle with Fc, and one PA cell toggles at 2Fc/3 at −4.5-dB PBO. Note that all three PA banks must keep the same configuration to maintain the same output power. Therefore, the subharmonic inherent cancellation requirement can be satisfied.

Between −7- and −9.5-dB PBO, all the PA cells toggle at different supplies and input switching frequencies. For example (see Fig. 8), in each PA bank, two PA cells toggle at 2Fc/3 with $2V_{\mathrm{DD}}$, and one PA cell toggles at Fc/3 with $3V_{\mathrm{DD}}$ at −7.8-dB PBO. From −9.5- and −13-dB PBO, all the PA cells have the same input switching frequency, Fc/3, and different supplies. In Fig. 8, all the PA cells toggle at Fc/3 with the $2V_{\mathrm{DD}}$ and $3V_{\mathrm{DD}}$ supplies, which creates −11.7-dB PBO. Based on the optimal efficiency value, we determine the combination of different supplies and switching frequencies. Note that the phase-interleaved subharmonic cancellation is effective for all amplitude levels, as the input waveforms of each PA bank are the same except for the 120° phase shift between them. The compiled LUT is fully synthesized in the multi-SHS block.

IV. Circuit Implementation

A. Overall Block Diagram

Fig. 9 shows the top-level block diagram of the phase-interleaved multi-SHS PA prototype. The prototype adopted

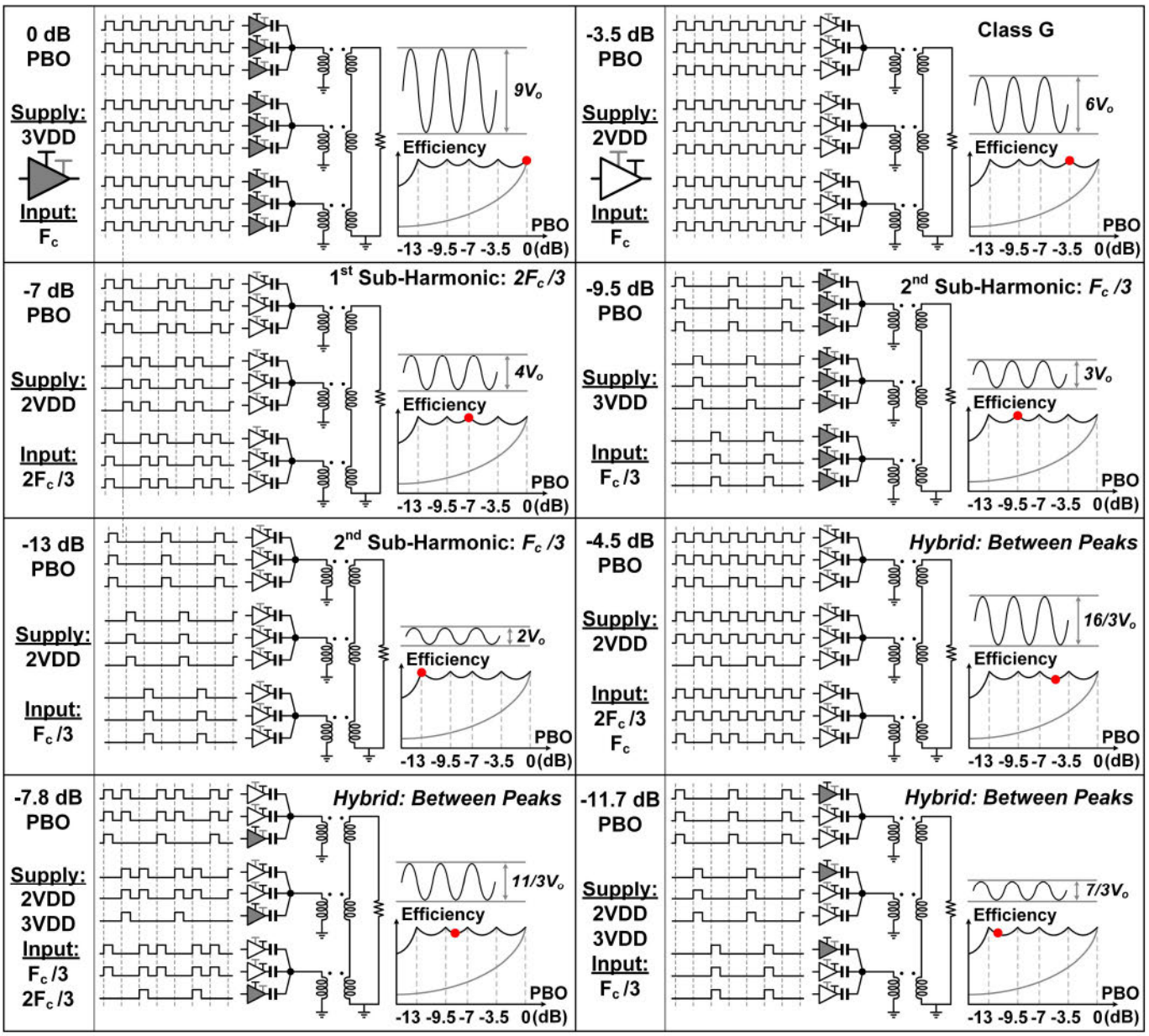

Fig. 8. Complete phase-interleaved multi-SHS digital PA with the hybrid class-G operation.

the polar architecture with the consideration of high efficiency. The input paths contain amplitude modulation (AM) and phase modulation (PM) paths. The differential PM signal first passes through the current-mode logic (CML) buffers and converts to the rail-to-rail CMOS-type PM signal. Then, the PM signal is distributed to three local phase generators with different control settings. The phase generator creates three phase signals, including a delayed original PM signal (Fc), a divide-by-three PM signal (Fc/3), and a non-uniform gated PM signal (2Fc/3). To mitigate time skew between different phase generators and different PM signals, phase detectors and tunable delays are implemented. The generated phase signals then pass through the high-speed multiplexer (MUX). Note that the phase control signal is retimed with the original PM signal to avoid phase glitches. Depending on the AM LUT, the MUX selects the PM signals corresponding to the intended PA input switching frequency.

The 8-bit AM signal and the clock signal are generated off-chip using the low-voltage differential signaling (LVDS) format. Depending on the modulated signal bandwidth, the sample rate of the AM signals can be set up to 1 GS/s. The AM signal is first sent to a digital decoder, which generates the LUT for multi-SHS with the hybrid class-G operation. The LUT outputs contain the amplitude code, phase control word, and supply control word to control the phase-interleaved PA core. All the control signals are properly retimed and phase-aligned for the multi-SHS operation. An "H-tree" layout strategy is utilized to minimize the time skew between different channels and control signals. Note that each PA bank must maintain the same amplitude code to generate the

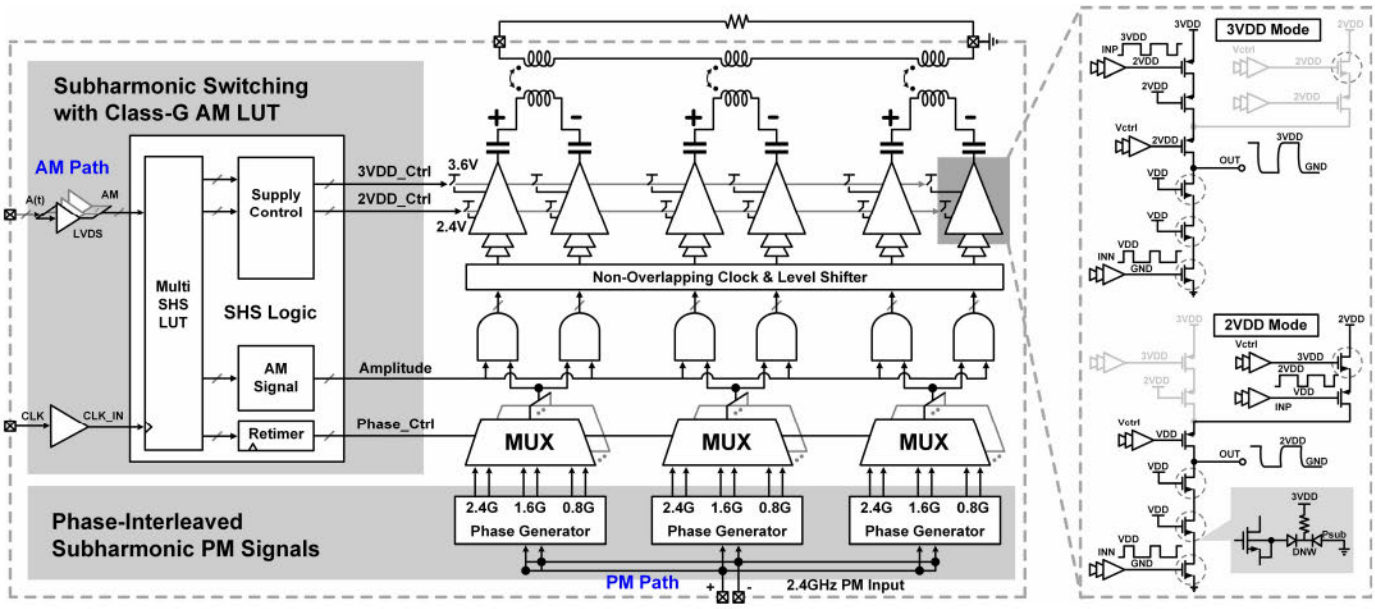

Fig. 9. Block diagram of the PA prototype.

same output power. It guarantees the subharmonic cancellation under all the different output power levels, as we discussed in Section II.

The desired PM signal and amplitude code are combined in the polar combiner before the PA drivers. The non-overlapping clock is implemented to generate non-overlapping PA input signals to suppress the crowbar current, which can improve the class-D driver peak efficiency. It also achieves an equivalent resolution of 1.2 mV in the voltage domain to fine calibrate the unwanted subharmonic spurs. We use a three-stacking class-D driver to enlarge the output voltage. Depending on the control LUT, the driver can work in the $2V_{DD}$ and $3V_{DD}$ modes separately. The load-pull simulation includes all the PA drivers that are matched to the load that generates the best efficiency point. More implementation details about the triple stacking drivers can be found in [23]. The PA driver outputs connect to the capacitor bank. The custom-designed precise MIM capacitor is implemented to result in differential nonlinearity (DNL). Finally, an on-chip three-way power combiner is used, which is described in the following Section IV.B.

B. Three-Way Power Combiner

The proposed transformer-based power combiner provides four main objectives in this PA prototype: power combining, inherent subharmonic cancellation, differential to single-ended conversion, and impedance matching. Fig. 10 shows the singled-ended equivalent circuit of the transformer. First, each of the transformers sees a differential $R_L/3$ load (single-ended $R_L/6$) due to the three-way power combiner. There are two turns for both primary and secondary sides to obtain enough inductance. The transformer's intrinsic inductance, together with the switched capacitor bank, will convert the load impedance to the PA optimum load impedance at the carrier frequency.

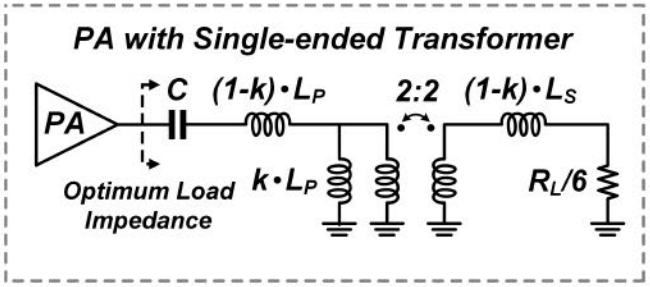

Fig. 10. Three-way power combiner model in HFSS.

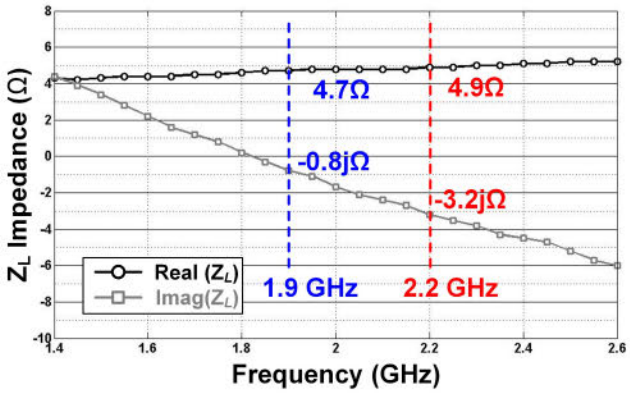

Fig. 11. Simulated PA load impedance Z_L versus frequency.

Fig. 11 shows the simulated PA load impedance Z_L versus the frequency. The result shows that the impedance is around 5.5 Ω with 1-Ω variation from 1.45 to 2.25 GHz, achieving wideband impedance transformation with low loss. The matching load impedance is designed as 5.5 Ω to provide optimum efficiency and output power.

The "figure 8" power combiner structure could be a potential candidate for a high-efficiency high-power PA design, as it helps reduce mutual coupling between adjacent primary coils.

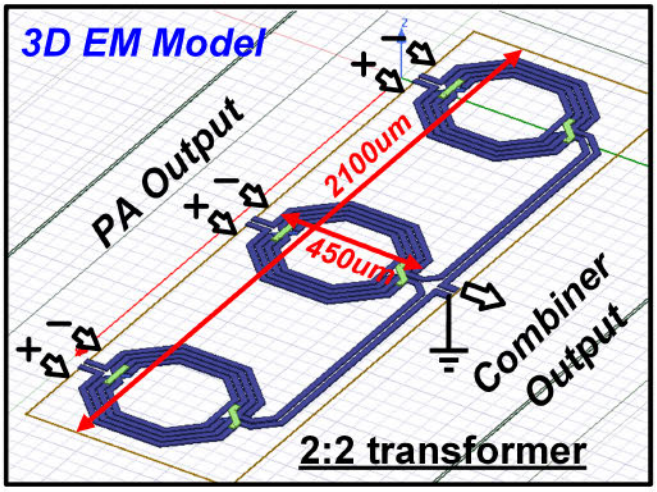

Fig. 12. Three-way power combiner model in HFSS.

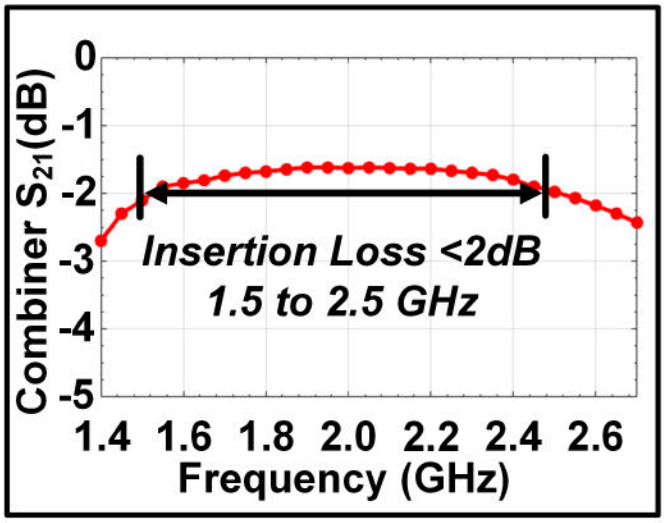

Fig. 13. Simulated S_{21} of the power combiner over the frequencies.

However, for the "figure 8" structure, all the primary windings are not symmetric with respect to the secondary, thus introducing an inherent amplitude and phase mismatch. Therefore, we choose the same 2:2 transformer footprint to keep the impedance conversion ratio symmetric. The parasitic coupling between the primary and secondary windings of the power combiner is minimized via layout optimization. It reduces the ratio of direct subharmonic coupling to the PA output, as it would have undermined the efficacy of subharmonic cancellation otherwise. To make it symmetric, the secondary coil of each PA bank always connects from the top side and connects to the adjacent channel. The coupling between the primary and secondary coils is balanced. Note that additional calibration circuitry is implemented to balance the asymmetric output trace of the transformer. The three-way power combiner is modeled and simulated in HFSS (see Fig. 12). It shows less than 2-dB insertion loss over 1-GHz bandwidth (see Fig. 13).

C. Multi-SHS PM Generator

To generate the multi-SHS waveform, we use three local PM generators to create three different subharmonics,

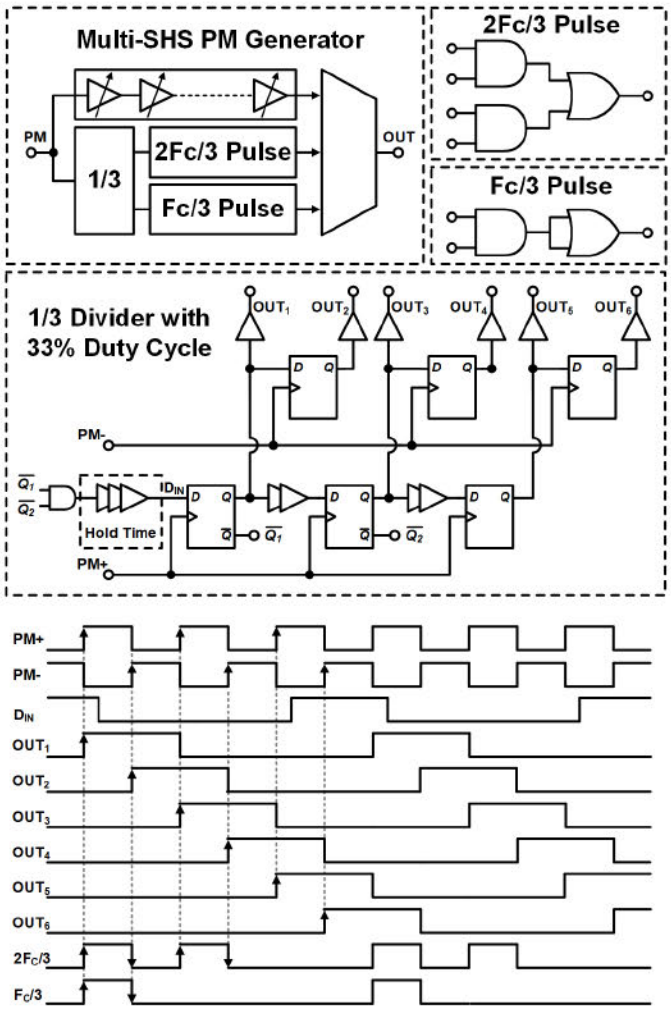

Fig. 14. Multi-SHS phase generator.

Fc, 2Fc/3, and Fc/3. The same Fc signal is distributed to three PM generators. For each PM generator shown in Fig. 14, it contains a one-third divider, Fc/3 pulse generator, 2Fc/3 pulse generator, tunable delay line, and output MUX. The one-third divider first generates the Fc/3 signals from OUT_1 to OUT_6, which have a 33% duty cycle with six different phases. The 2Fc/3 pulse generator and Fc/3 pulse generator will create the 2Fc/3 and Fc/3 subharmonics, respectively. The tunable delay line delays the original PA signal to align with these subharmonics. The layout is balanced for each building block to reduce the phase skew between different channels. The output MUX selects the desired phase and sends to each PA unit cell. The tunable delays are implemented to calibrate the subharmonics mismatch, which is described in Section II.

V. Measurement

The phase-interleaved multi-SHS PA prototype is implemented in the 65-nm bulk CMOS process with a die size of 3 mm × 2.4 mm (Fig. 15). The chip is directly mounted on the PCB to minimize the bond wire inductance to the PA supplies. The PA pre-drivers operate from 0 to 1.2 V. The PA output drivers are powered by either 2.4 or 3.6 V, as described previously, i.e., $2V_{DD}$ and $3V_{DD}$, respectively.

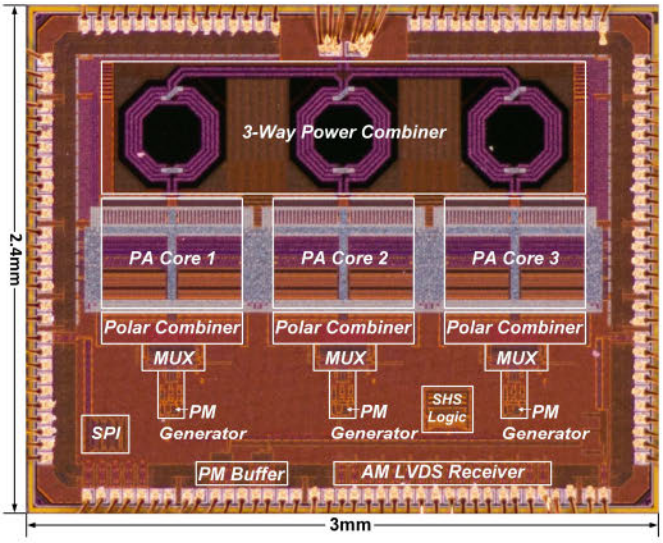

Fig. 15. Chip micrograph.

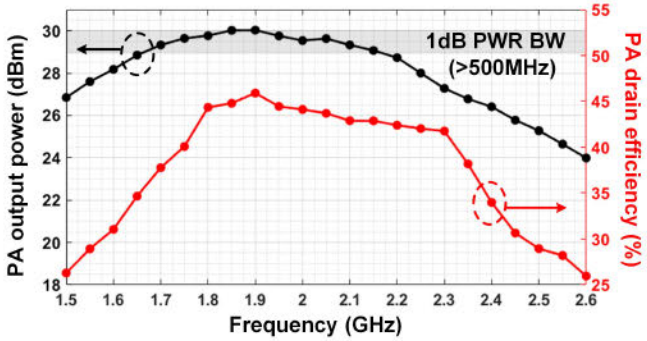

Fig. 16. Measured PA output power and efficiency over the frequencies.

To test this digital PA, we send the 12-bit PM digital code to an off-the-shelf evaluation board (AD9779) for generating the phase-modulated signal. With technology scaling, additional bits could be implemented to pursue higher linearity.

A. Continuous Wave Test

We first characterize the PA peak performance by measuring the PA peak output power (Psat) and the peak DE. The measured results under different frequencies are shown in Fig. 16. The measured PA peak output power and efficiency are 30 dBm and 45.9%, respectively, for a center frequency of 1.9 GHz. The measured 1-dB power bandwidth is more than 500 MHz. The efficiency is more than 40% between 1.8 and 2.3 GHz. The reported DE includes all the phase generators, polar combiners, level shifters, pre-drivers, output stages, and the transformer-based power combiner.

Figs. 17 and 18 show the measured PA back-off efficiency under different output power levels. Compared to the simulation results, the efficiency is around 10% lower than the measurement results. There is a total of five efficiency peaks due to the pre-compiled multi-SHS with hybrid class-G operation LUT, as described in Section III. At 1.9 GHz, the five efficiency peaks are located at 0, −3.5, −7.0, −9.5,

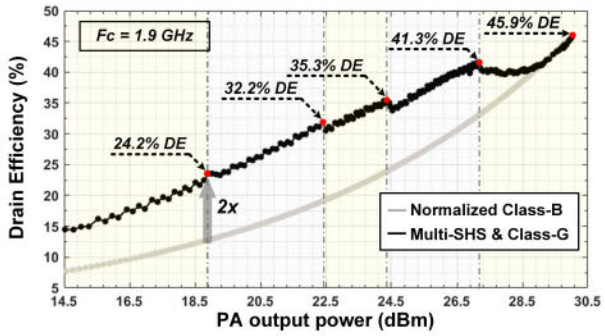

Fig. 17. Measured PA DE at 1.9 GHz versus PA P_{out}.

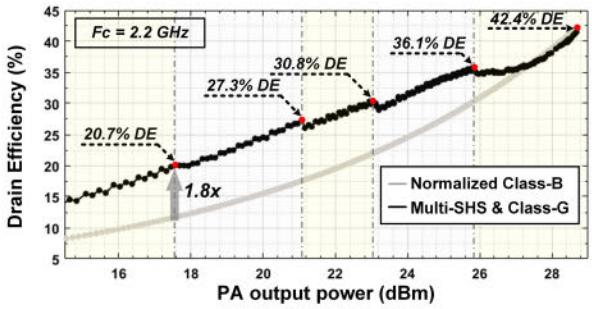

Fig. 18. Measured PA DE at 2.2 GHz versus PA P_{out}.

and −12 dB, indicating 45.9%/41.3%/35.3%/32.2%/24.2% output DE. The measured power efficiency improves as much as twofold at −12-dB PBO over the normalized class-B PA. At 2.2 GHz, a similar efficiency roll-off curve has been observed. The five efficiency peaks located at 0, −3.5, −7.0, −9.5, and −12 dB indicate 42.4%/36.1%/30.8%/27.3%/20.7% output DE. The measured power efficiency improves as much as 1.8X at −12-dB PBO over the normalized class-B via the proposed architecture. Note that the measurement shows that the efficiency peaks are not exactly located at the theoretical PBO points. For example, the last efficiency peak is located at −12-dB PBO. However, the theoretical results indicate −13-dB PBO. The reason for this offset is that the PA output saturates when the output power is high. It makes all the PBO efficiency points move closer to the peak point, which leads to −12 dB in this case. The efficiency roll-off curve is based on the pre-calculated LUT, using MATLAB simulation results, which yield the best efficiency among all the other combinations.

The AM–AM and AM–PM non-linearities at 1.9 GHz are shown in Figs. 19 and 20. They were measured by sweeping the amplitude codes. Note that the input code in Fig. 20 is flipped compared to the AM–AM characteristic curve. There is a wiggle shown in the AM–PM curve because of the non-linearity from the different PBO region of the PA operation, which matches the hybrid operation. Note that the AM–PM non-linearity is relatively large compared to that in other work [24]. One potential reason is that the watt-level PA cell yields a larger footprint, which leads to larger mismatch. This issue can be mitigated by technology scaling and better layout techniques. The discontinuities in AM–PM happened when the

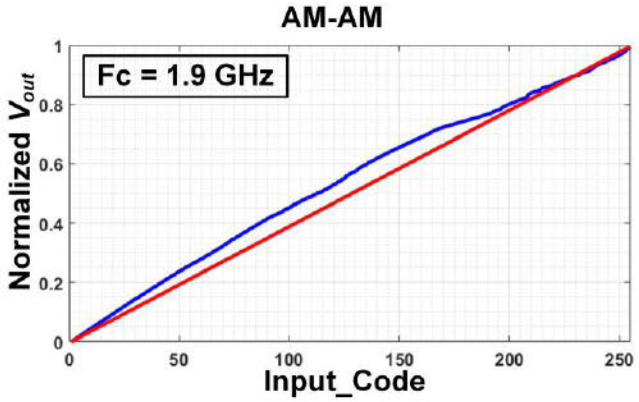

Fig. 19. Measured AM–AM characteristic curve at 1.9 GHz.

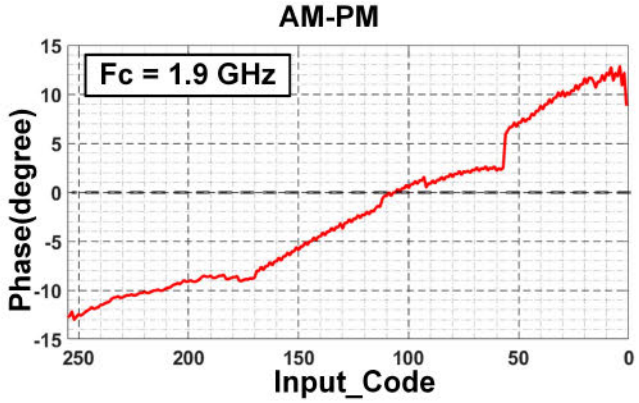

Fig. 20. Measured AM–PM characteristic curve at 1.9 GHz.

PA switches to different PBO regions under the synthesized LUT, e.g., switching from $3V_{DD}$ to $2V_{DD}$ due to the hybrid class G operation. The AM–AM and AM–PM characteristic curves are used to create pre-distorted input digital patterns for the dynamic measurement. The chip has been tested under different voltage and temperature corners. When the temperature increases from 25° to 100°, the AM–PM variation is around 5°. The AM–PM non-linearities with 1-, 1.2-, and 1.4-V supplies become 21°, 25°, and 35°, respectively.

B. Phase-Interleaved Subharmonic Cancellation

To validate the proposed phase-interleaved operation, we measured the worst case spur under multi-SHS with a hybrid class-G operation. In this case, all the PA cells toggle at the Fc/3 with the $2V_{DD}$ supply. In Fig. 21, all the PA cells first toggle at Fc/3 with zero phase difference. Although the matching network provides a bandpass shape at the carrier frequency, the attenuation is not sufficient to suppress all the spurs. The output spectrum shows large unwanted tones located at Fc/3 and 2Fc/3.

The effectiveness of performing subharmonic cancellation in the phase-interleaved scheme is shown in Fig. 21. In this case, the three interleaved PA channels toggle at Fc/3 with 120° apart. Only the Fc component is aligned in phase, while the phases of the unwanted Fc/3 and 2Fc/3 components are theoretically canceled. As we can see from the output

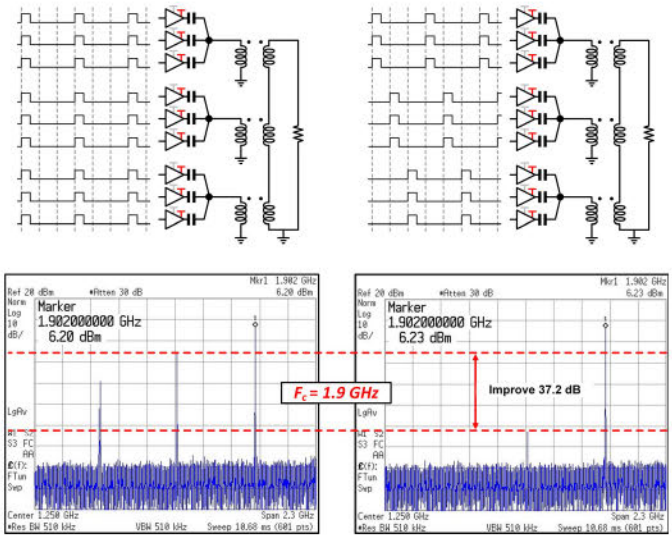

Fig. 21. Measured PA output spectrum at −13-dB PBO for in-phase and phase-interleaved subharmonic operation with all the PA cells toggle at Fc/3.

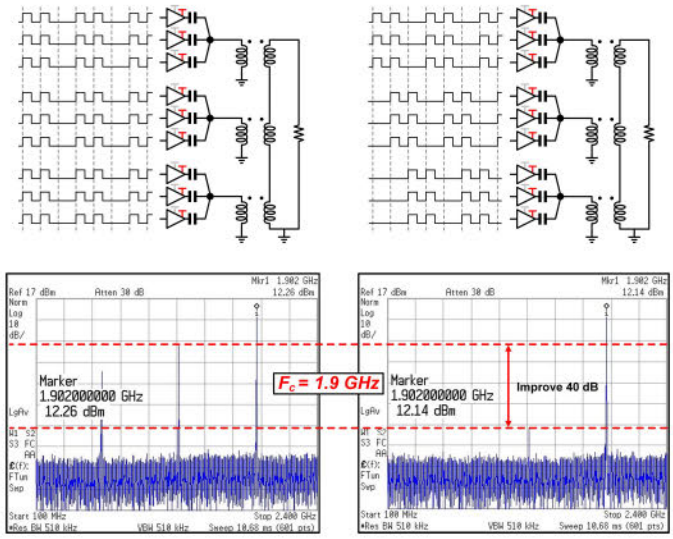

Fig. 22. Measured PA output spectrum at −7-dB PBO for in-phase and phase-interleaved subharmonic operation with all the PA cells toggle at 2Fc/3.

spectrum, the output power at the carrier frequency remains the same. The worst case spur is reduced by 37.2 dB, limited by the matching property between the phase-interleaved paths. The difference between the desired tone and the largest unwanted subharmonic is around 50 dB, which satisfies the mask requirement of most communication standards. Fig. 22 shows all the PA cells toggle at 2Fc/3. Similar to the Fc/3 case, the worst case spur is reduced by 40 dB, achieving 58-dB SFDR. Due to the large output power, the EMI/EMC requirement may be violated. Antenna with frequency selectivity can be implemented to provide additional attenuation.

C. Dynamic Measurement

The dynamic performance of the PA is evaluated using a 5-MHz, 52 sub-carrier, 16-QAM OFDM signal with a 7.2-dB PAPR. As noted, the PA is first pre-distorted by AM–AM and

TABLE I
PERFORMANCE COMPARISON WITH OTHER CMOS PAs

Specifications		This work		[36] D. Cousinard ISSCC 2017	[37] V. Vorapipat ISSCC 2017	[38] S. Hu ISSCC 2015	[39] K. Onizuka ISSCC 2013	[40] P. A. Godoy JSSC 2012	[11] S. Yoo JSSC 2019	[41] R. Bhat JSSC 2017	[42] W Tai JSSC 2012
Architecture		Watt Level SHS PA		CMOS PAs with Efficiency Enhancement Techniques					CMOS PAs with Watt Level Output Power		
Process	[nm]	65		28	45	65	65	65	65	65	45
Frequency	[GHz]	1.9	2.2	2.45	3.5	3.71	1.8	2.4	2.2	2.2	2.4
Max P_{out}	[dBm]	**30**	**28.7**	28.2	25.3	26.7	27.2	27.7	30.1	30.3	31.5
Peak DE	[%]	**45.9**	**42.4**	39	30.4‡	40.2	30	45.1‡	37‡	34‡	27‡
-3.5 dB DE	[%]	**41.3**	**36.1**	33*	26‡, *	32.5*	24‡, *	39‡, *	30‡, *	24‡, *	22‡, *
-7 dB DE	[%]	**35.3**	**30.8**	23*	23‡, *	35*	19‡, *	37‡, *	25‡, *	18‡, *	17‡, *
-9.5 dB DE	[%]	**32.2**	**27.3**	18*	19‡, *	31.5*	14‡, *	24‡, *	17‡, *	14‡, *	14‡, *
-12 dB DE	[%]	**24.2**	**20.7**	14*	17.4‡	26.2	9‡, *	22‡, *	12‡, *	9‡, *	12‡, *
PAPR	dB	7.2		5.7	6.3	5.8	5.9	7.5	7.6	6.5	6.7
Average DE	[%]	**31.4†**		30	24‡	28.8	18‡	27.6‡	18.3‡	16‡	16‡
Power Supply	[V]	2.4/3.6		2.2	1.2/2.4	3/1.65	3.3	2.5/1.8/ 1.35/0.85	2.5/1.2	2.6	2.4
EVM	[dB]	-24.7†		-25	-35.8	-24	-22	-31.4	-40.3	-30	-25
Modulation		16QAM OFDM 5MHz		64QAM OFDM 20MHz	256QAM OFDM 20MHz	16QAM SC 1MHz	64QAM OFDM 20MHz	64QAM OFDM 20MHz	256QAM SC 20MHz	64QAM SC 1.4MHz	64QAM OFDM 20MHz
Matching Network		On-Chip		On-Chip	On-Chip	On-Chip	On-Chip	Off-Chip	On-Chip	On-Chip	On-Chip
PBO Efficiency Enhancement Tech		Multi-SHS /Class-G		Polar/PWM	Doherty/ Class-G	Doherty/ Class-G	Supply Switching	AMO	IQ Shared/ Class-G	-	Current Switching

*Estimated from reported figures
SC: Single Carrier
‡Reported power added efficiency (PAE)
†Measured at center frequency 1.9GHz

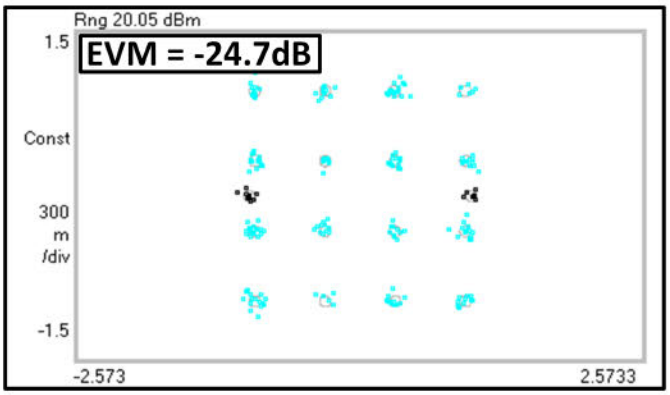

Fig. 23. Measured EVM for real-time multi-SHS and hybrid class-G operation.

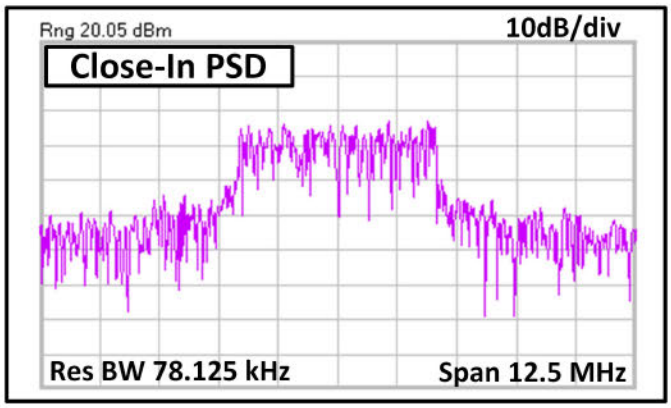

Fig. 24. Measured spectrum for real-time multi-SHS and hybrid class-G operation.

AM–PM LUTs. The average drain efficiency achieves 31.2% under real-time digital pre-distortion (DPD) operation (i.e., transmitting the modulated signal under the complied LUT operation).

The PA in-band and out-of-band linearities have been characterized. It achieves 22.8-dBm average power with an EVM of −24.7 dB (see Fig. 23). Fig. 24 shows the measured close-in PSD characteristics. The ACPR is −26.5 dBc before calibration and −35-dBc after calibration. The poor linearity is mainly because of the memory effect when the PA generates large output power. The poor linearity can be improved by reducing the output power level or using advanced DPD and memory effect calibration [25]–[35].

Table I summarizes the measured performance compared to other state-of-the-art CMOS PAs with different PBO efficiency-enhancement techniques [11], [36]–[42]. The PA prototype delivers 30-dBm peak output power with a 45.9% peak DE at 1.9 GHz. Table I shows a comparison of the DE at 0-, −3.5-, −7.0-, −9.5-, and −12-dB PBO, where the PA prototype shows improved deep PBO efficiency. Compared to other CMOS watt-level PAs, the efficiency improvement is even more significant, where real-time multi-SHS with hybrid class-G operation in this work achieves 31.4% average DE.

VI. CONCLUSION

This article presents a watt-level phase-interleaved multi-SHS digital PA. A phase-interleaved structure is demonstrated

for inherent subharmonic cancellation. To achieve watt-level output power, stacking PA drivers and power combining techniques are implemented. Multi-SHS is proposed to enhance PBO efficiency. Multi-SHS can be combined with hybrid class-G to further improve the average efficiency. The PA prototype enables watt-level peak output power with good PBO efficiency compared to the state-of-the-art CMOS PAs.

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