4.1 A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier Achieving 31.4% Average Drain Efficiency

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Modern wireless communication systems often utilize spectrum-efficient modulation schemes for higher data throughput, given the finite bandwidth. This type of modulation schemes, such as Orthogonal Frequency Division Multiplexing (OFDM), results in a high peak-to-average power ratio (PAPR) for the transmitted signal. Therefore, power amplifier efficiency in the power back-off (PBO) region has become an important design target. Meanwhile, obtaining high output power and high average efficiency still remains a key design challenge when developing an integrated CMOS PA. Recently, a subharmonic switching (SHS) digital PA architecture was reported in [1]. It toggles the PA cell at the subharmonic component of the carrier frequency (Fc) to achieve power back-off. The slower toggling rate reduces dynamic and conduction loss in the switching PA, resulting in better PBO efficiency. However, the SHS PA requires additional notch filtering of the subharmonic components in the matching network. Therefore, we propose a phase-interleaved architecture that combines three SHS PAs to increase output power (Watt-level) and inherently cancel the subharmonic components in the PBO mode, thereby alleviating the burden of the matching network. Moreover, multiple subharmonic components are utilized to create a greater number of efficiency peaks in the PBO region. This is referred to as a multi-SHS scheme. Lastly, a hybrid Class-G operation, in combination with the multi-SHS scheme, is used to further enhance average efficiency.

In the proof-of-concept prototype, a switched-capacitor (SC) PA [2] is employed as the baseline structure for digital-to-analog conversion. As shown in Fig. 4.1.1, the conventional SC PA utilizes the capacitor network to perform voltage division at the PA output, leading to power back-off. However, due to charge redistribution, the charge stored on the capacitor is lost, degrading PBO efficiency. The key idea of the SHS PA is to toggle the PA cells at a certain subharmonic frequency when the PA operates in the PBO region, e.g., Fc/3 (Fig. 4.1.1), where Fc is the carrier frequency, and to use the third harmonic component to carry the signal information, leading to PBO of -9.5dB in this particular case. Since all PA cells toggle together, dynamic charge loss in the switched capacitor bank is avoided. However, to remove the subharmonic components at the output spectrum, a notch response must be added to the matching network at subharmonic frequencies, thus incurring overhead.

The key concept of the proposed phase-interleaved architecture is to deploy an array of SHS PAs and balance the phases of their digital input waveforms in the PBO region, i.e. 120 degrees apart for the three interleaved PA channels. Accordingly, only the Fc component is aligned in phase, while the phases of the unwanted Fc/3 and 2Fc/3 components are inherently cancelled on the primary side of the transformer without additional loss (Fig. 4.1.1). Realistically, the effectiveness of the nullification depends on how well the phase and magnitude between the PA channels could be matched. This prototype is demonstrated to achieve more than 50dB subharmonic attenuation, given the extra design efforts in balancing it. It is noteworthy that, in the peak-output mode, the three PAs continue to operate at the carrier frequency (Fc), using the same input phases for power combining. In other words, phase-interleaved input is only applied when specific PA cells operate in subharmonic switching mode.

The key idea of multi-SHS is to use multiple subharmonic components for creating a greater number of efficiency peaks at PBO, in this case both Fc/3 and 2Fc/3 subharmonic components are used. Additionally, dual-power supplies (3VDD and 2VDD) are used in conjunction with the multi-SHS operation to create a total of five efficiency peaks located at various PBO points, i.e. 0dB, -3.5dB, -7dB, -9.5dB, and -13dB (Fig. 4.1.2). It is worth mentioning that phase balancing for the 2Fc/3 peak results in non-uniform toggling waveforms for each PA channel. By gating off every third cycle, the phases are balanced and hence the unwanted subharmonic components are rejected, which also leads to additional efficiency peaking at -7dB PBO. For the actual implementation, efficiency between peaks is further optimized by combining the different subharmonics and power supplies simultaneously in the individual PA cells.

When devising guidelines for the design, it is important to ensure that 1) the same number of PA cells are within each PA channel toggle for the same subharmonic component (either Fc/3 or 2Fc/3) in order to maintain equivalent transformer input impedance seen by each PA channel and 2) the input phases for the corresponding PA cell in each channel should always be balanced while operating in subharmonic mode. In that way, the PBO efficiency can be maximized while unwanted frequency components can be rejected.

The block diagram for the overall implementation of the PA is shown in Fig. 4.1.3. An external phase-modulated (PM) signal is used to generate phase-interleaved subharmonic components (Fc/3 and 2Fc/3), as well as the delayed PM signal via on-chip circuitry, including frequency dividers and delay lines. A high-speed multiplexer selects the correct PM signal for each PA cell, based on the corresponding amplitude code. The synthesized decoder converts the eight-bit amplitude code into a set that comprises amplitude, multi-SHS, and dual-power supply control words for each PA channel, based on the aforementioned switching rules for PBO efficiency enhancement. The output power of each PA channel can be tuned by making changes to the non-overlapping clock phase. A triple-stacked Class-D output driver is designed to enlarge the output voltage swing and lower the resultant impedance transformation ratio. Based on the hybrid operation, the pull-up path of the Class-D output driver selects either 3VDD (3.6V) or 2VDD (2.4V). This helps to reduce the power loss in the matching network and yield less efficiency degradation due to routing resistance.

A two-turn-transformer-based power combiner was designed to combine the power of the PA with subharmonic cancellation. A symmetric three-way power combiner layout was designed to balance the coupling factor for each PA channel, hence maintaining effective subharmonic cancellation. Parasitic coupling between the primary and secondly winding of the power combiner is minimized to reduce the ratio of direct subharmonic coupling to the PA output as it would have undermined the efficacy of subharmonic cancellation otherwise. The layout strategy used for the power combiner and the associated HFSS EM simulation results for insertion loss are shown in Fig. 4.1.3.

The proof-of-concept prototype is implemented in 65 nm CMOS as shown in Fig. 4.1.4. The PA delivers 30dBm peak output power with 45.9% drain efficiency at 1.9GHz and 28.7dBm peak output power with 42.4% drain efficiency at 2.2GHz. The proposed wideband three-way power combiner achieves a 3dB bandwidth of >500MHz. Figure 4.1.4 shows PA efficiency against different PBO levels, at both 1.9GHz and 2.2GHz. Five efficiency peaks are achieved in the PBO region after combining multi-SHS and hybrid Class-G operation. The last efficiency peak (24.2% drain efficiency) occurs at a -12dB PBO level (1dB PBO level offset due to peak power saturation), demonstrating 2× improvement compared with a normalized Class-B PA, which can benefit high PAPR modulation signal. Note that the multi-SHS scheme also helps to improve PBO efficiency between the five peaks. The AM-AM and AM-PM responses are measured for digital pre-distortion (DPD). The dynamic performance of the PA is evaluated using 5MHz 16-QAM OFDM signal. It achieves 22.8dBm average power with error vector magnitude (EVM) of -24.7dB and an adjacent channel power ratio (ACPR) of 35dBc. The average drain efficiency achieves 31.2% under real-time DPD operation using a 7.2dB PAPR modulated signal. The performance of our PA prototype is compared with that of prior-art CMOS PAs [3-8] (Fig. 4.1.6). The proposed architecture achieves superior PBO efficiency and compares favorably with the published Watt-level RF CMOS PAs in Fig. 4.1.6. Figure 4.1.7 shows a micrograph of the test chip.

Acknowledgements:
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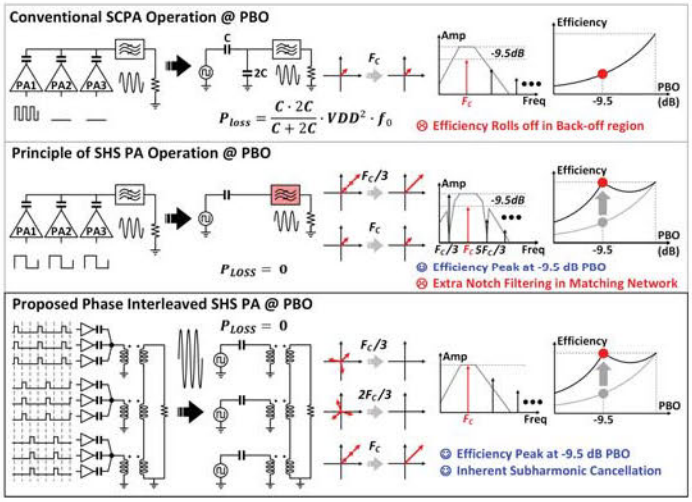

Figure 4.1.1: Proposed phase-interleaved architecture for the SHS PA in a PBO region.

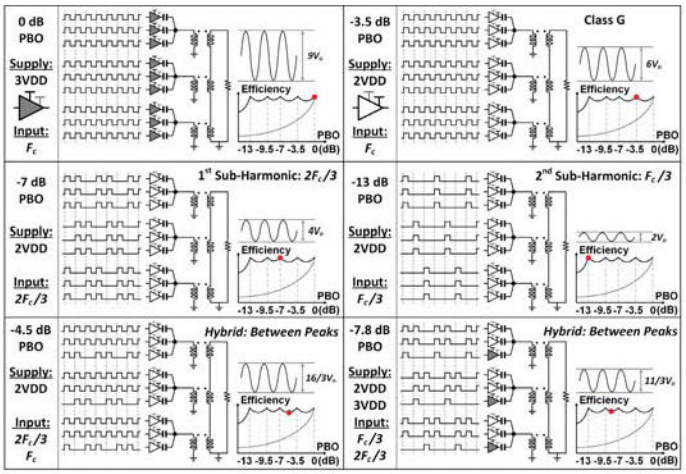

Figure 4.1.2: Hybrid operation modes for combining multi-SHS and dual power supplies.

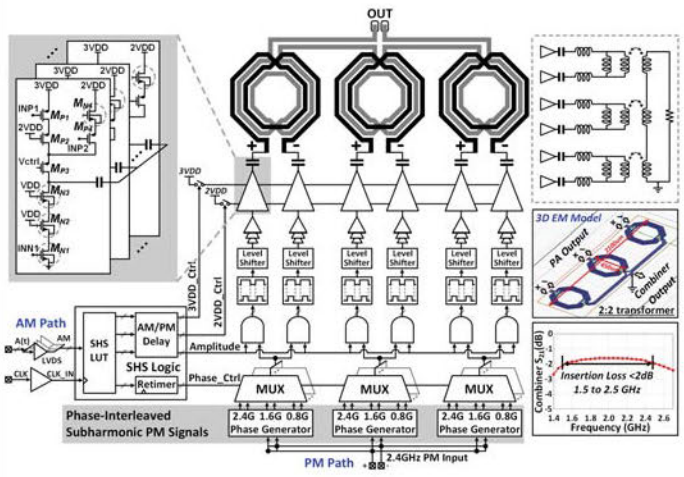

Figure 4.1.3: Simplified block diagram of the PA prototype. Here, $3V_{DD}$=3.6V and $2V_{DD}$=2.4V.

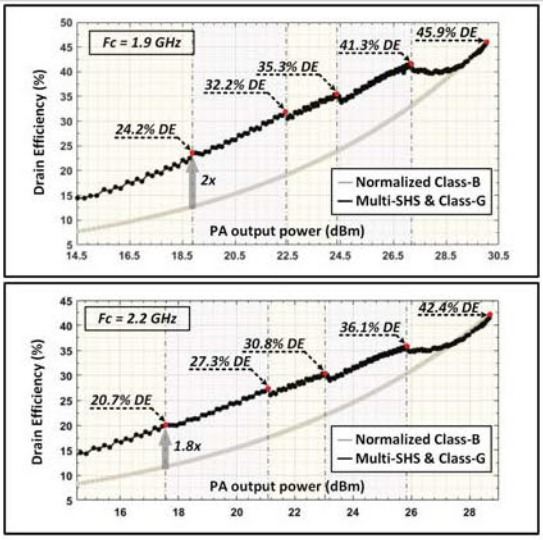

Figure 4.1.4: Measured drain efficiency using a CW signal at different PBO levels at 1.9GHz and 2.2GHz.

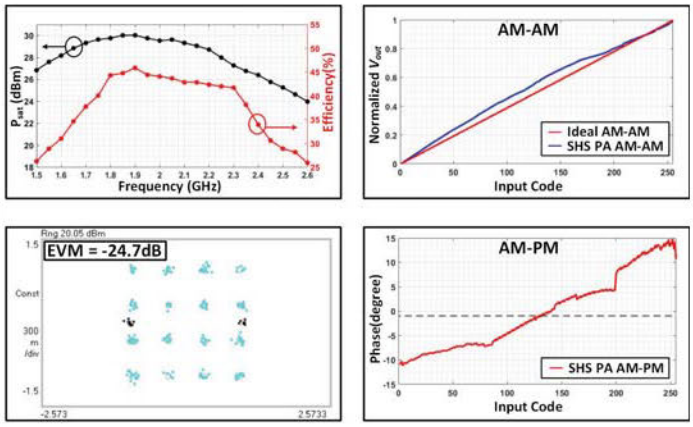

Figure 4.1.5: Measured EVM using 16-QAM OFDM signal with 7.2dB PAPR, AM-AM, AM-PM and peak static performance.

Specifications		This work		[3] ISSCC 2017	[4] ISSCC 2017	[5] ISSCC 2015	[6] ISSCC 2013	[7] JSSC 2012	[8] JSSC 2012
Process	[nm]	65		28	45	65	65	65	45
Frequency	[GHz]	1.9	2.2	2.45	3.5	3.71	1.8	2.4	2.4
Max P_{out}	[dBm]	30	28.7	28.2	25.3	26.7	27.2	27.7	31.5
Peak DE	[%]	45.9	42.4	39	30.4‡	40.2	30	45.1‡	27‡
-3.5 dB DE	[%]	41.3	36.1	33*	26‡, *	32.5*	24‡, *	39‡, *	22‡, *
-7 dB DE	[%]	35.3	30.8	23*	23‡, *	35*	19‡, *	37‡, *	17‡, *
-9.5 dB DE	[%]	32.2	27.3	18*	19‡, *	31.5*	14‡, *	24‡, *	14‡, *
-12 dB DE	[%]	24.2	20.7	14*	17.4‡	26.2	9‡, *	22‡, *	12‡, *
PAPR	dB	7.2		5.7	6.3	5.8	5.9	7.5	6.7
Average DE	[%]	31.4†		30	24‡	28.8	18‡	27.6‡	16‡
EVM	[dB]	-24.7†		-25	-35	-24	-22	-31.4	-25
Matching Network		On-Chip		On-Chip	On-Chip	On-Chip	On-Chip	Off-Chip	On-Chip
PBO Efficiency Enhancement Tech		Multi-SHS /Class-G		Polar/PWM	Doherty/ Class-G	Doherty/ Class-G	Supply Switching	AMO	Current Switching

*Estimated from reported figures
‡Reported Power Added Efficiency (PAE)
†Measured at center frequency 1.9 GHz

Figure 4.1.6: Comparison with prior-art CMOS PAs with PBO efficiency enhancement.

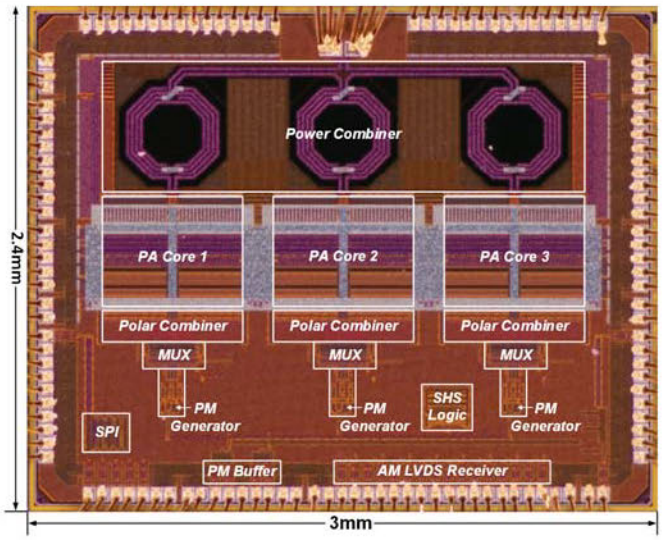

Figure 4.1.7: Die micrograph.

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