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To cite this article: Yaoxu Chen *et al* 2019 *Nanotechnology* **30** 394002

IOP Publishing Nanotechnology
Nanotechnology 30 (2019) 394002 (12pp) https://doi.org/10.1088/1361-6528/ab2853

Electrochemically triggered degradation of silicon membranes for smart on-demand transient electronic devices

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Received 3 April 2019, revised 9 May 2019
Accepted for publication 10 June 2019
Published 15 July 2019

Abstract

Transient electronics is an emerging technology that enables unique functional transformation or the physical disappearance of electronic devices, and is attracting increasing attention for potential applications in data secured hardware as an ultimate solution against data breaches. Developing smart triggered degradation modalities of silicon (Si) remain the key challenge to achieve advanced non-recoverable on-demand transient electronics. Here, we present a novel electrochemically triggered transience mechanism of Si by lithiation, allowing complete and controllable destruction of Si devices. The depth and microstructure of the lithiation-affected zone over time is investigated in detail and the results suggest a few hours of lithiation is sufficient to create microcracks and significantly promote lithium penetration. Finite element models are proposed to confirm the mechanism. Electrochemically triggered degradation of thin film Si ribbons and Si integrated circuit chips with metal-oxide-semiconductor field-effect transistors from a commercial 0.35 micrometer complementary metal-oxide-semiconductor technology node is performed to demonstrate the potential applications for commercial electronics. This work opens new opportunities for versatile triggered transience of Si-based devices for critical secured information systems and green consumer electronics.

Supplementary material for this article is available online

Keywords: transient electronics, silicon membranes, triggered transience, on-demand electronics, lithiation

(Some figures may appear in colour only in the online journal)

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1. Introduction

Modern commercially available electronic devices are typically designed to offer a robust and reliable operational characteristic. The emergence of electronics systems built on water-soluble materials capable of complete physical transience enables novel properties that cannot be addressed by conventional devices. Such type of electronics is referred to as transient electronics, and is attracting growing interest for bioresorbable medical implants, green consumer electronics, and data secured hardware [1–7]. For scenarios where data security is of high priority, such as healthcare facilities, business organizations, government institutions, and the military, conventional software encryption could be easily cracked and might not guarantee successful defense against data breaches. Compete on demand destruction of the hardware (e.g. memory device) represents an alternative ultimate solution for data security, to avoid stealing confidential information as well as critical chip design. Consequently, there is an increasing demand for specially designed non-recoverable transient electronics that would completely lose their functions or physically disappear with on-demand expectation [8–10].

Research on transient electronics are focused on water-soluble semiconductors, metals, dielectrics, substrates, and encapsulation materials [1, 11–20]. Semiconductors, especially silicon (Si), hold a critical role in the widely used high-performance complementary metal-oxide-semiconductor (CMOS) devices for logic and memory applications. To achieve advanced non-recoverable on-demand transient electronics for data secure hardware and consumer electronics, it is critical to leverage the existing manufacturing infrastructure for Si integrated circuits and explore novel triggered degradation modalities of Si. Extensive studies on the hydrolysis of Si nanomembranes in aqueous solutions have been reported, and the dissolution rates are in the range of 0.01–398.11 nm day^{-1}, depending on the type of solution, temperature, pH, and the doping level of Si [2, 6, 12, 21, 22]. Nevertheless, further acceleration of the dissolution rates remains a challenge. In some scenarios, the on-demand accelerated degradation of Si is desirable for fast self-destruction. However, due to the chemical stability of monocrystalline Si, only a few works have been reported on the triggered transience of Si circuits [8–10, 23]. The demonstrated triggered degradation of a Si-based device involves either substrate stress-induced physical disintegration or accelerated chemical reactions. Stress-induced disintegration of a Si device upon heat triggering of the expandable polymeric substrates has been reported [10], which however might fail to completely destruct devices into sufficiently small pieces and risks for data recovery still exist. Accelerated chemical reactions can be induced by initiating combustion [23] or releasing harsh chemicals (NaOH, KOH, hydrofluoric acid (HF), and buffered hydrofluoric acid from microfluidic reservoirs upon electrical triggering [8, 9, 23]. Nevertheless, the stability of long-term preservation of the exothermic energy release agent or chemical etchants in reservoirs may restrict potential applications.

To address the above issues, we present a novel electrochemically triggered transience of Si-based electronics by introducing lithiation of the Si layer, which can lead to both physical disintegration and chemical modification of the Si component that could completely eliminate potential device recovery. Si is a well-known attractive anode material for Li-ion batteries due to its high theoretical specific capacity (3579 mAh g^{-1}) [24]. However, the insertion of Li-ions into Si will cause a significant volume change of ~280% at full capacity, and the resulting fracture of Si poses a major challenge to the cycling life of a lithium-ion battery with a Si anode (Li-Si battery). Various Si nanostructures, such as spheres [25], nanowires [26], and nanomembranes [27], have therefore been proposed to relax the lithiation-induced stress [28]. By contrast, instead of making efforts to reduce the stress on the lithiation of Si, utilizing lithiation could contribute to the on-demand accelerated Si degradation for transient electronics. Due to the good controllability of electrochemical reactions and the maturity of lithiation devices (e.g., lithium-ion battery), the lithiation-induced triggered transience could possess better stability, controllability, and a robust destructive power compared with the reported substrate stress-induced disintegration or the accelerated chemical reactions induced by combustion or harsh chemicals. If combined with subsequent reaction with moisture or water in the atmospheric environment, complete disappearance of the Si component is possible as the Li_xSi alloy resulting from lithiation is highly reactive.

In this work, the depth of lithiated regions as a function of time in monocrystalline Si membrane is investigated, and a vein-like network of Li_xSi layer develops after 9 h of lithiation which greatly accelerates the lithiation-affected area. The evolution of the morphology could be caused by the propagation of microcracks generated from lithiation-induced stress and the hypothesis is confirmed by finite element models. The real-time observation of the lithiation of Si thin film ribbons reveals buckling and fracture phenomenon at various stages of lithium-ion insertion. Electrochemically triggered transience of a thin film Si integrated circuit (IC) chip with metal-oxide-semiconductor field-effect transistors (MOSFETs) from a commercial 0.35 μm CMOS technology node with a 7 nm gate oxide is demonstrated, suggesting potential applications for commercial electronics. The proposed novel on-demand accelerated degradation of Si device opens up new opportunities for versatile triggered transience modalities of Si-based electronics that can be used for critical secured information systems and green consumer electronics.

2. Method

2.1. Lithiation testing structure assembly of Si wafer samples

Double-side polished Si wafer (p-type boron-doped, 100, 500 μm, 0.001–0.01 ohm cm, LIJINGKEJI, Inc) served as the working electrode. The wafer was cleaned with acetone, isopropanol, and deionized water and then cut into pieces with a size of 5 × 5 mm. The Si samples were adhered to Cu foil with sliver paste (DJ 002, Hong Kong Welsolo Metal

Technology Co., Ltd), dried at 130 °C for 20 min, and then assembled into a CR2032 coin cell with Li as the counter electrode. The electrolyte was prepared by mixing 1 mol l^{-1} of $LiPF_6$ in ethylene carbonate (EC) + diethyl carbonate (DEC) (1:1 by volume). Upon assembly, the silicon sample was lithiated at a constant current density of 400 μA cm^{-2} for different period of times and then removed from the cell for further characterization. All assembly and disassembly processes were carried out inside a glove box filled with high-purified argon (Ar) gas to prevent a reaction with ambient air.

2.2. Auger electron spectroscopy (AES) characterization

After disassembly, the lithiated Si samples were washed in DEC twice and dried for 5 min. Then, the samples were transferred to the AES system (PHI-700, ULVAC-PHI, Inc.) with a sealed transfer vessel which was filled with highly purified Ar gas to avoid exposure to ambient air. The analysis was carried out at 5 kV/5 nA. The energy resolution could be as low as 0.1% and spatial resolution is less than 6 nm. AES depth profiles were obtained by using argon-ion (Ar^+) sputtering with a sputtering rate of 11 nm min^{-1} for the standard sample (SiO_2). As sputtering at high energy may lead to damage of the sample surface, the AES results will be inaccurate in the elemental analysis of the internal position of the sample after a long sputtering time. The sputtering time is therefore always maintained at less than 400 min in our work. The intensities of the C KLL (I_C), O KLL (I_O), Li KLL (I_{Li}), and Si LVV (I_{Si}) transitions are measured after 3, 6, and 9 h of lithiation. It is noted that a KLL transition indicates that the Auger electron was ejected from the L shell resulting from the energy released by an L shell electron filling a K shell hole created by the electron beam. A similar process also applies for the LVV transition. The same Si sample after 9 h of lithiation was tested twice on adjacent regions. To minimize the mutual interference of the analysis of adjacent regions, the sample is cut into two separate pieces for Auger measurement. In our work, I_C, I_O, I_{Li}, and I_{Si} were measured at the peak energy of 275, 570, 57, and 1621 eV, respectively.

2.3. Surface morphology and microstructure characterization

For the characterization of the microstructure of the lithiated Si samples, similar procedures were followed for disassembly and surface cleaning as those used for AES characterization. The samples were transferred into the focused ion beam-scanning electron microscope (FIB-SEM) system (Crossbeam 340, Carl Zeiss, Inc) from a glove box in a sealed vessel to avoid exposure to ambient air. Over 1 μm of platinum was deposited before FIB milling for the protection of the sample surface. For rough raster, FIB milling was carried out at 30 kV/300 pA. Then, the samples were further polished at 30 kV/30 pA at the final step to minimize the potential damage. Surface morphology characterization was also performed in a scanning electron microscopy (SEM) system (JSM-6700F, JEOL Ltd). As for the *in situ* optical observation of Si membrane ribbons during lithiation, the optical images were taken every 30 min in the same position with an optical microscope (Nikon, Eclipse CI) and a digital camera (Nikon, DS-U3).

2.4. Fabrication of Si thin film ribbons

The fabrication of Si ribbons followed a similar procedure as that reported for the fabrication of Si microstructure arrays and Si thin film electrodes [27, 29]. The Si ribbons were derived from the top layer of a silicon on insulator (SOI) wafer (p-type, boron-doped, 100, 0.005–0.01 ohm cm, Ice-MOS Technology Ltd). The thicknesses of the device layer, buried oxide layer, and handle layer are 2, 1.5, and 500 μm, respectively. Photoresist (SPR 220) was spin-casted onto the device layer, and then ribbons (500 μm in width, 10 mm in length) with rows of holes (50 μm in diameter) were patterned through contact-mode photolithography. Rows of holes were made to assist in the subsequent HF undercut process. The Si in the unprotected regions were removed through reactive ion etching (RIE) (SF_6 = 150 sccm, 88 mTorr, 100 W, 160 s for 2 μm thick of Si) and the buried oxide layer was exposed consequently. The SOI was briefly etched in hydrofluoric acid (49%) for 15 min, in order to remove SiO_2 not only in the exposed regions but also in the narrow regions beneath the edge of the ribbons. Afterwards, the photoresist (SPR 220) was spin-coated again to fill the place of the formerly removed SiO_2 and only the photoresist on the surface not covered by the Si ribbons was exposed to UV light and removed in the subsequent developing process. The photoresist beneath the edge of the Si ribbons served as anchors and supports during the HF undercut process. The remaining SiO_2 in the buried oxide layer was entirely etched in HF (49%) for 5 h during the undercut process. A slice of poly(dimethylsiloxane) (PDMS, 12 × 4 mm, 1 mm in thickness) was contacted against the Si ribbons and then peeled the Si ribbons off the Si handle by van der Waals adhesion. Gold (200 nm) was deposited by e-beam evaporation to serve as conductive layers on both ends of the Si ribbons and PDMS substrate.

2.5. Lithiation testing structure assembly for Si thin film ribbons

A hole (10 mm in diameter) was drilled on the positive case of the CR2032 coin cell and a slice of glass (20 mm in diameter, 500 μm in thickness) was placed at the hole and was sealed on the edge to create the observation window. A PDMS stamp with Si ribbons was then firmly adhered to the glass. Au (200 nm) was deposited again by e-beam evaporation on the edge of Si ribbons, PDMS substrate, and glass through a shadow mask to ensure a good electrical connection between the Si ribbons and the positive case. The assembly of the rest of the components used in the CR2032 coin cell (including the separator, lithium counter electrode, spacer, spring, and the negative case) as well as the disassembly procedures were exactly the same as those of the standard half coin cell mentioned above. A constant current density of 400 μA cm^{-2} is applied for lithiation.

2.6. Triggered transience testing structure assembly of the thin film Si IC chips with MOSFETs

The thin film Si IC chip with MOSFETs are from a commercial 0.35 μm SOI CMOS process with a single metallization layer. The polysilicon gate devices, designed for a normal operating voltage of 3.3 V, have a 70 Å thick thermally grown gate oxide. Devices have lightly doped-drain self-aligned implants to prevent current injection in the substrate. After the standard CMOS passivation process, contact windows were defined by photolithography, followed by deposition of Au film of 200 nm and a lift-off process to ensure good electrical contact. After that, temporary bonding and debonding technology was employed to separate the thin chips from the SOI substrate, i.e. temporary attachment of the SOI wafer face down to a carrier wafer, followed by back-thinning (dry and wet etching combined method) of the silicon substrate while using the buried oxide as an etch-stop layer. Subsequently, the buried SiO_2 layer is completely removed through RIE and the Si at the reverse side of the device layer is exposed. The DC electrical characteristics of the ultra-thin film transistors were performed using a Keithley 4200 Semiconductor Parameter Analyzer at room temperature. To form the lithiation testing structure, the thin film IC chips with MOSFETs (3.6 × 3 mm) were adhered to a Cu foil with sliver paste, following exactly the same process as that of the lithiation testing structure of the Si wafer samples. The rest of the components as well as the assembly and disassembly procedures were also exactly the same. The applied current density for lithiation was also 400 μA cm^{-2}.

3. Results and discussion

The depth of lithiation regions in Si as a function of time is studied using an experimental device similar to that of a lithium-ion battery. Monocrystalline Si wafer (0.005–0.01 ohm cm) with a size of 5 × 5 mm serves as the working electrode, Li foil is the counter electrode as the lithium source, and 1 mol l^{-1} $LiPF_6$ in ethylene carbonate (EC) + diethyl carbonate (DEC) (1:1 by volume) serves as the electrolyte. Lithium is electrochemically inserted into the Si through a galvanostatic mode at a constant current density of 400 μA cm^{-2} and the V-t curve is shown in figure S1, available online at stacks.iop.org/NANO/30/394002/mmedia (supporting information).

To have an intuitive understanding of the thickness and morphology of the lithiated regions in the Si samples, cross-sectional microstructure of Si samples at various lithiation stages (3, 6, and 9 h) are investigated through FIB-SEM, and the results appear in figures 1(a)–(c). Figures 1(a) and (b) show a planar reaction front between the Li_xSi layer and the unaffected Si substrate in the 3 and 6 h samples, the same as the widely reported morphology for Li-Si batteries [30–32]. The thickness of the Li_xSi layer of the 3 and 6 h samples are measured to be approximately 0.80 μm and 1.30 μm after the correction of sample stage inclination. Certain variation of the solid electrolyte interphase (SEI) thickness is detected, indicating the heterogeneous formation of the SEI layers. By contrast, instead of a planar phase boundary, a vein-like network of Li_xSi layer is formed beneath the planar Li_xSi layer after 9 h of lithiation as revealed in figure 1(c). The morphological transformation of the Li_xSi layer greatly accelerates the penetration of the Li_xSi layer into the unlithiated Si substrate and the total thickness of the lithiated region increases to be approximately 14 μm (figure 1(c)). The cross-sectional microstructure of the Si after 12 h of lithiation shows a further growth of Li_xSi layer and a more complex structure (figure S3, supporting information). The frontier of the vein-like Li_xSi network has reached over 25 μm after 12 h of lithiation.

The progress of SEI and Li_xSi alloy formation at the initial stages of lithiation is also given in figure S2 (supporting information). On the surface of the Si, small isolated 'clumps' grow into a continuous SEI layer of 100–200 nm thickness after 30 min of lithiation, and a thin Li_xSi layer forms beneath the SEI layer after 60 min of lithiation. These results suggest that the Li_xSi layer in Si does not occur after approximately 60 min of lithiation while a large proportion of the electrochemical reaction results in the formation of a thin SEI at this initial stage.

AES is carried out on the Si samples after 3, 6, and 9 h of lithiation to investigate the depth profiles of the lithium and associated elements through layer by layer argon-ion (Ar^+) sputtering. To achieve the layer by layer analysis, the AES measurement and argon-ion sputtering are conducted alternately. The sum of the sequential Ar^+ sputtering time gives the accumulative argon sputtering time and can be converted into the depth information. The intensities of the C KLL (I_C), O KLL (I_O), Li KLL (I_{Li}), and Si LVV (I_{Si}) transitions at different lithiation states are shown in figure S4 (supporting information). The atomic percentage of C (F_C), O (F_O), Li (F_{Li}), and Si (F_{Si}) in the Si samples can be calculated as follows [33, 34]:

$$F_X = \frac{I_X * S_X}{I_C * S_C + I_O * S_O + I_{Si} * S_{Si} + I_{Li} * S_{Li}}. \quad (1)$$

X refers to C, O, Li, or Si in the equation. The relative sensitivity factors of C (S_C), O (S_O), Li (S_{Li}), and Si (S_{Si}) are 0.128, 0.296, 0.07, and 0.069 at 5 kv/5 nA, respectively, and are considered as constants. Thus, the depth profile of each element as a function of Ar-ion sputtering time can be concluded from figure S4 and equation (1), and the results are presented in figures 1(d)–(g).

Figures 1(d) and (e) show the depth profiles of C, O, Li, and Si in the Si samples after 3 and 6 h of lithiation. Figures 1(f) and (g) present the representative depth profiles of C, O, Li, and Si in two adjacent regions in the same Si sample after 9 h of lithiation, as non-uniform morphology is observed (figure 1(c)). Certain levels of C and O are observed in the surface layer of all Si samples (figures 1(d)–(g)), indicating the formation of the SEI layer, similar to that found in the initial charging stage of lithium-ion battery [35–37]. The sputtering time of the C and O rich regions increases from approximately 2–30 min (figures 1(d) and (e)), suggesting that the SEI layer thickens greatly between 3 and 6 h

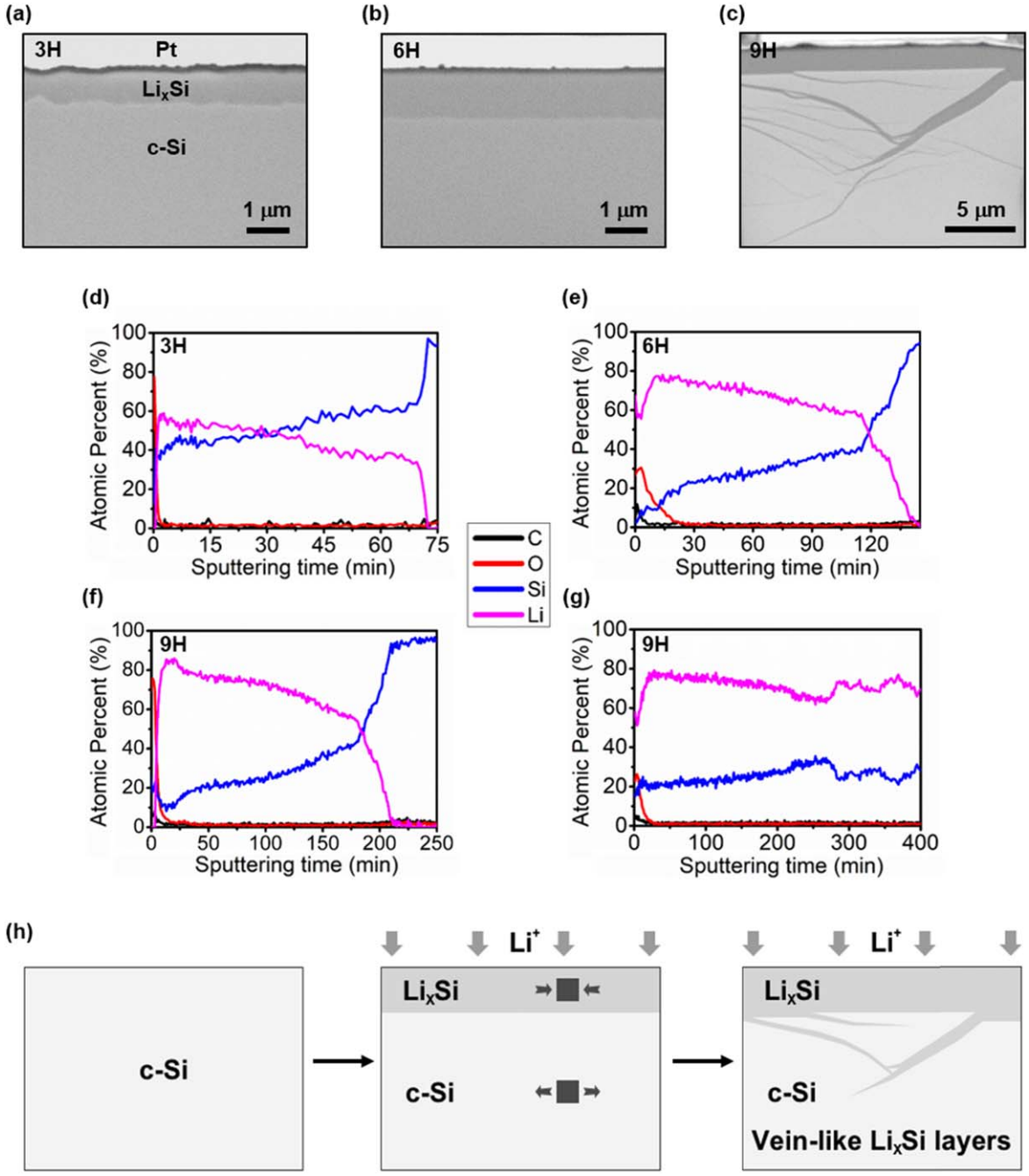

Figure 1. (a)–(c) Cross-sectional images of Si samples after 3, 6, and 9 h of lithiation; (d)–(e) The Auger depth profiles of C, O, Li, and Si in Si wafer samples after 3 and 6 h of lithiation; (f)–(g) The representative Auger depth profiles of C, O, Li, and Si in two adjacent regions in the same Si sample after 9 h of lithiation; (h) A schematic illustration of the morphological transformation of Li_xSi layers upon lithiation.

of lithiation, probably due to the competition between SEI formation and Li^+ insertion in the early stage before the stabilization of the SEI layer [38]. By contrast, the sputtering time of the C and O rich regions remains constant (~30 min) after 6 h (figures 1(f) and (g)), indicting the formation of a stable SEI layer before the end of 6 h of lithiation. The non-uniform C and O composition in different regions (figures 1(f) and (g)) could be due to the complex and heterogeneous formation process of the SEI layers at high current density [39–41].

The depth profiles of Li at different lithiation times exhibit the same variation tendency, as shown in figures 1(d)–(f). Li concentration first decreases gradually in the Li-rich region and then drops rapidly to zero in the transition region. This is consistent with the widely reported two-phase mechanism in the first lithiation cycle of the Si electrode of lithium-ion batteries [25, 32, 42–44]. It has been suggested that a higher concentration of Li near the Si–Si bond could accelerate the rate of the Si–Si bond breakage, so a clear boundary appears between the lithiated region and unaffected region

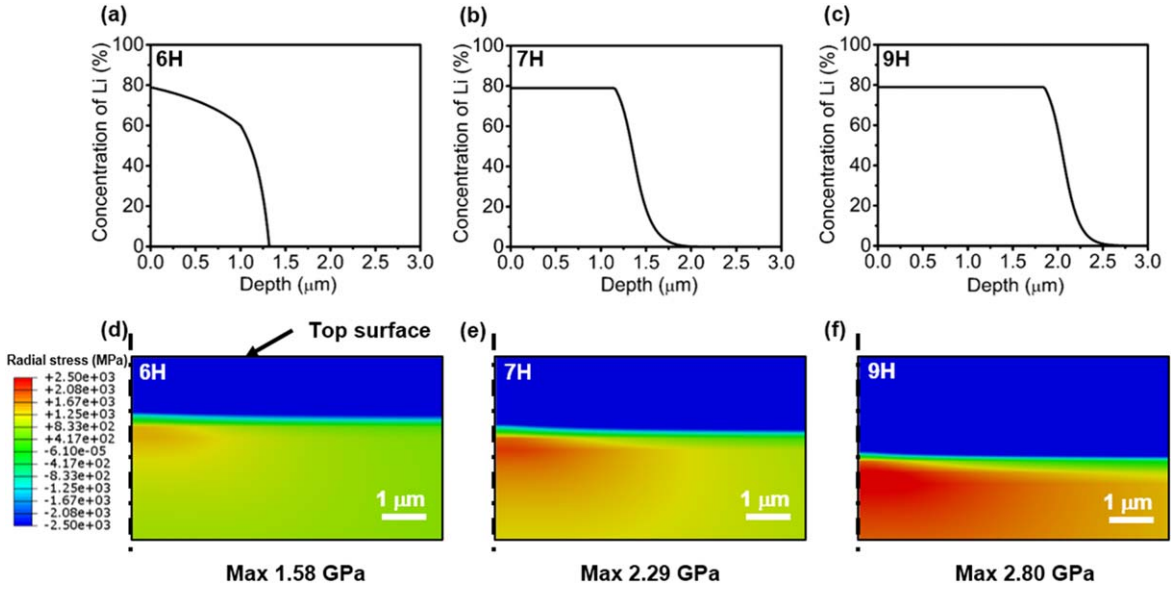

Figure 2. (a)–(c) Li concentration profiles in Si after 6, 7, and 9 h of lithiation calculated through the diffusion model; (d)–(f) The field of radial stress in Si after 6, 7, and 9 h of lithiation simulated by the finite element method (FEM).

[25]. Besides, in figure 1(f), the highest ratio of Li in lithiated Si is approximately 79%, indicting the formation of $Li_{3.75}Si$ which is the theoretical saturated state of lithiated Si at room temperature. Moreover, the thickness of the lithium affected regions can be obtained from the Auger profiles by converting the sputtering time into depth information. By using the sputtering rate of a standard silicon dioxide sample (11 nm min^{-1}) and excluding the sputtering time of the SEI layers, the lithium affected depth is calculated to be approximately 0.78 μm (71 min) and 1.32 μm (120 min), respectively, for 3 and 6 h of lithiation, consistent with the FIB-SEM observations.

As expected, two types of Li depth profiles are observed in the 9 h samples (figures 1(f)–(g)), in the sense that lithium concentration either monotonically decreases the same as the short-time lithiation samples (figure 1(f)), or fluctuates and remains at a high concentration for a much longer distance (figure 1(g)). This phenomenon is consistent with the inhomogeneous growth of the Li_xSi layer starting between 6 and 9 h of lithiation (figures 1(b) and (c)).

The mechanism of the morphological transformation probably originated from the formation of microcracks in the Si samples caused by the accumulated Li diffusion-induced stress, as shown in the schematic illustration in figure 1(h). The diffusion-induced stress in the planar Li_xSi layer is believed to be compressive due to volume expansion, while the stress turns to be tensile in the unlithiated region [45, 46]. When the accumulated tensile biaxial stress in the unlithiated Si region surpasses the fracture strength of Si, microcracks could occur. These microcracks in the Si substrate create fast paths for lithium diffusion, leading to the accelerated penetration of the Li_xSi layer and therefore significantly speeds up the degradation of the Si membranes [30].

Two models are developed to reveal the evolution of the diffusion-induced stress which could lead to the generation of microcracks in Si samples. The simulations are performed up to 9 h of lithiation when the inhomogeneous Li diffusion starts (formation of vein-like LixSi network), to reveal the critical point that microcracks start and significantly promote Li penetration. The Li profiles in Si as a function of time are calculated by an analytical model and solved numerically, and are used as the input for a separate finite element model to obtain the accumulated stress. (Details of the model can be found in the supporting information.)

Figures 2(a)–(c) show the analytical modeling results of the distribution of Li in Si after 6, 7, and 9 h of lithiation, respectively. The modeling result in figure 2(c) indicates that the thickness of the lithiated region is 2.5 μm after 9 h of lithiation, comparable with the experimental result of the cross-sectional image in figure 1(c), where the planar Li_xSi layer in Si after 9 h of lithiation is approximately 2 μm. It is noted that the vein-like Li_xSi structure is not accounted for in the model.

Figures 2(d)–(f) show the radial stress distribution in the Si samples after 6, 7, and 9 h of lithiation simulated by the FEM. The stress is compressive in lithiated region and transforms to be tensile through a transition layer in the unlithiated region. Radial stress concentration is observed at the symmetry axis beneath the transition layer. The maximum values of radial stress are 1.58, 2.29, and 2.80 GPa in figures 2(d)–(f), respectively, showing a clear trend of the diffusion-induced tensile stress accumulating rapidly in the unlithiated region. When the internal tensile stress exceeds the fracture strength of the electrode, cracks could occur. Measured fracture strengths of 2–4 GPa have been reported for small Si wafer plates (400–500 μm in thickness, (100), ~5 × 5 mm) [47, 48], which is consistent with the calculated maximum value of radial stress in Si samples lithiated for 6–9 h, indicating the stress accumulation upon lithiation for a few hours is sufficient to reach a critical point that causes Si fracture. These microcracks could create fast paths for lithium diffusion, and the following crack propagation and lithiation

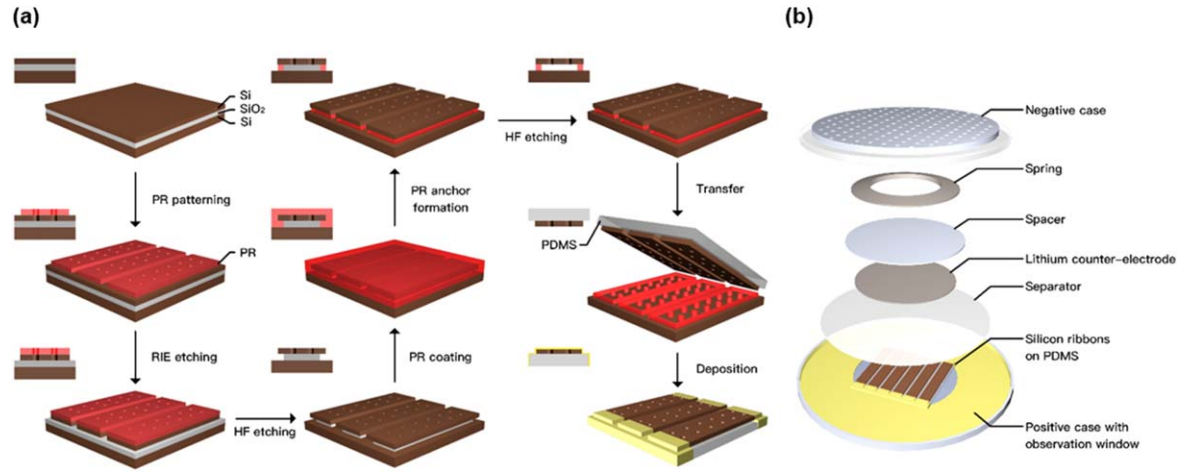

Figure 3. (a) Schematic illustration of the fabrication process of Si thin film ribbons. The Si ribbons were patterned on the top layer of an SOI wafer and transferred onto a PDMS stamp after forming anchors beneath the edges of the Si ribbons with photoresist and removing the buried oxide layer; (b) the exploded view of the lithiation testing structure with an observation window.

could result in the vein-like network of the Li_xSi layer which could significantly promote the lithiation-affected depth. Thus, the onset of the microcracks triggers the formation of the vein-like networks, which is qualitatively predicted in the current model. A future extended FEM could be performed to simulate the detailed evolution of the vein-like network if accurate experimental data on the fracture limits/toughness of thin Li_xSi ribbons are available.

The study of lithium penetration depth and stress evolution as a function of time provides information on potential lithium affected regions if electrochemically inserted into the Si layer of transient electronics. These results suggest that electrochemical lithiation for 6–9 h is sufficient to generate stress that cause microcracks and significantly promotes Li penetration depth (up to 14 μm), suggesting the feasibility of triggered degradation of a Si device. In the next step, thin film Si ribbons (2 μm in thickness, 10 mm $\times$ 500 μm, 0.005–0.01 ohm cm) are used to simulate Si electronics in the thin film format to investigate the morphological evolution upon lithiation. Figure 3(a) presents a schematic illustration of the fabrication of Si ribbons and figure 3(b) shows the exploded view of the testing structure. Si ribbons is obtained from a SOI wafer through photolithography and RIE. Following forming photoresist anchors and HF undercut, Si membrane ribbons are transfer printed onto a poly(dimethylsiloxane) (PDMS) stamp. It is noted that rows of holes are made in the Si ribbons to accelerate the HF undercut process. A thin layer of gold is then deposited on the sides of the Si ribbons to assure good electrical contact, and the PDMS with Si ribbons is assembled in the case of a CR2032 coin cell with a transparent observation window as shown in figure 3(b). A constant current density of 400 μA cm^{-2} is applied to perform the lithiation experiment. More fabrication details can be found in the methodology session.

The *in situ* lithiation process of Si ribbons are monitored and recorded every 30 min since the start of the reaction (video S1 in the supporting information, consisting of 25 photos taken from 0−12 h of lithiation). Figures 4(a)–(e) present the evolution of the morphology of the Si ribbons after 0, 3, 6, 9, and 12 h of lithiation. The rows of holes shown in figure 4(a) are made through the ribbon fabrication process to assist HF undercut. Note that some bright points and lines are observed on the Si ribbons in all the images, probably because the Si membranes on the PDMS became slightly uneven after the assembly of the testing structure. As shown in figure 4(a), the Si ribbons are relatively flat before lithiation, and buckling morphology gradually develops between 3 and 6 h which results in the strong light reflection in the images (figures 4(b)–(c)). Although no buckling morphology is observed in the Si wafer samples upon lithiation, it is a common phenomenon for Si membrane ribbons due to the good flexibility resulting from the reduced thickness and soft PDMS substrate [27, 49]. The wrinkles are non-uniform and anisotropic because the electrical conductivity of highly doped Si is still limited and variation of electrochemical reactions could exist across the samples. As lithiation proceeds, the diffusion-induced stress further accumulates in the buckled Si, and fracture occurs after 6–9 h as shown in figures 4(d) and (e) which leads to a weaker reflection in the optical images.

The corresponding SEM images of the representative fracture morphology at 0, 9, and 12 h appear in figures 4(f)–(h). The results show that the Si ribbons are flat and intact to begin with, and fragmented into tiny microscale pieces after approximately 6–9 h of lithiation, followed by fragmentation into even smaller pieces after 12 h, consistent with the optical observations. The anisotropic wrinkles, especially those localized wrinkles, and the vein-like network of the Li_xSi layer may lead to local concentration of diffusion-induced stress, and macrocracks and even integral fracture could occur consequently. The micro-scaled pieces breaking up into even tiny strips indicates that fracture could occur multiple times at the center of the broken pieces in further lithiation. As each broken piece can be considered as a separate electrode, the evolution from micro-scaled pieces to even smaller strips fit well with our simulation results in figures 2(d)–(f) that the

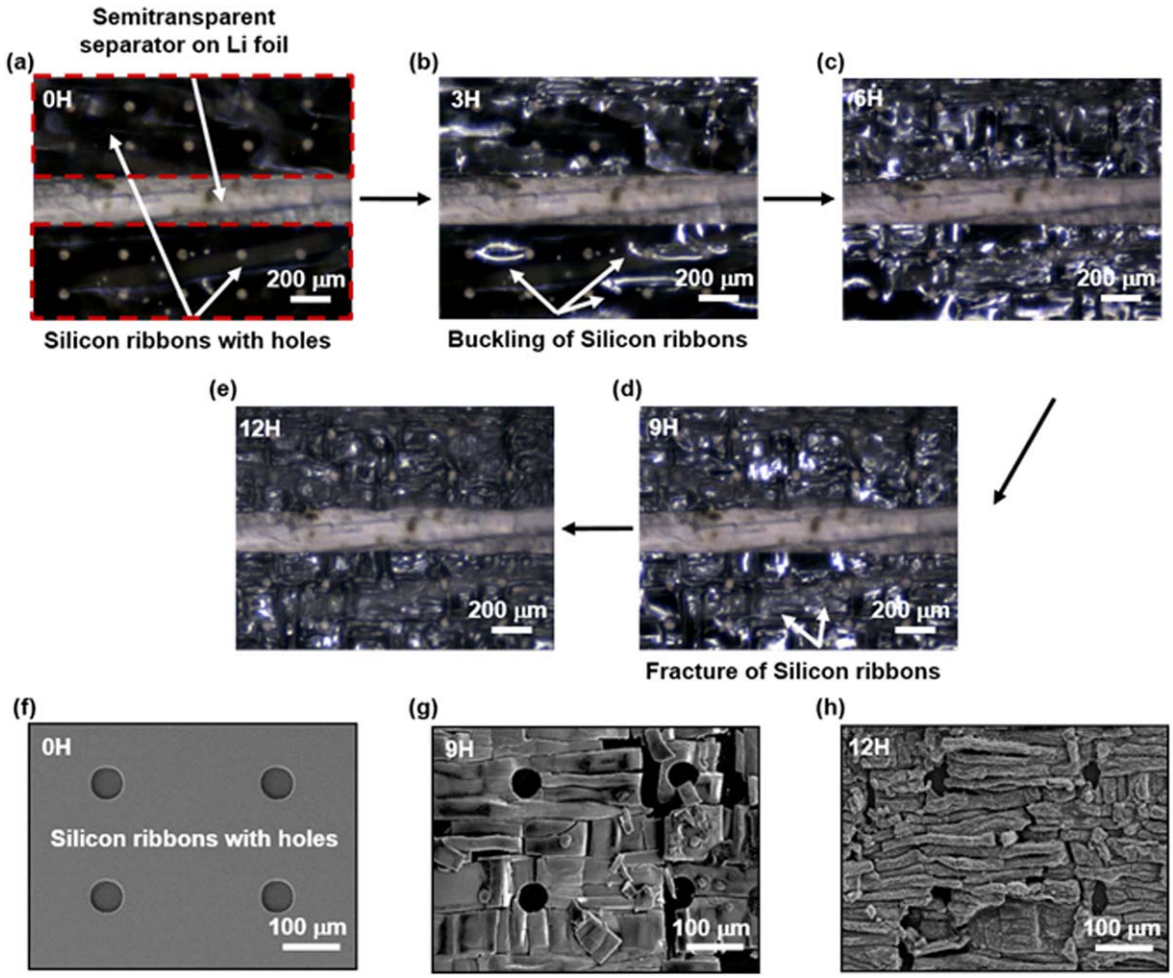

Figure 4. The evolution of the morphology of the Si membrane ribbons (highlighted regions in red dotted boxes) after lithiation. (a)–(e) the *in situ* observation of the evolution of the morphology of the Si ribbons after 0, 3, 6, 9, and 12 h of lithiation; (f)–(h) SEM images of the representative fracture morphology at 0, 9, and 12 h.

greatest radial stress concentrate near the center of the samples.

During the course of electrochemical triggering by lithiation, the chemistry modification by lithiation and physical fracture probably play the key role over buckling in the device breakdown. As the peak strain of materials under deformation scales down with thickness, thin Si membranes ensure a low strain level upon bending or buckling and therefore will probably not significantly influence its electrical performance [50]. In fact, Si membrane devices have been reported to have electrical performance depending on the bending conditions [51], and it has been proved that Si membrane devices can maintain good electrical behavior under a certain degree of bending [52–54]. As the buckling on Si membrane devices could be regarded as anisotropic bending, non-severe buckling alone would probably not lead to critical device failure. Si membranes are therefore considered to have good flexibility and have become one of the most promising semiconductor materials for soft electronics [55]. By contrast, the insertion of lithium ions that modify the materials chemistry and fracture and induces physical disintegration at a later stage plays a critical role, which would guarantee complete device failure.

To further demonstrate the feasibility of applying the electrochemically triggered transience mechanism to commercial electronics which consists of multilayer structures including Si, SiO_2, metals, etc. Thin film Si IC chips with standard commercial MOSFETs (providing both n-channel and p-channel devices) cut into a sample size of 3.6 × 3 mm are used to investigate the on-demand degradation behavior. A detailed schematic illustration of the MOSFET is presented in figure 5(a). The corresponding thickness of the P-sub), N-epi, FOX, ILD, and metallization layers are 2.5, 0.7, 0.4, 1, and 0.5 μm, respectively. Total thickness of the device layers is around 4.5−5 μm. The front surface of an individual n-type metal-oxide-semiconductor (NMOS) transistor is shown in figure 5(b), and the typical I_d-V_d output characteristics for the NMOS for different gate overdrives are presented in figure 5(c), indicating a desirable electrical performance after wafer thinning down to about 5 μm.

The thin film device is adhered to a Cu foil with sliver paste, and assembled into the CR2032 coin cell with the structure similar to that of figure 3(b), but without the observation window. Lithiation is performed at a constant current density of 400 μA cm^{-2}. Li is inserted into the electronics from the exposed Si side. Figure 5(d) shows the

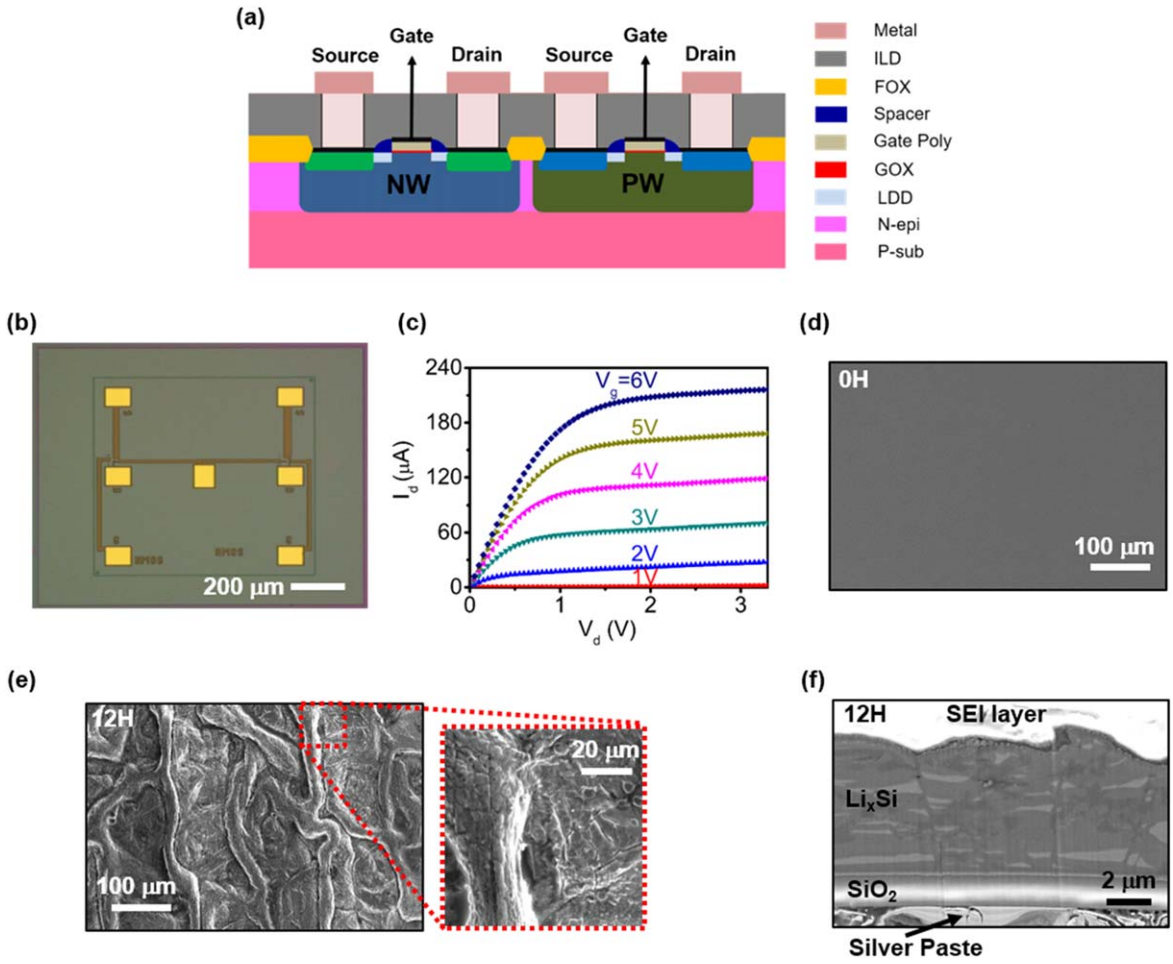

Figure 5. On-demand degradation behavior of thin film Si IC chips with MOSFETs. (a) A schematic illustration of the device structures; (b) the front surface of a representative NMOS transistor; (c) typical I_d-V_d characteristics of an NMOS transistor; (d) The morphology of the reverse side (Si side) of the MOSFETs before lithiation; (e) morphology of the reverse side (Si side) of the MOSFETs after 12 h of lithiation; (f) cross-sectional FIB-SEM image of the MOSFETs after 12 h of lithiation.

morphology of the reverse side (Si side) of the sample before lithiation, which is flat and intact. As expected, deformation and buckling of the thin film transistor after 9 h of lithiation is observed (figure S5, supporting information) and deformation become more severe after 12 h of lithiation, as the SEM image shown in figure 5(e), and multiple microcracks are illustrated in the enlarged SEM view, which are in good consistence with the previous results. The deformation morphology of the MOSFET device is more complicated compared to that in the Si ribbons due to the much more complex structure (with various doping profiles and multilayer compositions) of the sample, especially in the active regions which could create a certain constraint for diffusion-induced stress. Figure 5(f) presents the cross-sectional FIB-SEM image of the thin film device after 12 h of lithiation, which is taken at the peak area of the buckling structure. Although the SiO_2 layer remains unaffected as it is relatively stable upon lithiation, a vein-like lithium affected region develops throughout the entire Si layer. The morphology in figure 5(f) is similar to that in figures 1(c) and S4, yet the vein-like network of Li_xSi layer is more intensive and penetrates through the entire device. The Si layer consists of the substrate layer and the epitaxy layer, and their original thickness is 3.2 μm in total before lithiation. This layer expands severely during lithiation and almost doubles that original thickness (6 μm). As the diffusion of lithium into Si could cause a volume change of 280% at full capacity ($Li_{15}Si_4$) in room temperature, the observed expansion ratio less than 200% in our work suggests that the Si layer might not yet reach saturation after 12 h of lithiation.

The aforementioned experimental results indicate that electrochemical lithiation is able to induce complete destruction of single Si membranes and Si IC chips with thickness comparable to industrial standards. The device is expected to lose functions once lithiation is initiated, while complete material degradation to Li_xSi occurs after 9–12 h.

Although the degradation time is a crucial factor for self-destructive devices other factors, such as long-term stability and completeness of destruction, are equally important in practical applications. For example, the device could lose its functions, but the critical IC design can be retrieved and the devices could still undergo recovery risks. Complete destruction is therefore important. On the other hand, robust

stability is also critical as unwanted triggering will greatly impair device functions. Although a relatively long degradation time (∼9 h) might limit practical applications in scenarios that require immediate device transience, this electrochemical transience mechanism can be of great importance for scenarios in which both robust stability and complete destruction of the device are highly required while slightly longer triggering time can be tolerated, such as data secured hardware that has a certain expected lifetime. Future work reducing the degradation time through electrochemical triggering would definitely expand its application capability. Potential methods include: (1) introducing pre-lithiation at the backsides of a Si device without affecting device performance, to reduce the time (a couple of hours) needed to establish a stable SEI layer and formation of the uniform Li_xSi layers; (2) forming micropatterns on the backside of a Si device to promote the lithiation kinetics; (3) reducing the device thickness to accelerate the degradation process.

To ensure stability, a CR2032 cell battery structure is applied in our work to prove the concept of lithiation-induced cracking of thin film monocrystalline silicon. Measurement of the real-time electrical performance upon lithiation should provide detailed information on the device breakdown process. In order to do so, a future new testing structure is needed to allow electrical probing of thin film devices. The new testing structure would allow the outlets of the electrical wires but still maintain a good sealing. The CMOS device would also need a special design to have extended contact pads to allow wiring to measure the electrical performance. For future integration of the lithiation setup with standard IC chips, instead of assembling the device into a battery structure, a thin chamber could be formed on the backside of the IC chip packaging separator, electrolyte, and lithium sources. A solid electrolyte (inorganic ceramic or organic solid polymer) could also be used to replace the liquid electrolyte, to reduce the difficulty of packaging. As the lithium source and electrolyte materials are highly reactive with oxygen and water, the setup assembly has to be conducted in an inert atmosphere. An appropriate sealing method is therefore needed to ensure desirable performance. Since sealing technology is quite mature for devices requiring inert atmosphere such as lithium-ion batteries, lithiation setup assembly with IC chips in inert atmosphere is expected to be feasible. Once the sealing is completed, the package can be used in ambient air without affecting the performance. Moreover, to minimize the risk of ceasing the lithiation process manually by external force, the device structure could be carefully designed to enable the compacted and inseparable integration of Si IC chips, making it difficult to cease the lithiation process without incurring non-recoverable damage to the Si IC chips. In addition, a secondary transience method could also be integrated into the setup as a double insurance and would be automatically triggered once the lithiation process is abruptly ceased. For example, micro water containers could be added and trigger the reaction with the lithiated Si layer.

4. Conclusion

To summarize, a novel electrochemically triggered transience mechanism of Si is proposed, allowing the on-demand and complete failure of Si electronics. The depth profiles of lithiated regions in monocrystalline Si wafer samples as a function of time is studied with AES and corresponding cross-sectional microstructure are investigated by FIB-SEM. The vein-like network of the Li_xSi microstructure develops after 9 h of lithiation and greatly accelerates Li penetration depth. The evolution of the morphology is attributed to the microcracks generated from the accumulation of significant diffusion-induced stress during lithiation, and finite element models are proposed to support the hypothesis. Real-time observation of the evolution of the morphology upon lithiation of Si thin film ribbons is performed to simulate the behavior of Si electronics upon electrochemical lithiation. Fragmentation of Si thin film ribbons into micro-scaled pieces after 6–9 h of lithiation are observed. Demonstration of such electrochemically triggered transience is also successfully performed with thin film Si IC chips with MOSFETs from commercial 0.35 μm CMOS technology node, showing degradation of the entire Si component into Li_xSi alloy and generating multiple micro-scale cracks in the thin film device within 9 h of lithiation. The new electrochemically triggered transience by lithiation provides novel complete on-demand degradation for Si thin film electronics, with practical configurations compatible with CMOS foundry standards. If combined with subsequent transience, e.g., reaction with moisture or water in the atmosphere, complete physical disappearance of the active Si part is possible at the IC level. Future work will involve developing strategies to incorporate the testing structure shown in the current work with standard IC chips. Given the maturity of Li-ion battery assembly, the long-term preservation of the device package could be robust. The lithiation process could also provide extra power for electronics if needed. Incorporating a wireless electrical triggering component can further advance the transient modality. Although the complete degradation time of the chip materials takes a few hours, the device is expected to be dysfunctional much sooner after the electrochemical triggering. The electrochemically triggered transience mechanism shows unique features in robust stability, precise controllability, and complete destruction, and can be of great importance for security hardware that can tolerate slightly longer triggering time. This work provides new routes and insights for designing advanced smart and on-demand transient electronics, with great potential applications for secured data storage and environmentally benign consumer electronics.

Acknowledgments

Yaoxu Chen, Huachun Wang, and Yuan Zhang contributed equally to the work. Thanks to Qihan Luo for assistance in the preparation of the figures and video. This work was supported by

the National Natural Science Foundation of China (NSFC) 51601103 (L Y) and 1000 Youth Talents Program in China (L Y). S W acknowledges the support from the National Science Foundation (Grant DMR-1905741) and Oklahoma Center for the Advancement of Science and Technology (HR18-085-1). Xing Sheng also acknowledges the support from Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences (18ZS01).

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