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Enhancement of WSe_2 FET Performance Using Low-Temperature Annealing

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In this study, we investigate a non-thermal annealing process for two-dimensional materials. Instead of high temperature, we exploit the electron wind force at near-room temperature conditions. It is an atomic-scale mechanical force that acts only in the defective regions, which is proposed to provide very high defect mobility. The process is demonstrated on back-gated WSe_2 transistors. Electron wind force annealing was performed by passing current through the device channel while actively removing the Joule heating. We observe approximately one order of magnitude increase in the drain current, validating our hypothesis on the mobility imparted by the electron wind force to migrate and eliminate defects. To explain the atomistic mechanisms behind the room-temperature annealing, we perform molecular dynamics simulation. Computational evidence of defects annihilation and local metallic phase transformation supports the experimental results, which can enhance the device performance. Further developments of the proposed technique will potentially lead to time- and cost-effective post-processing of two-dimensional materials-based devices.

Key words: Two-dimensional materials, WSe_2 back-gated transistor, electron wind force, molecular dynamics, atomic mobility, phase transformation

INTRODUCTION

Extraordinary electrical, optical and mechanical properties[1–5] of transition metal dichalcogenides (TMDCs)[5–9] make them potential candidate materials for next-generation nano-electronic applications. Unlike graphene, TMDCs exhibit an indirect-to-direct band gap transition as the layer thickness is reduced to a single layer.[10,11] Due to this tunable band gap, TMDC electronics such as field effect transistors (FETs), photodetectors and memory components offer devices with selectable properties.[12–15] Unlike other TMDCs, p-type, n-type and ambipolar carrier transport can be achieved in WSe_2 transistors via electrode engineering and thickness modulation.[16,17] Due to these unique properties, WSe_2 has received tremendous attention in the field of two-dimensional (2D) materials and devices.[18–20]

Performance of the 2D electronics critically depends on the crystallinity of the TMDC material. It is well-known that grain boundaries and other defects such as ring defects, dangling bonds, and vacancy defects may appear in 2D materials, depending upon the synthesis conditions.[21–27] Thus, these defects could degrade the physical properties such as carrier mobility, resistivity, thermal conductivity and mechanical properties,[28–34] which commute through device performance. Thermal annealing is the conventional method to reduce

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the defect density. However, it requires very high temperature (> 800°C), which itself can degrade the material by creating more defects or stagnate the existing ones due to the residual thermal stress between material interfaces. Thermal annealing is not suitable for many applications that employ low-temperature materials. It is also a slow process based on random diffusion. However, instead of conventional thermal annealing,[35] electrothermal annealing (ETA) could be an alternative viable path to enhance device performance after fabrication. ETA technique uses Joule heating to eliminate defects and enhance device performance.[36] Such ETA techniques have been successfully implemented on metal-oxide semiconductor field-effect transistors (MOSFETs)[36] and amorphous-oxide-semiconductor (AOS) thin-film transistors[37] using electrical current. These studies use short pulses (0.1–1 ms) at high voltages to repair devices. However, their optimization efforts suggest that annealing time and voltage could be adjusted to achieve desired annealing effects.

In this study, we propose an alternative, non-thermal route to conventional thermal annealing. Instead of using heat energy to increase the atomic mobility, we specifically target defective atoms with mechanical force, leaving the crystalline lattice alone. To achieve this, we pass electrical current through the specimen. The electrons are minimally scattered by the lattice, but they transfer their momentum whenever they meet defects and grain boundaries.[38] This gives rise to highly defect-specific atomic-scale force known as the electron wind force (EWF). Thus, the EWF is minimum inside the lattice and maximum at the defects. It is coupled with resistive (Joule) heating, which is well-known in the electromigration literature.[39] Previous studies on blanket films of thin metal[40–42] and 2D materials[43,44] indicate the effectiveness of EWF, even in the presence of Joule heating. However, it is not clear whether the improvement in crystallinity is due to the EWF or the heat. To the best of our knowledge, there is no study in the literature that eliminates the Joule heating using active cooling and yet demonstrates enhancement of crystallinity. The essence of this study is that we decouple and eliminate the Joule heating through active cooling to maintain the transistor surface at room temperature. This in contrast to the literature, where defect mobility is viewed as a predominantly Joule heating effect. Another contribution of this study is the investigation of WSe_2 FETs instead of blanket films. Two layers of WSe_2 were grown via metal-organic chemical vapor deposition (MOCVD) at relatively lower temperature for higher defect density. The study thus demonstrates EWF annealing of fully functional electronic devices and provides insights on the processing parameters and their optimization for time- and cost-effective performance enhancement.

MATERIALS AND METHODS

Metal-Organic Chemical Vapor Deposition (MOCVD) Synthesis of Epitaxial WSe_2

The MOCVD growth of WSe_2 thin films was carried out in a custom-built vertical cold-wall CVD reactor as previously reported elsewhere.[45] The tungsten hexacarbonyl [$W(CO)_6$] (99.99%, Sigma-Aldrich) and hydrogen selenide [H_2Se (99.99%, Matheson)] were used as metal and chalcogen precursors, respectively, with high-purity H_2 as the carrier gas. The $W(CO)_6$ source was kept inside a stainless-steel bubbler where temperature and pressure were maintained at 30°C and 725 Torr, respectively. H_2Se gas was supplied from a separate gas manifold and introduced at the inlet of the reactor from a separate line to prevent the intermixing of the precursors. The epitaxial WSe_2 was synthesized as in a previously reported three-step growth method (nucleation, ripening and lateral growth) at 800°C and 700 Torr on c-plane sapphire substrates.[45,46] Prior to the growth, the substrates were cleaned using ultrasonication in acetone (10 min) and isopropyl alcohol (10 min) followed by 20 min immersion in commercial Piranha solution (Nanostrip, KMG Electronic Chemicals) at 90°C and deionized (DI) water rinse (10–14 times).

Device Fabrication and Characterization

The WSe_2-based field effect transistors (FETs) were fabricated and characterized in order to study the impact of the EWF annealing process on synthetic two-dimensional materials. The as-grown monolayer WSe_2 film was transferred to a rigid Si substrate with 285-nm thermally grown SiO_2 dielectric layer that served as the global back-gate by employing a PMMA-assisted wet transfer technique. A standard e-beam lithography (Vistec EBPG 5200) process was used to pattern the WSe_2 film and the source and drain electrodes. A Plasma-Therm Versalock 700 high-density inductively coupled (ICP) plasma etch tool was used to isolate the WSe_2 channels with a SF_6/O_2 30/10 sccm gas mixture for 20 s. An evaporated 40-nm Ni/30-nm Au metal stack was used as the source and drain electrodes. The electrical measurements were carried out at room temperature in a high-vacuum ($\sim 10^{-5}$ Torr) CRX-VF Lake Shore probe station to minimize threshold shifts due to moisture along with a Keysight B1500A Semiconductor Device Analyzer.

Modeling and Simulation

To investigate the microstructural changes resulting from EWF, we simulated monolayer WSe_2 using the molecular dynamics (MD) method. Due to the length and time scale limitations, MD simulation can provide a qualitative understanding of the defect annihilation mechanism and quality

enhancement of the WSe_2 film. In our present study, we employed Stillinger–Weber[47] potential to model WSe_2 using LAMMPS[48] code. Polycrystalline WSe_2 samples with 16 grains (Fig. 4a) and a grain size of 8 nm were modeled using the Voronoi tessellation method. The grains were rotated at 0°, 30°, 45° and 60° with respect to the basal plane. At the beginning, we performed energy minimization using the conjugate gradient (CG) method followed by isothermal–isobaric (NPT) dynamics runs for several thousand steps to obtain a residual stress-free structure. Once we obtained an equilibrated structure, we apply wind force on each atom calculated from the Huntington-Grone[49] ballistic model to mimic electrical annealing (EA). EWF simulations were performed using the Verlet algorithm under the canonical NVT dynamics. The simulation temperature was kept constant at 300 K by rescaling the velocity, and a time step of 0.5×10^{-15} s was employed during all simulations. In our simulations, we also applied periodic boundary conditions along all directions.

A unique aspect of this study is the decoupling of the Joule heating from the EWF and exploitation of the latter to anneal the 2D WSe_2 at near-room temperature. In our experiments, the transistor was placed on an actively cooled stage. Direct measurement of the temperature was difficult because of the small size (channel length and width of 1 μm and 5 μm, respectively) of the region of interest compared to commercially available thermal microscopes. To investigate temperature rise in the sample during the electrical annealing, we performed multi-physics modeling of Joule heating using COMSOL® software as shown in Fig. 1c and d. In our present study, we consider interfacial thermal boundary conductance of 12 MW/m^2 K [50] and 125 MW/m^2 K [51] between WSe_2-SiO_2 and Si-SiO_2, respectively. Our multi-physics modeling did not show any significant temperature rise during 20 V and 30 V annealing, which could be attributed to the low annealing current density ($\sim 3.2 \times 10^7$ A/m^2) and controlled stage temperature (i.e., 296 K). However, temperature may rise as high as 380 K, as shown in Fig. 1c, due to the Joule heating effects with an annealing voltage of 50 V at moderately high current density ($\sim 3.2 \times 10^8$ A/m^2). Our calculated temperature rise is in a good agreement with recent study.[51]

RESULTS AND DISCUSSION

WSe_2 FETs were annealed using electrical current at different drain voltages under vacuum condition. Electrical annealing induces both Joule heating and EWF. However, during the annealing process, temperature was controlled at 296 K to avoid any temperature rise. Additionally, the transistor substrate acts as massive heat sink during the annealing process. The finite element electrothermal simulation also indicates negligible temperature (304 K) rise with an annealing voltage of 30 V. Thus, it can be assumed that EWF alone induced the observed annealing effect at low temperatures.

Figure 2a shows our experimental results on low-temperature EWF-induced annealing in terms of the output characteristic curve (I_d versus V_d). The blue line in Fig. 2a indicates the drain output current before annealing. However, after annealing

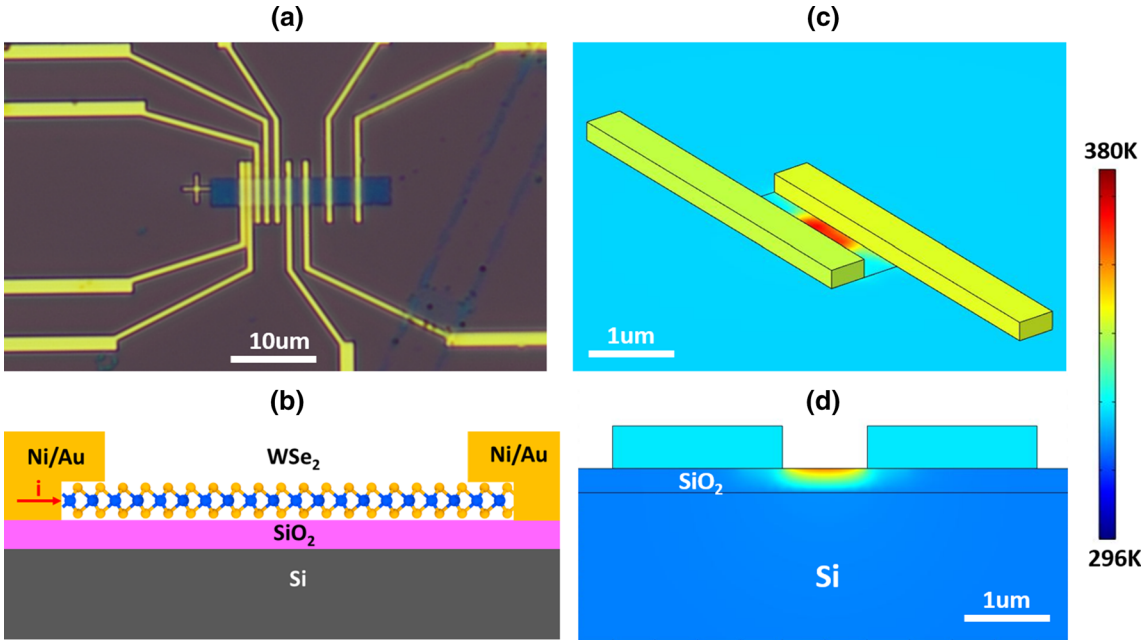

Fig. 1. (a) Optical microscope image of fabricated WSe_2 transistor, (b) schematic diagram of WSe_2 transistor, (c) electrothermal simulation result showing temperature rise during the annealing and (d) temperature profile across the cross-section obtained from electrothermal simulation model.

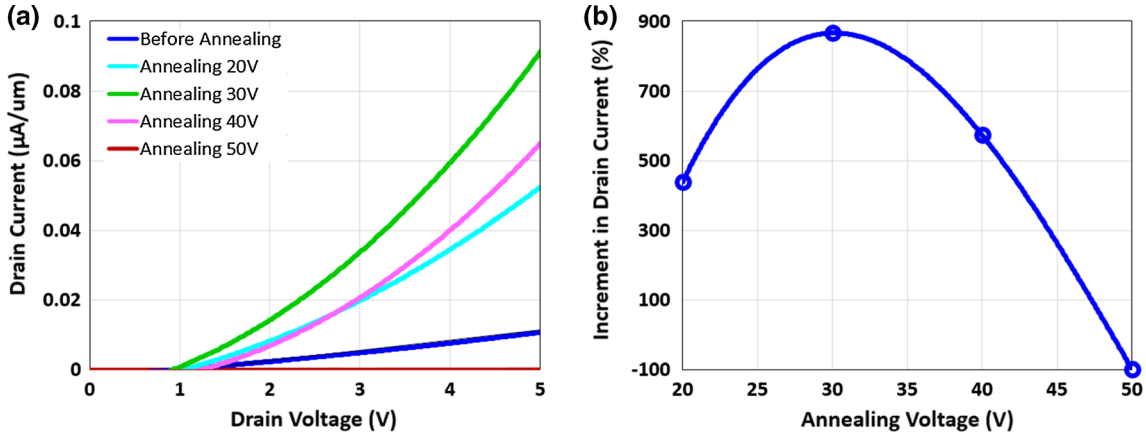

Fig. 2. (a) Output characteristics of the WSe_2 transistor after annealing at different drain voltages; (b) improvement in drain current after annealing with the FET surface maintained at 23°C.

at a drain voltage of 20 V, the output current increased more than one order of magnitude, as shown by the cyan line in Fig. 2a. During 20 V EWF annealing, the channel current reached a maximum value of 0.2 μA. The total biasing lasted for 5 min, which was sufficiently longer compared to a previous study.[37] This prolonged annealing duration makes the EWF method effective without inducing any significant temperature rise in the device. Thus, enhancement in the drain output current during low-temperature annealing could be attributed to the improvement of film quality as well as contact resistance at the interface of the electrode and the device layer.[35,43,52] Almost one order of magnitude drain output current enhancement suggests significant defect annihilation in the WSe_2 channel. This represents more pronounced channel quality improvement in recent study on MoS_2 FET devices, which indicates a 21% increase in drain current after annealing.[53] Figure 2b shows our efforts at optimizing the EWF annealing at different voltages, namely 20 V, 30 V, 40 V and 50 V. With annealing voltage as the tunable parameter, we found optimum performance at 30 V. Beyond this voltage, the device started to degrade and then was damaged at 50 V, probably because the EWF itself started to migrate atoms from the cathode to anode and create nano-voids that coalesce with the progression of the experiment. Essentially, the EWF minimized vacancy defects that can form in 2D materials during synthesis or device fabrication.[54] These atomic-scale defects can strongly influence physical properties due to the high surface-to-bulk ratio in 2D materials. For example, a recent study[55] showed that tungsten (W) and selenium (Se) atom vacancy might introduce semiconducting to metallic behavior in WSe_2. Another study[56] reported that MoS_2 with Mo vacancy exhibits p-type semiconducting behavior. It has been reported that electronic properties such as electron mobility can be significantly limited by atomic-scale defects such as vacancies, dislocations and grain boundaries.[57]

Figure 3 shows the transfer characteristics at a fixed (5 V) drain voltage. Before annealing, the device showed a maximum drain current of 1.89×10^{-2} μA/μm achieved at a gate voltage of 45 V. After annealing at 20 V, it showed a significant improvement in drain current as indicated by the pink line in Fig. 3a. The drain current reached a maximum plateau value of 5.47×10^{-2} μA/μm at around 45 V gate biasing. At this point, we did not notice any threshold voltage shift (Fig. 3a). Figure 3b shows the results of our optimization efforts. For annealing voltage of 30 V, a maximum drain current of 1.35×10^{-1} μA/μm (Fig. 3b) was achieved, which is one order of magnitude higher compared to the as-received device. This remarkable increment of device performance can be attributed to the enhancement of the channel quality. Consistent with our observation on output function, the device started degrading beyond 30 V annealing voltage, and the gate could not be opened for 50 V. At high biasing condition, channel current increased and electrons gained sufficiently high kinetic energy (known as hot electron) and induced traps in the channel layer.[58] These traps acted as defects and hindered the electron mobility which potentially reduces the output current of the device after annealing at high biasing condition. In our present study, all measurements were performed three times after each EWF annealing, and output results were consistent. We also ran three sets of experiments to confirm the effectiveness of the annealing. Degradation at higher annealing voltage (i.e., $>$ 30 V) could be attributed to the combined electrical and thermal field-induced defects formation and migration effects. Due to this detrimental migration effect, atomic flux mobility increases, and defects/voids appear in the channel layer. At high current density, both EWF and temperature could enhance the mobility of atomic flux, J. Individual contribution of atomic flux due to the EWF (J_{EWF}) and temperature (J_T) can be expressed as follows:[59]

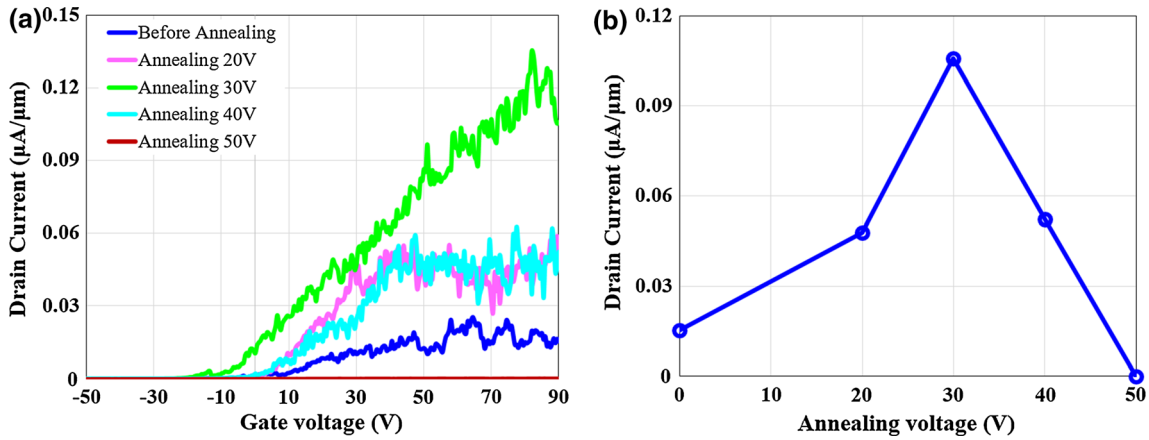

Fig. 3. (a) Transfer characteristics of the WSe_2 transistors after annealing at different voltage; (b) maximum drain current obtained from transfer characteristics after annealing.

$$J_{EWF} = \frac{NeZ^{*}D\rho}{kT} j; J_T = -\frac{NDQ\rho}{kT^2}\nabla T \qquad (1)$$

where D is diffusivity, k is Boltzmann's constant, T is absolute temperature, N is vacancy concentration, Z^* is effective charge number, e is the elementary charge, j is current density and Q is the heat of transport. Equation (1) shows that atomic flux mobility is proportional to current density (j) and temperature gradient (∇T). Thus, at higher annealing voltage, both EWF and Joule heating become dominant, which enhances atomic flux mobility. High EWF in conjunction with a high thermal field can induce directed diffusion of atoms from the cathode to anode side of the transistor (shown later in Fig. 7). This directed diffusion of atoms creates defects such as voids and cracks near the cathode side, and hillocks at the anode side, which degrade the device performance, and the device eventually fails due to the defects formation and migration effect.

Synthetic 2D TMDCs usually exhibit higher defect densities compared to their mechanically exfoliated counterparts.[31] Grain boundaries, metal and chalcogen vacancies, and ring defects are commonly found in synthetic materials which ultimately has a negative impact on the transport performance of the devices.[26,60–62] Since defect-free synthesis of TMDCs still remains challenging, we propose an alternative approach to improve the film quality and transport performance using EWF annealing.[40–43]

However, direct visualization of the defect annihilation or grain boundary reconstruction is difficult, even with atomic-resolution microscopes. Therefore, we take resort in atomistic simulation. Figure 4 shows the model of a nanocrystalline WSe_2 film with 16 grains and average size of 8 nm. The initial equilibrated structure primarily contains 2H phase (Fig. 4a), and after annealing, it contains 2H, 1T and intermediate phase as well as reconstructed grain boundaries of WSe_2 (Fig. 4b). The green and red bands as shown in Fig. 4b indicate the cathode and anode, respectively. After EWF annealing, we notice grain boundary (GB) defects could be annihilated as shown in Fig. 4b. The GB defects could be annihilated via phase transformation, an intermediate structure and twinning. Phase transformation from 2H to 1T in monolayer MoS_2 has been observed in a recent experiment.[63] Another recent study[27] also shows semiconducting to metallic behavior of WSe_2 during 2H-to-1T phase transformation. This local 1T phase transformation might enhance the device performance due to the metallic behavior. The colored arrowhead in Fig. 4b indicates possible electron flow paths without scattering at the GBs. The annihilation of defects at GBs which further forms an uninterrupted electron flow path might be the primary cause for the higher output current as shown in Fig. 2a.

The advantage of atomistic simulation is the ability to track different types of defects individually over time and space. It is known that grain boundaries in 2D materials contain ring-type defects[57,64] (Fig. 5a). For example, GB defects could be the four-ring type defects, as shown in Fig. 5, where we have marked four ring defects as R1, R2, R3 and R4 and two eight-ring defects as R8 (Fig. 5a). At 0 ps, the 2H structure is separated by four-ring defects at the GB. Under the influence of EWF, both W and Se atoms glide along the armchair edge, as shown in Fig. 5b. The pink arrowhead indicates atomic displacement after a 7-ps simulation run. The green and red dashed lines both indicate Se atom gliding. The black dashed line indicates new bond formation between W and Se under EWF along the armchair direction. At this stage, W–W atomic distance (marked by green and red dashed lines in Fig. 5b) decreases due to the EWF. After 23.5 ps, we observe gliding of Se atoms toward eight-ring defects as marked by red dashed circle in Fig. 5c. A row of Se atoms with four coordinations is observed near four-ring defects as marked by the cyan dashed line. A similar type of

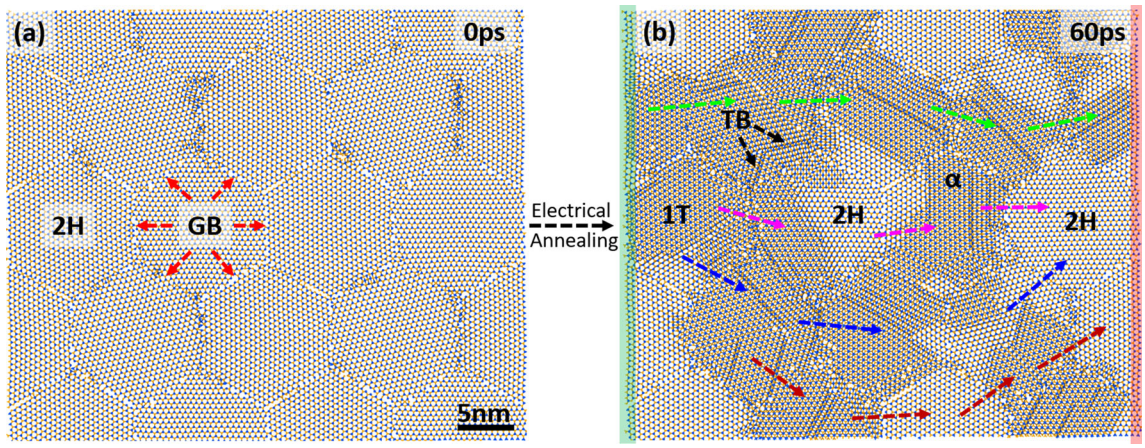

Fig. 4. Monolayer WSe_2: (a) before annealing and (b) after annealing.

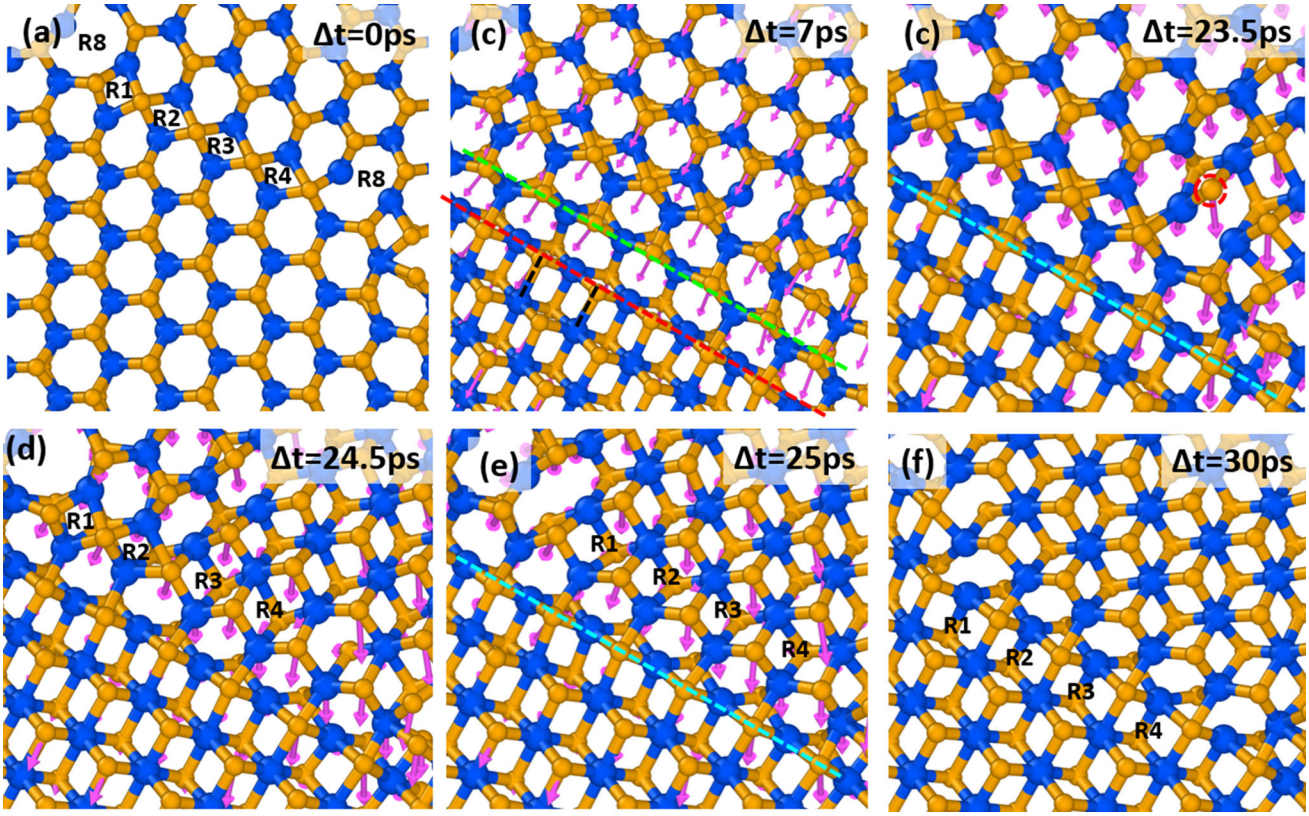

Fig. 5. Defects annihilation at the GB containing four-ring defects: (a) before annealing; (b) both W and Se atoms are gliding along the armchair edge and form a W–Se bond; (c) compression of W atoms leads to α phase and gliding of S atoms toward W atoms in eight-ring defects; (d) gliding of Se atoms and formation of a W–Se bond and partial transformation of four-ring defects to 1T phase; (e) complete transformation of 4-ring defects to 1T phase; (f) eight-ring defects to 1T phase transformation.

coordination in S has been reported[63] in MoS_2 structure, which corresponds to an intermediate β structure. Due to this gliding, eight-ring defects transform to 1T phase after 24.5 ps, as indicated in Fig. 5d. Additionally, two four-ring defects, i.e., R3 and R4, also reconstructed to 1T phase. After 25 ps, all four-ring defects convert to 1T phase, as shown in Fig. 5e. After 30 ps, the GB defects are completely annihilated by EWF, which leaves 1T phase near the four-ring GB (Fig. 5f).

Our computational results show an intriguing phenomenon called metallic twinning.[65] Figure 6a shows polycrystalline WSe_2 with 2H phase before EA. After EWF processing, we notice GB reconstruction and phase transformation in the sample (Fig. 6b). Under the influence of EWF, metallic twinning forms inside the domain of 1T phase.

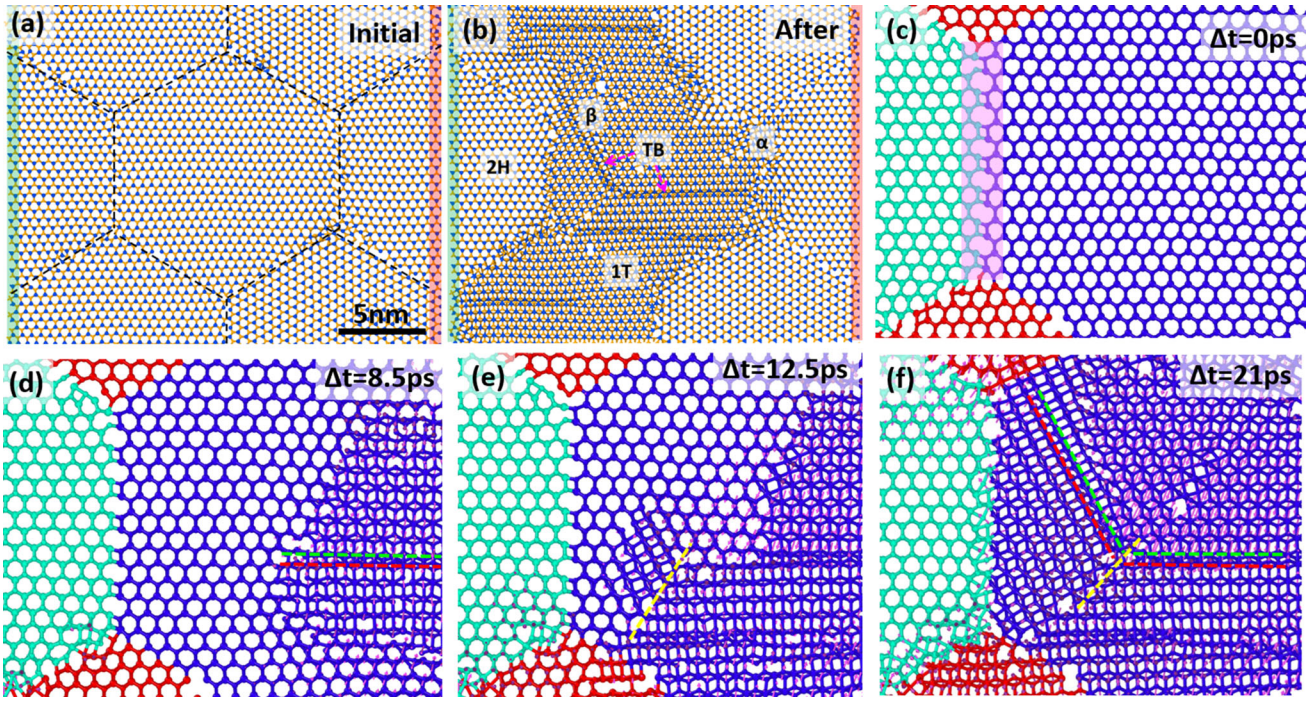

Fig. 6. (a) Sample before annealing. (b) 1T phase transformation and formation of twin boundaries; twin boundary tracking near the GB: (c) 0 ps, (d) gliding of Se atoms in the opposite direction, (e) mirror plane near the GB and formation of twining, and (f) completion of twinning formation.

Figure 6c shows the GB between grain G1 and G2 which primarily contains 8–4 defects as marked by the pink band. Both grains have 2H phase before processing. After 8.5 ps, 1T phase transformation takes place inside G2. Green and red color indicates gliding of Se atoms in an opposite direction. The row of Se atoms on the green line shows four coordinations, which is an indication of intermediate β-phase. Phase transformation continues until it reaches a triple point (Fig. 6e). After reaching the triple point, phase transformation starts on the left side of the mirror plane (yellow dashed line). After 21 ps, we notice completion of twinning formation (Fig. 6f). At this stage, we observe out-of-plane (i.e., along the basal plane) displacement of the Se atomic row on the red dashed line (Fig. 6d). The twinning formation mechanism involves complex atomic motion of both Mo and Se atoms. At the beginning, Se atoms glide along the diagonal direction (instead of the armchair or zigzag direction), and displacement of the Se atomic row marked by green and yellow colors is in the opposite direction. After the formation of twinning, displacement of the Se atomic row on the red dashed line is along the basal plane (i.e., out-of-plane). This could be attributed to the in-plane constriction in the twinning region, which is further counterbalanced by out-of-plane motion of Se atoms. As mentioned earlier, the GB might contain 8–4 ring defects (Fig. 6c); thus, we have studied their annihilation mechanism during EA (supplementary Fig. S1).

Our computational model also provides insights into the device degradation observed beyond the optimum value of the annealing voltage. This phenomenon could be attributed to the thermal- and electrical field-induced failure, which is readily observed in metallic thin films.[40,66,67] At higher biasing voltage, electrical current density is high enough to induce Joule heating as well as atomic mobility of atoms which further degrades the WSe_2 film. In order to investigate void formation and migration in WSe_2 FET, we apply sufficiently high EWF in the WSe_2 device layer and track atomic motion, as shown in Fig. 7. The initial sample with the anode and cathode marked by red and blue regions is shown in Fig. 7a. After 5 ps, we observe voids near the cathode area of the sample. The color bar in Fig. 7 shows the atomic stress distribution in the sample. At this stage, it is obvious that tensile stress arises near the cathode side, while the anode side is under compressive stress due to the EWF. As the simulation time progress, voids start to grow, as shown in Fig. 7c and d. As the voids start to grow, we observe stress relaxation in the vicinity of the voids. With the progression of simulation time, we notice gradual increment in void size near the cathode area and mass accumulation at the anode area. Thus, the device might fail due to this high atomic mobility and thermal field generated by electrical current. Figure 7g and j show a side view of the sample under high EWF. At the beginning of the simulation, there is no void or mass accumulation near the cathode (left side) and anode (right

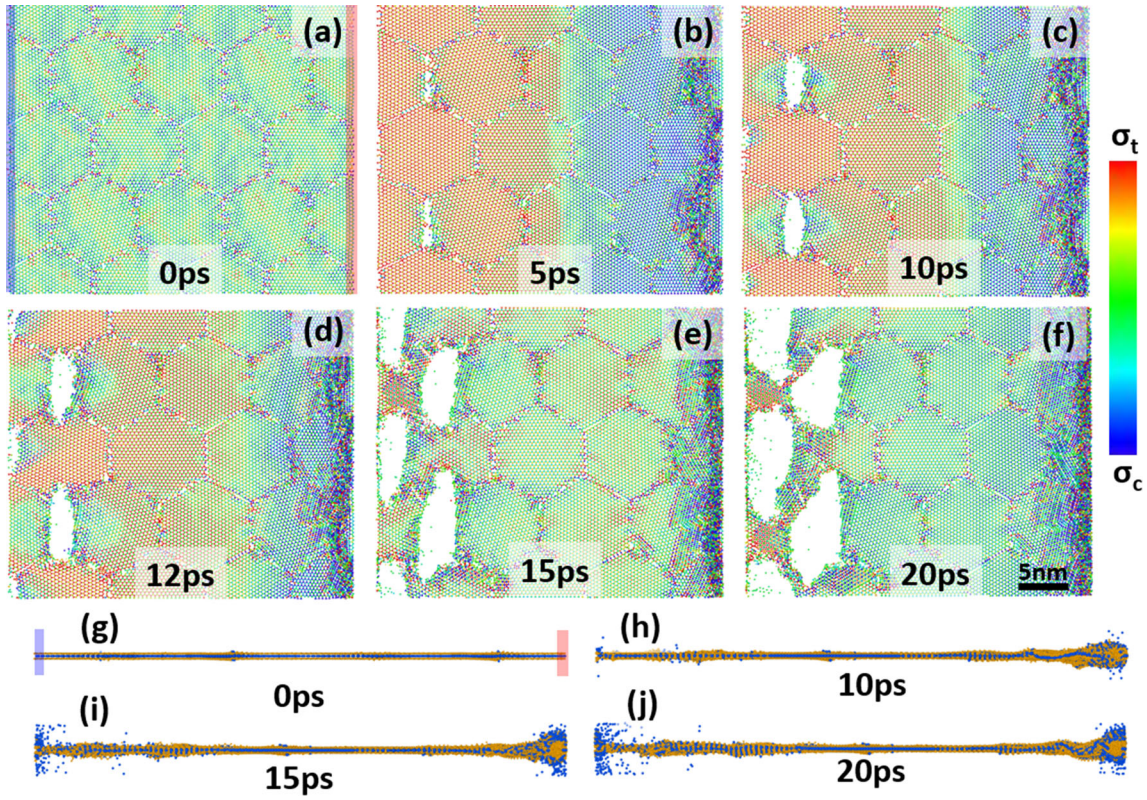

Fig. 7. (a)–(f) Failure at high biasing condition due to the electrical and thermal field, and (g)–(j) side view of the sample showing void creation at the cathode side (left) and mass accumulation at the anode side (right).

side), respectively, as shown in Fig. 7g. However, with the progression of simulation time, voids starts to form, and mass accumulation takes place (Fig. 7h and i), and eventually the WSe_2 sample fails after 20 ps, as shown in Fig. 7j.

In this present study, we have employed electrical annealing to enhance the WSe_2 FET device performance. Experimental study shows that output current can be increased by one order of magnitude at an optimum annealing voltage (i.e., 30 V). However, beyond this optimum condition, device performance starts to degrade, and the device fails to operate after 50 V annealing voltage. To comprehend the mechanism related to the device performance, we conduct MD simulation. Simulation study shows that under the impetus of EWF, GB defects could be annihilated due to the atomic mobility, intermediate phase transformation and 2H-to-1T phase transformation. The present study provides insights into an alternative, cost- and time-efficient annealing technique, which can improve device performance without introducing thermal stress, and can be applied to a wide range of devices, including flexible electronics.

CONCLUSIONS

We have studied low-temperature processing of a WSe_2 back-gated transistor using a semiconductor parametric analyzer and MD simulation methods. Our investigation shows that low-temperature processing enhances drain current output by more than one order of magnitude. Enhancement of device performance is a nonlinear function of annealing voltage, and device performance degrades after a certain annealing voltage. In our present study, experimental investigation shows that the devices exhibit enhanced performance up to 30 V and fail to operate above 50 V annealing voltage. To investigate the electrical annealing-induced atomistic mechanism, we apply a molecular dynamics method to polycrystalline WSe_2. Study shows that during electrical annealing, GB defects could be annihilated due to the atomic mobility and phase transformation even at low temperature under the influence of EWF. During defects annihilation, metallic phase transformation may take place, which could be attributed to the enhanced performance of the device. Simulation also reveals that higher voltage may degrade the device due to the defects formation and migration, which creates voids near the cathode and hillocks near the anode. Low-temperature electrical annealing can be applied to flexible electronics or other devices during their operation without inducing any thermal stress. Additionally, EWF processing requires less than 5 min, which indicates this process is an order of magnitude faster than conventional thermal annealing.

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ELECTRONIC SUPPLEMENTARY MATERIAL

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