

# ***In Situ* 2D MoS<sub>2</sub> Field Effect Transistors with an Electron Beam Gate**

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## **Abstract**

We use the beam of a transmission electron microscope (TEM) to modulate *In Situ* the current-voltage characteristics of a two-terminal monolayer molybdenum disulfide (MoS<sub>2</sub>) channel fabricated on a silicon nitride substrate. Suppression of the two-dimensional (2D) MoS<sub>2</sub> channel conductance up to 94% is observed when the beam hits and charges the substrate surface. Gate-tunable transistor characteristics dependent on beam current are observed even when the beam is up to tens of microns away from the channel. In contrast, conductance remains constant when the beam passes through a micron-size hole in the substrate. There is no MoS<sub>2</sub> structural damage during gating and the conductance reverts to its original value when the beam is turned off. We observe on/off ratios up  $\sim 60$  that are independent of beam size and channel length. This TEM field effect transistor (TEM-FET) architecture with electron beam gating provides a platform for future *In Situ* electrical measurements.

## **Keywords**

*in situ* transmission electron microscopy, transition metal dichalcogenides, field effect transistor, electronic transport, silicon nitride, molybdenum disulfide.

Transmission electron microscopy (TEM) offers an ideal platform for the structural and analytical analysis of atomically thin two-dimensional (2D) materials.<sup>1–7</sup> *In Situ* studies that combine the atomic-resolution capabilities of TEM with the growing array of electrochemistry, gas/fluid flow, and high/low temperature TEM holders have emerged as powerful tools for 2D nanoscale characterization.<sup>8–11</sup> However, methods for *In Situ* electrical biasing have seen little development and are currently limited to two terminal measurements since conventional architectures consisting of metallic back or top gates are not readily electron transparent.<sup>12,13</sup> Several *In Situ* devices including an electrical gate (*i.e.*, third terminal) have previously been demonstrated. For example, Kim *et al.* fabricated carbon nanotube (CNT) field effect transistors containing slits that allow for simultaneous transport measurements and TEM imaging.<sup>14</sup> Similarly, Rodriguez-Manzo *et al.* showed that a freestanding graphene side gate could be used to modulate the conductance in a graphene nanoribbon (GNR) spaced up to 100 nm away.<sup>15</sup> These techniques involve relatively complex fabrication procedures and result in a weak, spatially non-uniform gating effect.

Previous *In Situ* TEM works have also utilized direct electron beam irradiation of suspended as well as on-substrate 2D materials to modulate two-terminal conductance, for example, in graphene,<sup>15–18</sup> MoS<sub>2</sub>,<sup>19</sup> and WS<sub>2</sub>.<sup>20</sup> While conductance is generally suppressed due to 2D material damage from beam exposure, *In Situ* TEM Joule heating from the electrical current between the source and drain electrodes was used to induce recrystallization of the 2D lattice and cause a conductance increase.<sup>15–18,20</sup> Despite these reconstructions, techniques involving direct interactions between the electron beam and 2D material introduce some degree of irreversible damage, which results in a permanent change in electronic properties. Additional efforts are therefore needed to produce platforms for *In Situ* electrical biasing with a robust, tunable, and position-controlled gate parameter.

Here, we report the *In Situ* electrical gating of 2D MoS<sub>2</sub> channels by targeting the electron beam of a TEM at controlled positions on a silicon nitride (SiN<sub>x</sub>) window. The main features of 2D channel gating by the electron beam are summarized as follows. Devices consist of a two-terminal monolayer TMD geometry supported on a SiN<sub>x</sub> window. When the electron beam is turned on and hits the insulating substrate of the transistor chip, even up to 50 microns away from the device channel, conductance of the 2D channel changes and gating occurs due to substrate charging. As long as the beam does not hit the 2D channel material itself, this conductance

modulation is completely reversible and there is no device hysteresis or structural damage to the 2D material. Gating is controlled by tuning the strength of the TEM condenser lens (*i.e.*, spot size), which results in electron beam currents between 0 and 70 nA in this study. We observe 2D channel current on/off ratios up  $\sim 60$  that are approximately independent of beam position relative to the 2D channel, beam size, and other parameters over the timescales of our measurements.

Importantly, we establish that there is no change in the 2D channel conductance when the beam passes near the channel but through vacuum and has no interaction with the chip, as there is no SiN<sub>x</sub> substrate charging. This measurement was successfully performed by intentionally drilling a one-micron size hole in the SiN<sub>x</sub> membrane near the 2D channel using focused ion beam (FIB) milling and targeting the electron beam through its center. Similarly, no gating is observed when the beam is positioned to hit the outside of the TEM-transparent, 100 nm thick suspended SiN<sub>x</sub> window region, suggesting that charges are dissipated through the conductive Si support chip so that no significant charging occurs. *In Situ* charging and discharging on the SiN<sub>x</sub> substrate are additionally monitored by time-dependent current-voltage measurements in the 2D channel. After turning the electron beam off, the current in the 2D channel displays an exponential-like rise,  $1 - \exp(-t/\tau)$ , as the substrate discharges with a characteristic time constant of  $\tau \sim 100$  s.

## Results and Discussion

**Figure 1a** shows the optical image of the TEM field-effect-transistor (TEM-FET) device consisting of monolayer 90-100  $\mu\text{m}$  large MoS<sub>2</sub> flakes deposited onto a 100 nm thick, 60  $\mu\text{m}$  wide SiN<sub>x</sub> window. The electron transparent window is located in the center of a 3 mm by 5 mm Si/SiN<sub>x</sub> chip (**Figure 1d inset**). The MoS<sub>2</sub> crystals utilized in this study were grown through chemical vapor deposition (CVD). The photoluminescence (PL) spectrum of as-grown MoS<sub>2</sub> in **Figure 1b** exhibits a narrow peak at  $\sim 1.88$  eV that is consistent with monolayer thickness.<sup>21</sup> Likewise, the frequency separation of  $\sim 20$  cm<sup>-1</sup> between the in-plane E<sub>2g</sub><sup>1</sup> and out-of-plane A<sub>1g</sub> phonon modes agrees well with expected values for monolayer MoS<sub>2</sub> under a 532 nm excitation (**Figure 1b inset**).<sup>22</sup> Dark-field scanning TEM (STEM) lattice imaging and selected area electron diffraction (SAED) patterns indicate a hexagonal 2H phase structure, which is a relatively stable, well-characterized semiconductor compared to the metallic 1T phase (**Figure 1c**).<sup>23,24</sup>

The electrical measurement setup inside the TEM is shown schematically in **Figure 1d**. The MoS<sub>2</sub> flake is contacted through two-terminal Cr/Au leads and an *In Situ* electrical biasing

TEM holder to an external source meter. Electron-beam-lithography and 2D flake growth and transfer details can be found in the Methods and **Supplementary Figure S2**. The 200 keV electron beam used in this study is precisely positioned on the device surface by moving the TEM sample stage. We present results showing how the measured drain-source current ( $I_{ds}$ ) with an applied drain-source voltage ( $V_{ds}$ ) across the MoS<sub>2</sub> channel of length  $L_{ch}$  is gated when changing the TEM beam current ( $I_{beam}$ ), beam diameter ( $d_{beam}$ ), and its position relative to the 2D channel. The magnitude of  $I_{beam}$  is controlled in the TEM by tuning the strength of condenser lens 1 (CL1), typically referred to as “spot size.” Data presented include results from multiple (>200) continuous DC and  $I_{ds}$ - $V_{ds}$  measurements on 5 MoS<sub>2</sub>-based devices, that were electrically characterized in the TEM and gated by the TEM beam. While the magnitude of  $I_{ds}$  was observed to be different across devices due to differences in contact resistance, similar degrees of gating and current suppression were seen (for example, see **Supplementary Figures S4-S5**).

As shown in **Figure 1e**, the two-terminal monolayer MoS<sub>2</sub> device exhibits a non-linear  $I_{ds}$ - $V_{ds}$  curve under ambient *Ex Situ* conditions (pressure  $p = 1 \times 10^5$  Pa). When placed in the column of the TEM ( $p = 5 \times 10^{-6}$  Pa), an increase in  $I_{ds}$  is observed. This has previously been demonstrated in conventional back-gated MoS<sub>2</sub> FETs measured in air and in vacuum and was attributed to the desorption of gas molecules at the TMD-metal interface in vacuum, which causes a lowering of the Schottky barrier and improved charge carrier injection.<sup>25</sup> The high vacuum condition of the TEM column ( $p = 5 \times 10^{-6}$  Pa) is advantageous for producing near-ohmic behavior in TEM-FETs.

**Figure 2a** is a TEM image of one of the devices tested, with the indicated source and drain electrodes and the outline of the 2D MoS<sub>2</sub> flake deposited on top and between the electrodes. We designed and fabricated this TEM-FET device to also contain a 1.2  $\mu\text{m}$  diameter FIB hole in the SiN<sub>x</sub> window, with a high-magnification TEM image of the hole region shown in the inset of **Figure 2a**. The hole is also marked by a pink arrow in **Figure 2a** and is located about 6  $\mu\text{m}$  away from the edge of the source electrode. This hole was fabricated with ion beam milling using a 30 keV Ga<sup>+</sup> FIB after the other parts of the device were assembled. By moving the sample stage *In Situ*, the location of the electron beam is precisely guided to expose different locations on the device.

In the *hole exposure* experiment, the TEM beam with  $d_{beam} = 10$  nm was positioned to pass through the center of the hole in **Figure 2a** (pink dot) so that the beam traveled only through

vacuum and did not have direct physical contact with the SiN<sub>x</sub> surface. In the *SiN<sub>x</sub> exposure* experiment, the beam was positioned to impinge directly onto the SiN<sub>x</sub> surface; this beam location is indicated by the blue dot in **Figure 2a**. In both experiments, an I<sub>ds</sub>-V<sub>ds</sub> curve is first acquired with the electron beam turned off (*i.e.*, closed beam valve). After turning on the beam at the specified position and waiting 3-5 seconds, a series of 4 I<sub>ds</sub>-V<sub>ds</sub> measurements are taken, each with a different beam current: I<sub>beam</sub> = 0.5, 3.4, 9.6, and 23 nA. The I<sub>ds</sub>-V<sub>ds</sub> measurements take 10-12 seconds each and are obtained in random order to reduce sampling bias and systematic errors (see Methods) while a negligible leakage current (< 500 pA) was observed through the SiN<sub>x</sub> membrane (see also current-voltage curves in **Figure 4**). The beam is subsequently turned off and after 3-5 seconds, another I<sub>ds</sub>-V<sub>ds</sub> curve is acquired.

**Figures 2c** and **2d** show the corresponding I<sub>ds</sub>-V<sub>ds</sub> traces for I<sub>beam</sub> = 0.5 (pink), 3.4 (blue), 9.6 (green), and 23 (yellow) nA. Curves taken with the electron beam off (I<sub>beam</sub> = 0 nA) prior to and after these measurements are also given (purple and red curves, respectively). From the slope of each I<sub>ds</sub>-V<sub>ds</sub> trace, we calculate the two-terminal device conductance given by:

$$G = \frac{I_{ds}}{V_{ds}}$$

**Figure 2c** shows that when the beam is passing straight through the hole (*i.e.*, *hole exposure*), the device conductance remains virtually unchanged. A change in TEM-FET conductance due to the electron beam occurs *only* when it hits the SiN<sub>x</sub> surface and can be quantified through:

$$\frac{\Delta G}{G} (\%) = \frac{G_{I_{beam}=0 \text{ nA}} - G_{I_{beam}=23 \text{ nA}}}{G_{I_{beam}=0 \text{ nA}}}$$

Where G<sub>I<sub>beam</sub> = 0 nA</sub> and G<sub>I<sub>beam</sub> = 23 nA</sub> are the conductance values measured under beam currents of 0 and 23 nA, respectively. In the *SiN<sub>x</sub> exposure* experiment (**Figure 2d**), a significant ΔG/G value of 73% is observed when the beam hits the SiN<sub>x</sub> surface. Specifically, the conductance is maximum when the electron beam is off (I<sub>beam</sub> = 0 nA). As I<sub>beam</sub> increases and more electrons hit the SiN<sub>x</sub> per unit time over a fixed beam area (up to 1.8x10<sup>9</sup> electrons per second·nm<sup>2</sup>), the conductance decreases, yielding a minimum conductance for the maximum beam current, I<sub>beam</sub> = 23 nA. Direct interaction between incident electrons and a suspended SiN<sub>x</sub> window generates an additional

electrostatic field and current suppression in the MoS<sub>2</sub> channel. We utilize this phenomenon for further *In Situ* gating of the 2D TEM-FET devices, and explain it below in more detail.

When the drain-source voltage ( $V_{ds}$ ) is fixed and the beam is turned on or off, it takes some time for the 2D channel conductance to respond to this event and asymptotically reach some equilibrium value. This is illustrated by the measurement in **Figure 2b** on the same device where we monitor  $I_{ds}$  as a function of time under a fixed drain-source voltage of 10 mV. The TEM beam with  $I_{beam} = 3.4$  nA is first placed at the location on the SiN<sub>x</sub> window indicated by the blue dot in **Figure 2a**, about 30  $\mu$ m away from the MoS<sub>2</sub> channel. Under this electron beam exposure for 30 seconds, the drain-source current  $I_{ds}$  was first constant (blue curve). When the beam was subsequently turned off (*i.e.*, beam valve closed),  $I_{ds}$  increases rapidly at first before nearly leveling off over a period of 5 minutes (orange curve).

The current vs. time is well described by a limited exponential growth over time:

$$I_{ds}(t) = I_{ds,0} \left[ 1 - e^{-t/\tau} \right]$$

where  $t$  is time,  $\tau$  is a characteristic time constant, and  $I_{ds,0}$  is the steady-state current value. Here, we obtain  $\tau \sim 105$  s. The black line in **Figure 2b** shows a fit of this model to the experimental  $I_{ds}$ - $t$  data. This is consistent with previous studies that observed exponential behavior for charging in SiN<sub>x</sub><sup>26</sup> and suggests the insulating SiN<sub>x</sub> substrate undergoes discharging when the beam is turned off. Similar behavior is also observed when the electron beam is turned on and the 2D channel current decreases exponentially,  $1 + \exp(-t/\tau)$ , as the SiN<sub>x</sub> substrate is charged by the impinging electron beam (**Supplementary Figure S3**).

In general, electron exposure in TEM specimens results in radiation damage through primarily two modes: knock-on collisions and radiolysis.<sup>27–29</sup> Electrically insulating materials such as SiN<sub>x</sub> also experience significant electrostatic charge accumulation. When exposed to the TEM beam, the ejection of secondary and Auger electrons from the insulating specimen leads to a charge imbalance.<sup>29</sup> This electron-deficient, hole-rich SiN<sub>x</sub> membrane subsequently acquires a positive surface potential relative to the MoS<sub>2</sub> flake, leading to current modulation in the 2D channel. In the case of TEM-FETs here (see **Figure 1a**), stronger electron beam exposure results in a more electron-deficient membrane and therefore a larger gating effect. A full discussion of electron-SiN<sub>x</sub> interactions that have been studied here can be found in **Supplementary Section S1**.<sup>30–32</sup>

In order to characterize the gating behavior in the MoS<sub>2</sub> TEM-FET by the electron beam, we next varied the beam location across the window. **Figure 3a** is an optical image of an TEM-FET device with a monolayer MoS<sub>2</sub> flake outlined in white. A broad TEM beam with a constant  $d_{\text{beam}} = 8.7 \mu\text{m}$  was positioned at seven locations indicated by dashed circles on both the MoS<sub>2</sub> flake (yellow) and the bare SiN<sub>x</sub> window (blue). We note that the electron beam was mainly situated on the *Source* side of the MoS<sub>2</sub> channel (**Figure 3a**) such that further experiments are needed to study the similarities and differences in  $\Delta G/G$  when placing the beam on the *Drain* side. A comparison between tightly focused and broad beam exposure conditions is provided later in **Figure 4h**. A series of  $I_{\text{ds}}-V_{\text{ds}}$  curves for different  $I_{\text{beam}}$  were obtained at each location (see also **Supplementary Figure S4**), with the resulting  $\Delta G/G$  values displayed in **Figure 3a**. We observe no correlation between  $\Delta G/G$  and the distance of the electron beam from the MoS<sub>2</sub> channel. For example, the beam locations closest to ( $7.7 \mu\text{m}$ ) and farthest from ( $52 \mu\text{m}$ ) the channel both display  $\Delta G/G = 89\%$  (**Figure 3a**).

However, conductance suppression is observed to be significantly stronger when the electron beam is incident on MoS<sub>2</sub> compared to the bare SiN<sub>x</sub> substrate. We note that the exposed MoS<sub>2</sub> is outside of the transistor channel region, a feature which will be discussed later (see **Figure 4**). **Figures 3b** and **3c** show  $I_{\text{beam}}$ -dependent  $I_{\text{ds}}-V_{\text{ds}}$  data for electron beam exposure to bare SiN<sub>x</sub> and MoS<sub>2</sub>, respectively. Although traces with the beam off ( $I_{\text{beam}} = 0 \text{ nA}$ ) are nearly identical, MoS<sub>2</sub> channel currents with the beam on ( $I_{\text{beam}} \neq 0 \text{ nA}$ ) are substantially lower when the MoS<sub>2</sub> region is exposed (**Figure 3c**). As shown in **Figure 3a**, this behavior is consistent across the TEM-FET, with average  $\Delta G/G$  values of  $90\% (\pm 1.3\%)$  at MoS<sub>2</sub> locations and  $58\% (\pm 2.8\%)$  on SiN<sub>x</sub>. Therefore,  $\Delta G/G$  is relatively constant across the extent of the TEM-FET and is amplified when the electron beam interacts with the semiconducting MoS<sub>2</sub> layer on the insulating window. We also note that negligible differences in  $\Delta G/G$  are observed between cases where the exposed MoS<sub>2</sub> flake is contacted to the source/drain and when it is electrically-isolated (see **Supplementary Figure S5**), suggesting that charge carrier injection from the electron beam to the MoS<sub>2</sub> device channel is insignificant.

In order to accurately quantify the ability of TEM-FET devices to return to their initial conductance values after gating with the electron beam (*i.e.*, hysteresis), we introduce the following parameter that reflects the degree of hysteretic behavior:

$$\frac{\Delta G_{hys}}{G} (\%) = \frac{G_{on,prior} - G_{on,after}}{G_{on,prior}}$$

Where  $G_{on,prior}$  and  $G_{on,after}$  correspond to conductances with the electron beam off ( $I_{beam} = 0$  nA) prior to and after electron beam gating (purple and red curves, respectively). As shown in **Figure 4a**, devices reported until now (**Figures 2** and **3**) have involved positioning of the electron beam outside of the MoS<sub>2</sub> source-drain channel region. The small  $\Delta G_{hys}/G$  values (<2%) exhibited by these systems are within the detectable noise limit of our measurement system (**Supplementary Figure S6**). This indicates that the electron beam gating in these configurations did not affect the TEM-FET's original conductance once the beam was turned off. In contrast, substantially higher hysteresis is measured when the TEM beam is placed on the channel itself, for example the device in **Figure 4b** which displays  $\Delta G_{hys}/G = 53\%$ . We attribute this to defect creation by the 200 keV electron beam implemented in this study, which is known to cause the irreversible formation of S vacancies and a degradation in the electronic transport of MoS<sub>2</sub> and WS<sub>2</sub>.<sup>19,20,33,34</sup>

In addition to probing electron-MoS<sub>2</sub> interactions, we also study the effect of placing the TEM beam outside of the electron transparent window (**Figure 4d**) to highlight the role of suspended SiN<sub>x</sub> in producing the gating effect. As illustrated in **Figure 1a**, the suspended SiN<sub>x</sub> window (orange) containing the source-drain channel is encompassed with Si-supported SiN<sub>x</sub> (light blue), which acts as a robust device platform (see also **Supplementary Figure S7**) and is grounded to the TEM column. **Figures 4e** and **4f** show  $I_{ds}$ - $V_{ds}$  curves when the beam is positioned in these on-window and off-window regions, respectively. Beam placement outside of the window results in no conductance change at all since the underlying Si is relatively conducting and allows charges from electron irradiation to quickly dissipate.<sup>35,36</sup> *In Situ* MoS<sub>2</sub> current modulation is therefore possible only when the beam hits the suspended SiN<sub>x</sub> window region.

To analyze the effects of other TEM beam parameters, we probe device conductance while changing diameter  $d_{beam}$  of the electron beam to vary the size of the region exposed to electrons (**Figure 4g**). With the electron beam placed on the SiN<sub>x</sub> window at a fixed current ( $I_{beam} = 23$  nA), **Figure 4h** shows  $I_{ds}$ - $V_{ds}$  data under tightly focused (green,  $d_{beam} = 10$  nm) and broad beam (gray,  $d_{beam} = 8.7$   $\mu$ m) illumination. A negligible difference in conductance is observed between the two, suggesting that electronic transport in the TEM-FET is not affected by the area of interaction between the incident beam and SiN<sub>x</sub> window as long as the total beam current is constant. We also



note a negligible leakage current ( $< 500$  pA) between the source and drain electrodes through the SiN<sub>x</sub> membrane (**Figure 4i**).

**Figure 5** displays *In Situ* electronic transport characteristics of a typical TEM-FET device where the electron beam is positioned on the SiN<sub>x</sub> window at a distance  $\sim 28$   $\mu\text{m}$  from the 2D channel (this specific configuration is shown in **Figure 1d**). **Figure 5a** contains  $I_{\text{ds}}-V_{\text{ds}}$  curves from a MoS<sub>2</sub> channel with  $I_{\text{beam}}$  from 0 (*i.e.*, electron beam off) to 23 nA. From an initial conductance  $G = 46$  nS at  $I_{\text{beam}} = 0$  nA,  $G$  drops to 37, 29, 24, and 17 nS for beam currents of 0.5, 3.4, 9.6, and 23 nA, respectively. The maximum conductance drop for this device was  $\Delta G/G = 63\%$ . Standard error values for  $G$  and  $\Delta G/G$ , that most likely arise from contact resistance in the transport measurement setup or field fluctuations from electromagnetic lenses within the TEM, are discussed in **Supplementary Figure S6**. The corresponding gating curve showing the dependence of  $I_{\text{ds}}$  on the electron beam current  $I_{\text{beam}}$  is given in **Figure 5b**. Because the current of the electron beam,  $I_{\text{beam}}$ , controls the current through the MoS<sub>2</sub> device, it can be used as the gating parameter (*i.e.*, x-axis in a conventional  $I_{\text{ds}}-V_{\text{g}}$  transistor gating curve). Therefore, the beam current is here to some extent analogous to the gate voltage applied in a traditional transistor. Here, the transistor is in the “*off state*” when the electron beam current is maximal,  $I_{\text{beam}} = 23$  nA, while it is in the “*on state*” with its maximum conductance, when the beam current is minimal,  $I_{\text{beam}} = 0$  nA.

The  $I_{\text{ds}}-I_{\text{beam}}$  curves for varying  $V_{\text{ds}}$  values from 30 to 180 mV show clear transistor characteristics.<sup>37,38</sup> The quality of a FET is conventionally quantified through on/off ratio,  $I_{\text{on}}/I_{\text{off}}$ , which is given by:

$$I_{\text{on}}/I_{\text{off}} = \frac{I_{\text{ds,on}}}{I_{\text{ds,off}}}$$

Where  $I_{\text{ds,off(on)}}$  is equivalent to  $I_{\text{ds}}$  when  $I_{\text{beam}}$  is at maximum (23 nA) and minimum (0 nA) values. The device shown in **Figure 5b** exhibits an  $I_{\text{on}}/I_{\text{off}}$  of 2.7. Under stronger electron beams, higher levels of gating and drain-source current suppression were observed. For example, the TEM-FET displayed in **Figures 5c** and **5d** under an electron beam current of 70 nA exhibits  $\Delta G/G = 94\%$  and  $I_{\text{on}}/I_{\text{off}} = 56$ , significantly higher than values obtained under  $I_{\text{beam}} = 23$  nA. This suggests that a three-fold increase of the beam current leads to an increase in  $I_{\text{on}}/I_{\text{off}}$  by about 20 times. Considering that on/off ratios shown in our study are about five orders of magnitude below conventional MoS<sub>2</sub> FET devices,<sup>38,39</sup> increasing the beam current further is not likely to match the

performance of standard back-gated FETs, and at best, a further increase of beam current by few-fold may increase the on/off ratio by a factor of 10-100. It is possible that this gating effect could be more pronounced by minimizing the contact resistance. While further studies are needed to elucidate the role of electron voltage and different 2D materials, an *In Situ* gating platform without the need for extra electrodes or complex geometries presents opportunities for 2D characterization and nanoelectronics.

## Conclusions

In conclusion, we have reported 2D MoS<sub>2</sub>-based TEM-FETs that enable concurrent structural characterization with electron microscopy and *In Situ* electrical biasing measurements on the same platform. Applying the electron beam to the TEM-FET causes charging of the SiN<sub>x</sub> substrate, which leads to a positive surface potential and current suppression in the biased MoS<sub>2</sub> channel. We show that the magnitude of gating is dependent on the electron beam current but largely decoupled from the position and size of the TEM beam. Under SiN<sub>x</sub> exposure conditions and electrical gating of the 2D channel, the TEM-FET devices exhibit virtually no device hysteresis, maximum  $I_{\text{on}}/I_{\text{off}}$  values up to 56, and clear transistor-like characteristics. The TEM-FET framework can be easily extended to study the electronic transport properties of nanomaterials together with atomic resolution structural and analytical capabilities of electron microscopy.

## Methods

*MoS<sub>2</sub> Growth.* Monolayer MoS<sub>2</sub> was grown using a modified CVD process from a previous work.<sup>40</sup> 1% (w/w) ammonium heptamolybdate ((NH<sub>4</sub>)<sub>6</sub>Mo<sub>7</sub>O<sub>24</sub>) and sodium cholate (C<sub>24</sub>H<sub>39</sub>NaO<sub>5</sub>) solutions were spin-coated onto 300 nm Si/SiO<sub>2</sub> substrates and loaded into a 1 inch diameter tube furnace with 100 mg of sulfur powder. The furnace was heated to 750°C for 15 minutes under a 400 sccm N<sub>2</sub> gas flow and then rapidly cooled to room temperature.

*MoS<sub>2</sub> Characterization.* PL and Raman measurements were obtained at room temperature in an NTEGRA Spectra system under a 532 nm wavelength (green) excitation and < 50  $\mu$ W laser power.<sup>41</sup> An aberration-corrected JEOL 200ARM-CF operating at 200 keV with a high-angle annular dark-field (HAADF) detector was used to acquire STEM images and SAED patterns. STEM images were exposed to an average background subtraction filter to reduce image noise. Additional analysis and detailed defect quantification of pristine MoS<sub>2</sub> material can be found in previous works.<sup>40,42</sup>

*Device Fabrication.* 60  $\mu$ m wide electron-transparent windows were first fabricated using conventional photolithography in 100 nm thick LPCVD-deposited low-stress SiN<sub>x</sub> sitting on 290  $\mu$ m thick <100> Si substrates (Nova Electronic Materials) with an intrinsic resistivity of 1-10  $\Omega$ -cm.<sup>43</sup> 5/40 nm thick Cr/Au contact pads were then patterned around the windows with physical vapor deposition. CVD-grown monolayer MoS<sub>2</sub> flakes were then transferred to the windows using a KOH-based wet etch procedure and electrically connected to the pre-patterned contact pads using electron beam lithography. Al wire bonds then connect these substrates to a custom chip carrier, which is inserted into a 6-lead electrical biasing *In Situ* TEM holder (Hummingbird Scientific).<sup>44</sup> Details and images of this workflow can be found in Supplementary Figure S2.

*TEM Experiments.* *In Situ* measurements were taken in a JEOL F200 operating at 200 keV in HRTEM mode.  $I_{\text{beam}}$  was varied from 0 to 23 nA by changing the spot size (*i.e.*, strength of CL1) and calibrated using an ammeter connected to the instrument's phosphor screen. A vacuum level of approximately  $5 \times 10^{-6}$  Pa was maintained during experiments. The measurements shown in Figure 5c-d were performed on a JEOL 2010F operating at 200 keV in HRTEM mode with  $I_{\text{beam}}$  values from 0 to 70 nA.

*Transport Measurements.* Electronic characterization was performed using two-terminal DC and  $I_{\text{ds}}-V_{\text{ds}}$  measurements with a Keithley 2410 SourceMeter.  $I_{\text{beam}}$ -dependent  $I_{\text{ds}}-V_{\text{ds}}$  sweeps

were acquired in random order to eliminate sampling bias. Unless otherwise noted,  $V_{ds}$  was kept below 200 mV to minimize Joule heating.<sup>17</sup> Measurements were acquired and processed with custom Python and Matlab scripts.

### **Associated Content**

The Supporting Information is available free of charge at <https://pubs.acs.org>.

Additional details of the TEM-FET fabrication process as well as the full set of data for the location-dependent experiment shown in Figure 3. A discussion of electron-SiN<sub>x</sub> interactions including knock-on collisions (K<sup>+</sup> centers) and radiolysis/thermal excitations is provided. Also shown are characteristics of electrically-isolated MoS<sub>2</sub> flakes, DC measurements of SiN<sub>x</sub> membrane charging, and  $I_{ds}$ - $V_{ds}$  curves/optical images for additional devices. Comments on calculated conductance error values are also given.

The authors declare no competing financial interests.

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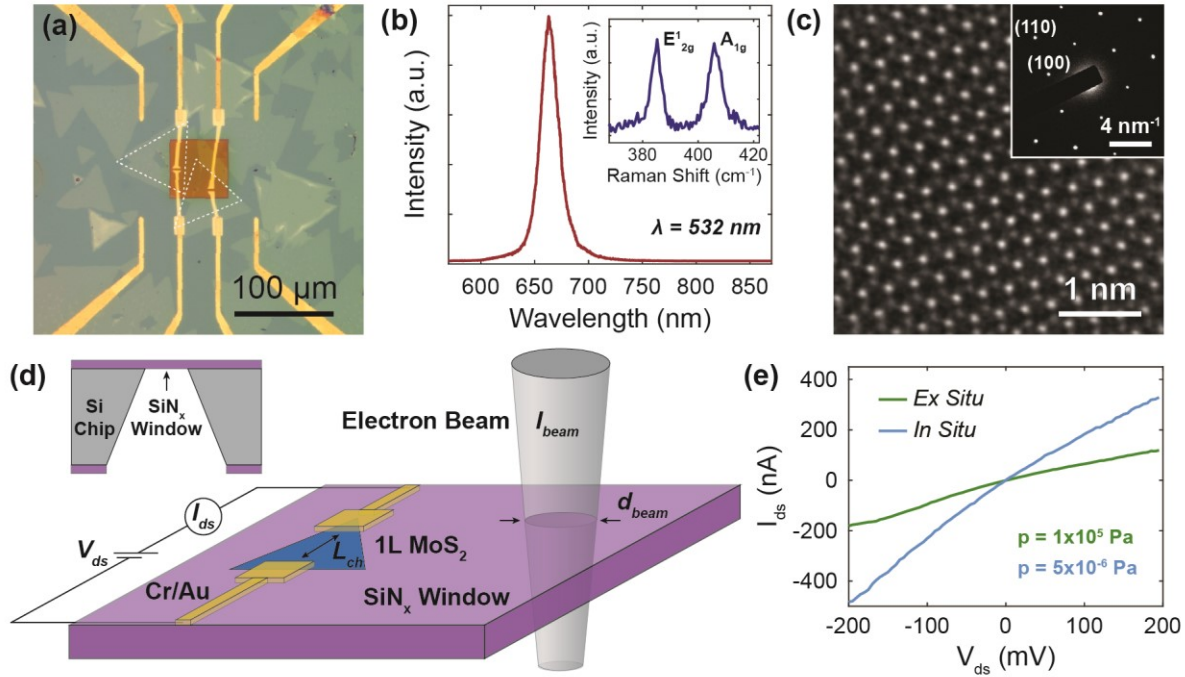
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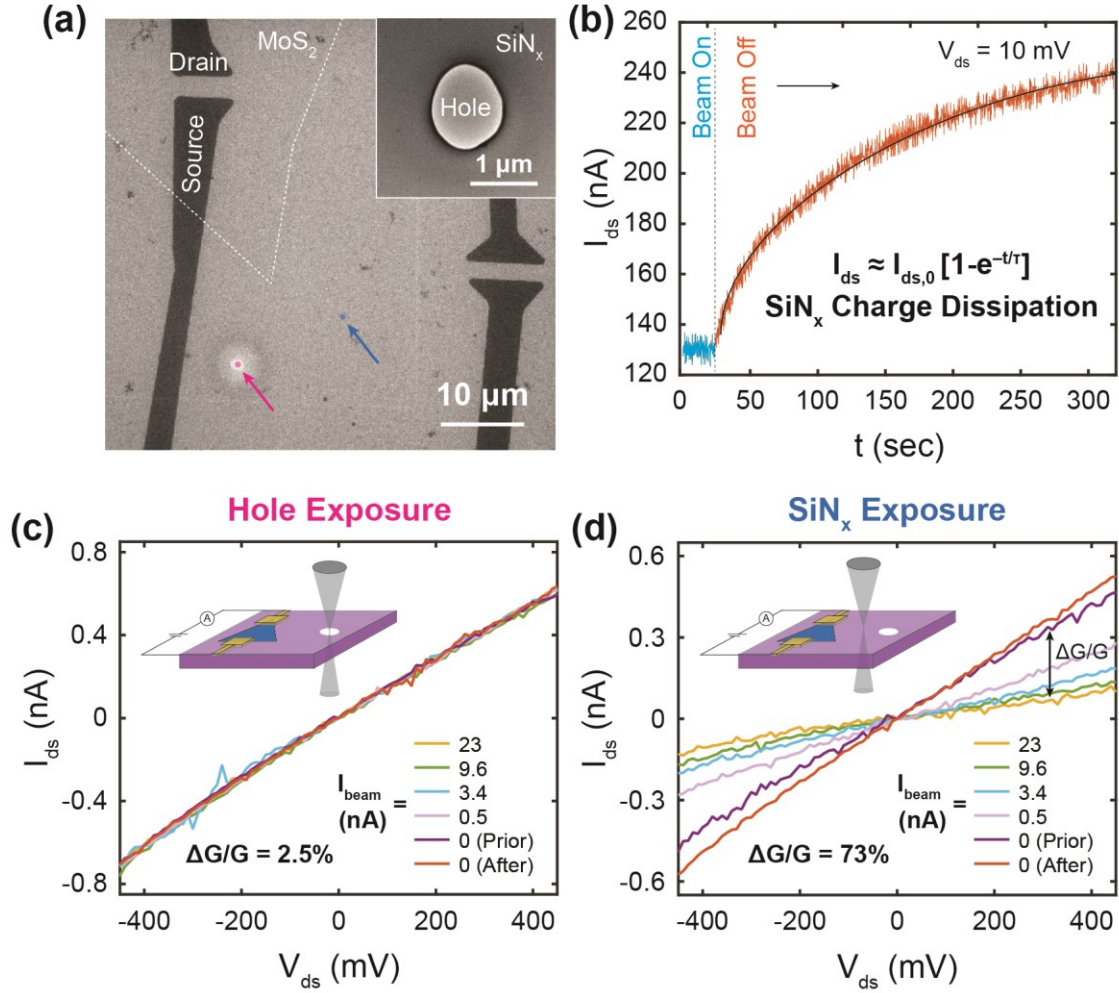
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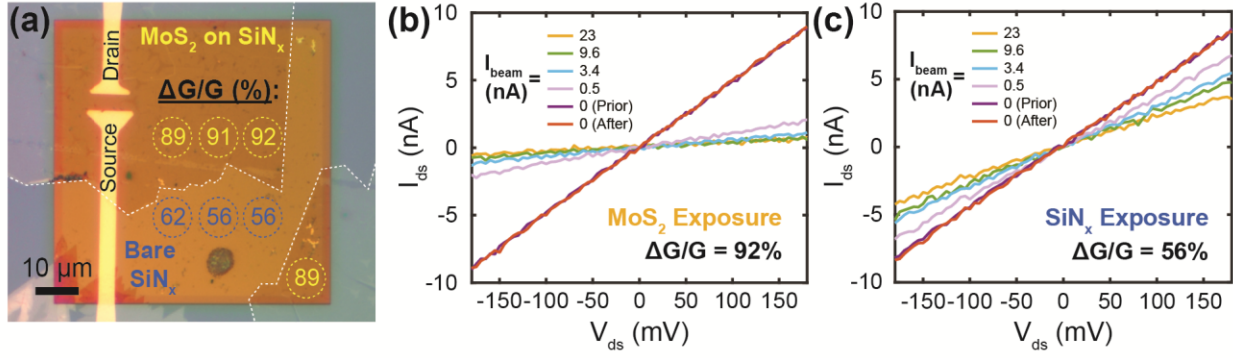


**Figure 1. TEM-FET device architecture, current-voltage measurement, and MoS<sub>2</sub> Raman and TEM characterization.** (a) Optical image of monolayer MoS<sub>2</sub> flakes (outlined in white) transferred onto a 60  $\mu\text{m}$  square SiN<sub>x</sub> window (orange) with top-contacted Cr/Au metallic leads (yellow). (b) Photoluminescence (PL) and (inset) Raman spectra of MoS<sub>2</sub> under an excitation wavelength of 532 nm. The PL peak at 660 nm and Raman mode separation ( $\omega_{\text{A1g}} - \omega_{\text{E2g}}$ ) of 20  $\text{cm}^{-1}$  are indicative of monolayer thickness. (c) High-angle annular dark-field (HAADF) STEM lattice image and (inset) selected area electron diffraction (SAED) pattern of monolayer 2H-phase MoS<sub>2</sub> showing first-order (100) and second-order (110) reflections. (d) Device configuration showing electron beam (gray) exposure on a 100 nm thick SiN<sub>x</sub> window containing a two-terminal MoS<sub>2</sub> device.  $V_{\text{ds}}$ ,  $I_{\text{ds}}$ ,  $L_{\text{ch}}$ ,  $I_{\text{beam}}$ , and  $d_{\text{beam}}$  correspond to drain-source voltage, drain-source current, channel length, electron beam current, and electron beam diameter in the specimen plane, respectively. (Inset) The SiN<sub>x</sub> window sits in the center of a 290  $\mu\text{m}$  thick Si chip (3 mm x 5 mm). Additional fabrication details can be found in **Supplementary Figure S2**. (e) *Ex Situ* and *In Situ*  $I_{\text{ds}}-V_{\text{ds}}$  curves for a MoS<sub>2</sub> TEM-FET at pressure levels of  $1 \times 10^5$  and  $5 \times 10^{-6}$  Pa, respectively, with the electron beam turned off.

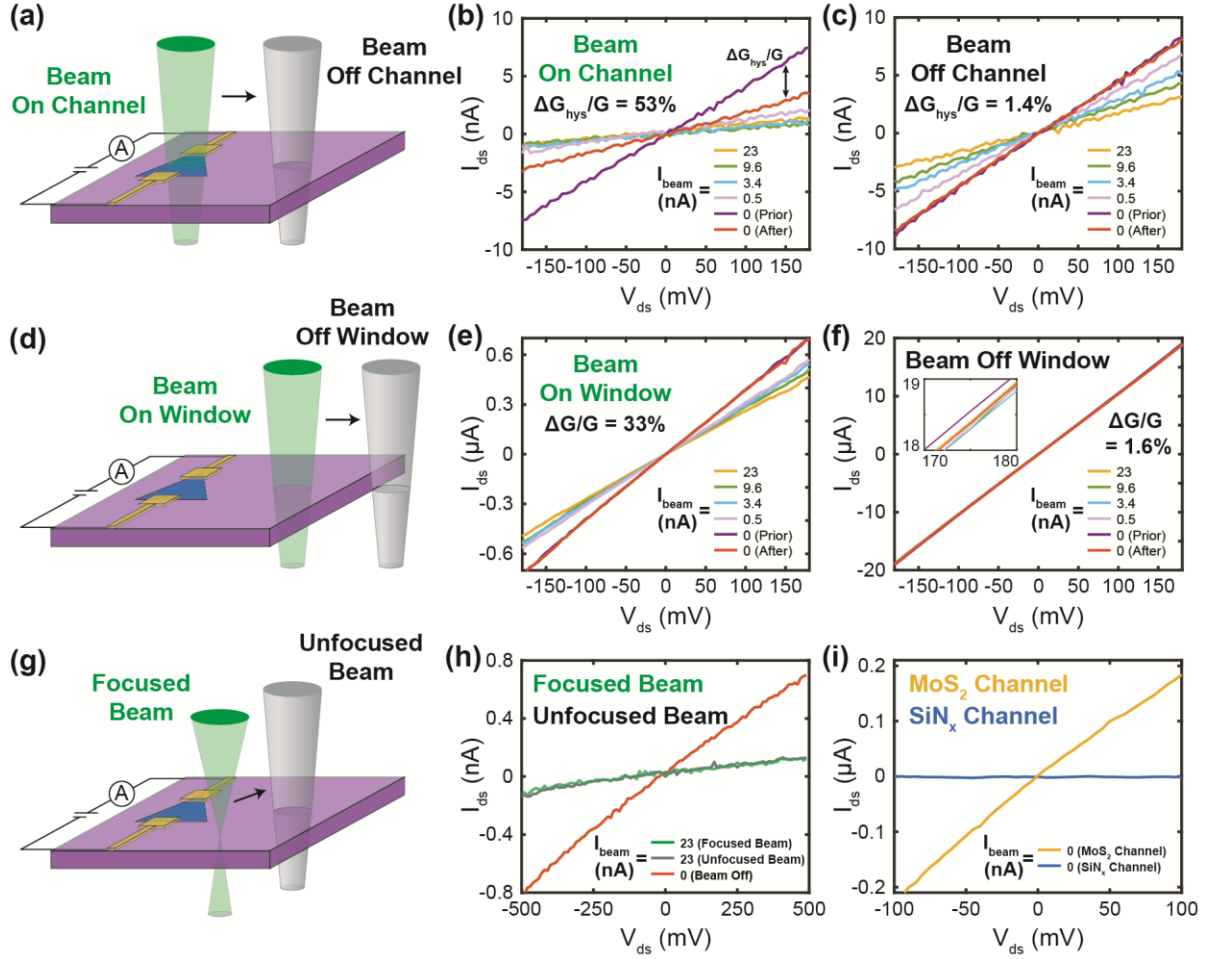


**Figure 2. Charging of the SiN<sub>x</sub> substrate using the electron beam causes MoS<sub>2</sub> gating, and absence of gating if the electron beam is passing through a micron-size hole in the substrate.** (a) Low-magnification TEM image of a TEM-FET SiN<sub>x</sub> window containing a 1.2 μm diameter FIB hole indicated by the pink arrow. The pink and blue holes show the location of the electron beam during  $I_{ds}$ - $V_{ds}$  measurements in (c) and (d), respectively. (inset) High-magnification TEM image of the hole. (b) Continuous DC measurement of  $I_{ds}$  in an TEM-FET over a period of 5 minutes under a constant  $V_{ds} = 10$  mV. After turning the electron beam off (orange), the device current rises and is indicative of electronic charge dissipation. The limited exponential fit is shown as a solid black line. (c-d)  $I_{ds}$ - $V_{ds}$  curves when a focused electron beam ( $d_{beam} = 10$  nm) is placed (c) through the FIB hole and (d) on the SiN<sub>x</sub> window at the locations marked by the pink and blue arrows, respectively, in panel (b). The insets in (c) and (d) provide schematics of the exposure conditions. Conductance,  $G$ , is taken as the slope of each  $I_{ds}$ - $V_{ds}$  curve. Conductance change,

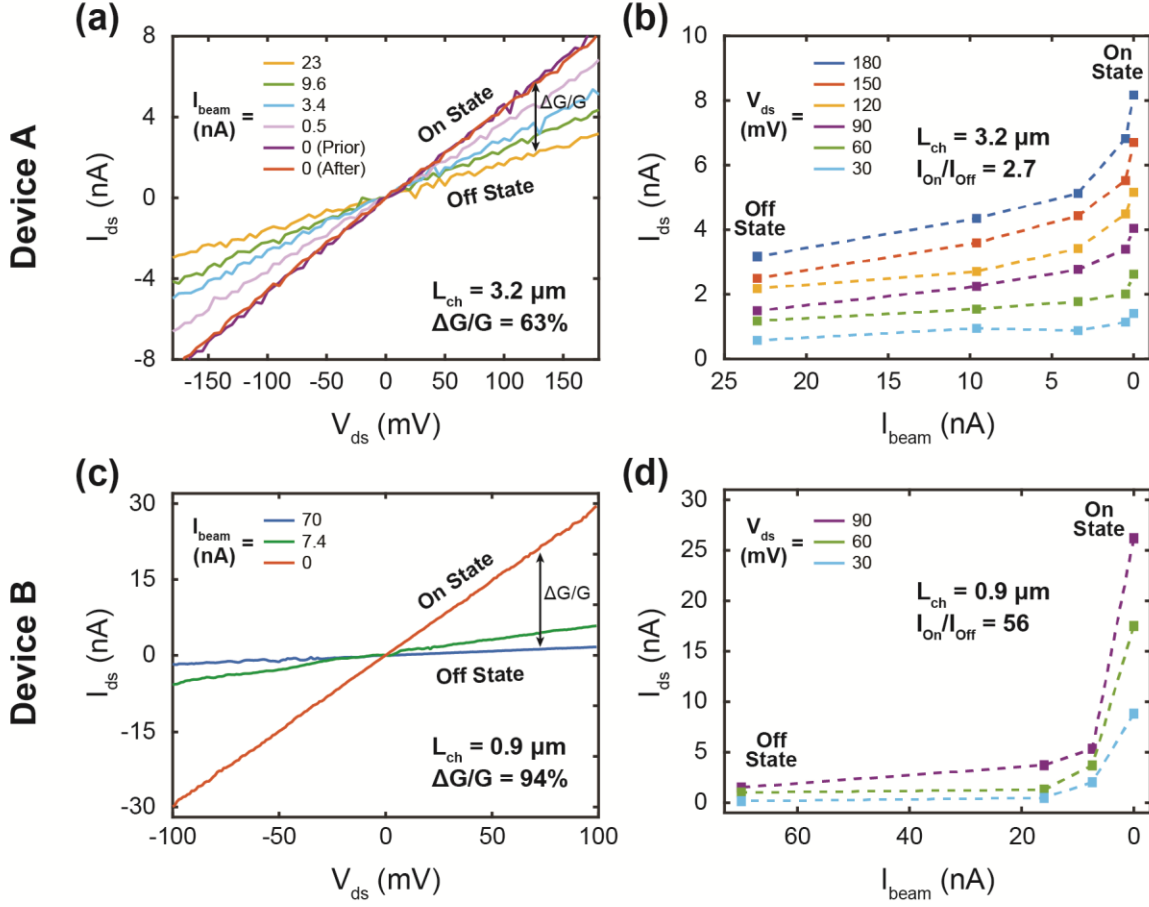
$\Delta G/G$ , is taken as the percent change between the G values of the purple ( $I_{\text{beam}} = 0$  nA) and yellow ( $I_{\text{beam}} = 23$  nA) curves, respectively. No gating effect ( $\Delta G/G = 2.5\%$ ) is observed in the hole exposure condition, which highlights the crucial role of the  $\text{SiN}_x$  substrate in creating a tunable field effect.



**Figure 3. Current-voltage measurements of MoS<sub>2</sub> for several different positions of the electron beam on the insulating SiN<sub>x</sub> substrate.** (a) Optical image of an TEM-FET showing  $\Delta G/G$  values as a function of electron beam position on the SiN<sub>x</sub> window. Each number corresponds to a  $\Delta G/G$  value (%) obtained while the encircled area (dashed circle) was exposed to a TEM beam ( $d_{\text{beam}} = 8.7 \mu\text{m}$ ). Yellow and blue values correspond to exposure on areas of the SiN<sub>x</sub> window with and without monolayer MoS<sub>2</sub> (outlined in white), respectively. Due to a stronger field effect, higher  $\Delta G/G$  values are observed when the electron beam is parked on a region containing MoS<sub>2</sub> (b) Example  $I_{\text{ds}}-V_{\text{ds}}$  curves for electron beam exposure on a bare SiN<sub>x</sub> window with  $\Delta G/G = 56\%$ . (c)  $I_{\text{ds}}-V_{\text{ds}}$  curves under electron beam exposure to an MoS<sub>2</sub>-covered region with resulting  $\Delta G/G = 92\%$ .  $I_{\text{ds}}-V_{\text{ds}}$  curves for all locations indicated in panel (a) can be found in **Supplementary Figure S4**.



**Figure 4. TEM-FET current-voltage characterization as a function of beam position and size: on and off the MoS<sub>2</sub> channel, on and off the suspended SiN<sub>x</sub> region, and focused vs. unfocused illumination.** (a) Schematic and (b-c) transport characteristics when the electron beam is parked on (green) and off (black) of the MoS<sub>2</sub> device channel (gray). Electron beam exposure to the transistor channel results in a degree of hysteresis ( $\Delta G_{hys}/G = 53\%$ ) due to the irreversible damage to the MoS<sub>2</sub> from the creation of sulfur vacancies in the conduction region. (d) Schematic and (e-f)  $I_{ds}$ - $V_{ds}$  curves for on- (green) and off-window (black) electron beam irradiation. Compared to exposure on the window ( $\Delta G/G = 33\%$ ), a negligible degree of gating ( $\Delta G/G = 1.6\%$ ) is seen when the beam is placed off the window because of the absence of an electric field. (g) Schematic and (h) electronic characteristics of focused (green,  $d_{beam} = 10$  nm) and unfocused (gray,  $d_{beam} = 8.7$   $\mu$ m) beam placement on the TEM-FET window. No difference in conductance is observed between the two conditions. (i)  $I_{ds}$ - $V_{ds}$  curves for separate two-terminal devices with MoS<sub>2</sub> (yellow) and bare SiN<sub>x</sub> (blue) channels. Electronic current is only detected through MoS<sub>2</sub> material.



**Figure 5. *In Situ* current-voltage curves and on/off gating characteristics of MoS<sub>2</sub>-based TEM-FETs.** (a)  $I_{ds}$ - $V_{ds}$  curves as a function of  $I_{beam}$  for a MoS<sub>2</sub> device with  $L_{ch} = 3.2 \mu\text{m}$ .  $G$  is observed to decrease at larger  $I_{beam}$  values due to a stronger field effect. The sample shown in (a) exhibited  $\Delta G/G = 63\%$ . Curves obtained before and after  $I_{ds}$ - $V_{ds}$  sweep measurements under no electron beam exposure are also shown in purple and red, respectively, to demonstrate the absence of device hysteresis. (b)  $I_{ds}$ - $I_{beam}$  gating curve as a function of  $V_{ds}$  for the same device. Transistor on/off ratio,  $I_{on}/I_{off}$ , is taken as the ratio of  $I_{ds}$  values between the TEM-FET *on* ( $I_{beam} = 0$  nA) and *off* ( $I_{beam} = 23$  nA) states, which are indicated in panels (a)-(d). The curve in (b) shows an  $I_{on}/I_{off}$  of 2.7. (c)  $I_{ds}$ - $V_{ds}$  and (d)  $I_{ds}$ - $I_{beam}$  curves for a different sample showing a higher  $I_{on}/I_{off}$  of 56 under a stronger electron beam (70 nA). In (d), the device *off* state is taken as  $I_{beam} = 70$  nA.

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