Voltage Balancing Control with Active Gate Driver for Series Connected SiC MOSFETs

Inhwan Lee, Lu Yue, Xiu Yao
Electrical Engineering
State University of New York at Buffalo
Buffalo, USA
Email: inhwanle@buffalo.edu

***Abstract*—Silicon carbide (SiC) device is expected to replace silicon (Si) device in many high voltage and power application due to potentially higher switching frequency and voltage capabilities. Even though its potential voltage capability, the highest voltage rating of a single commercial SiC MOSFET is 1.7 kV. An alternative method to achieve higher voltage is a device series connection. However, it causes a voltage unbalance issue during turn-off state that can harm the devices. Therefore, the voltage balancing control (VBC) must be considered in device series connection. In this paper, a VBC method with active gate driver (AGD) is proposed. A gate resistance modulation method with a signal time delay is adopted for dynamic voltage sharing. The proposed method is experimentally verified.**

Keywords— Wide bandgap (WBG) device; Silicon carbide (SiC) MOSFET; Series connection; Voltage balancing control; Active gate driver.

I. INTRODUCTION

Si is the most commonly used material in power electronic devices. However, the physical property of the material limits the performance of power device regarding switching frequency and blocking voltage. To achieve higher switching frequency and voltage capability, wide band gap (WBG) materials, such as SiC and gallium nitride (GaN), have been recently under extensive research and development. WBG materials have higher energy gap, electric field, and electron velocity that allow to achieve higher voltage and switching frequency capability. Therefore, it is expected that WBG device will provide higher breakdown voltage maintaining the same size and on-resistance in comparison to Si device. This will significantly shrink the size of power devices and reduce the power loss at the same time. Besides, because of thermal characteristics, it is more appropriate in high temperature applications [1].

Especially, SiC device is expected to replace the Si device in many high voltage converter and power application. Even though the potential voltage capability of SiC material is higher than Si, the highest voltage rating of a commercial single SiC MOSFET is 1.7 kV. To achieve higher voltage with commercial WBG device, a series connection of discrete device is promising alternative. However, it causes a critical problem which is a voltage unbalance issue that can harm the devices. The unbalance can be caused by differences of device capacitances and mismatch in device turn-off times due to delay of external gate drive circuit [2]. Therefore, a VBC is necessary in device series connection.

In general, the VBC for device series connection consists of gate-side control and drain-side control [3]. For the gate-side control method, DSP and FPGA based control techniques are studied in [4]–[7]. The external balancing circuits to the gate-side are also proposed in [8], [9]. The other method is drain-side control. A passive snubber circuits are commonly used in drain-side control. A snubber circuit is proposed and verified with different devices [2], [10]. Optimization of RC value is significant to optimize switching loss and voltage overshoot. The algorithm for optimal RC value selection is studied in [11]. Gate-side method is complicated to implement and the drain-side method such as the passive snubber circuit causes considerable losses by itself.

With the emergence of WBG device, the AGD has been widely studied to optimize switching speed and energy loss. Due to fast switching speed of WBG device, the dynamic characteristic of WBG device is more sensitive to parasitic component of device and printed circuit board than Si device. It results in oscillation and overshoot issues of voltage and current. By controlling the injected gate current, the undesirable effects can be diminished. The gate current can be controlled by modulating gate resistance values during switch-

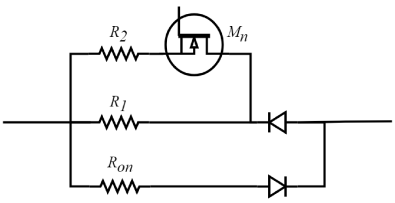

Figure 1. Active gate driver circuit for dynamic voltage balancing

978-1-7281-0395-2/19/$31.00 ©2019 IEEE

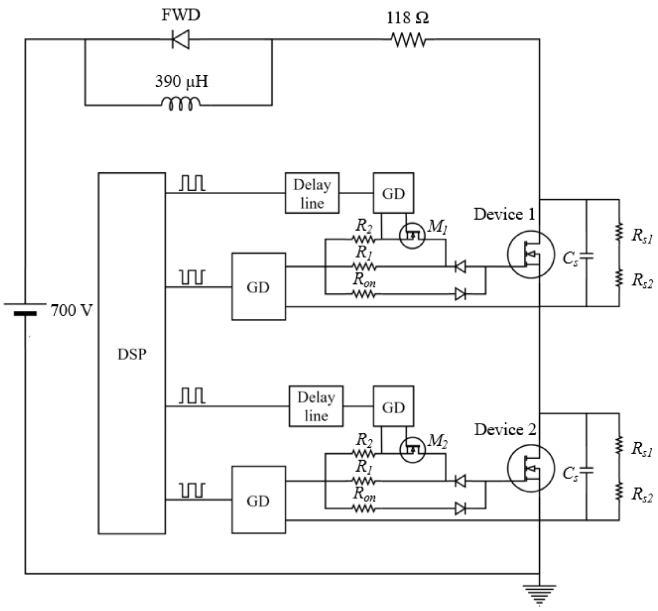

Figure 2. Circuit configuration of device series connection with AGD

ing transient. The multiple-stage gate resistance modulation techniques are proposed in [12], [13] and a gate impedance modulation technique is studied in [14].

In this paper, a VBC with AGD for device series connection is proposed. The AGD modulates the turn-off gate resistance (R_{off}) with signal time delay technique for voltage balancing. The rest of this paper is organized as follows: In Section II, the circuit configuration and operation principle is described; in Section III, the proposed VBC with AGD is presented; in Section IV, the proposed VBC is experimentally verified; finally, Conclusion and future work in Section V.

II. Circuit Configuration and Operation Principle

A main idea of the proposed VBC with AGD is to modulate the R_{off} with signal time delay of auxiliary switch. It is first proposed and verified in LTspice simulation [15]. A two stage gate resistance modulation technique is adopted for AGD as shown in Fig. 1. It consists of three resistors (R_{on}, R_1, and R_2) and one auxiliary MOSFET (M_n). R_{off} is modulated during turn-off transient for voltage balancing. When M_n is turned-off, R_{off} has resistance value of R_1. If M_n is turned on, the R_1 and R_2 are connected in parallel,

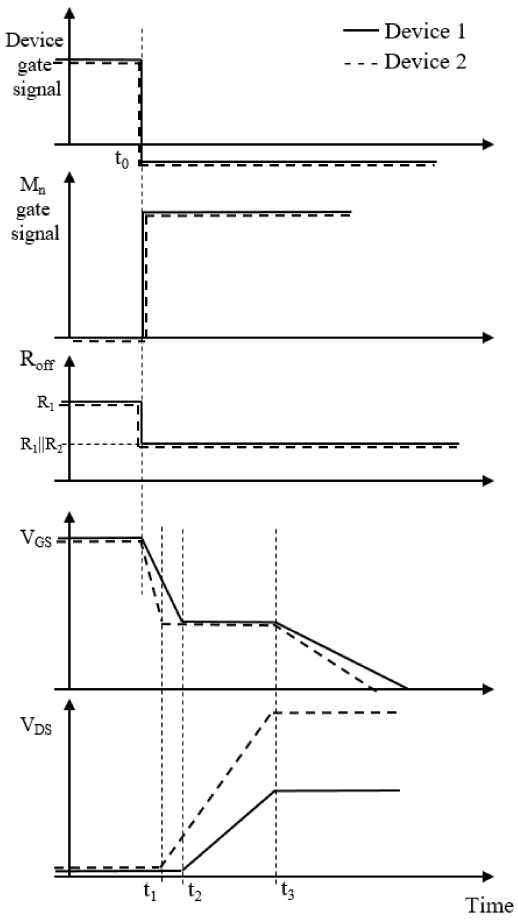

Figure 3. Switching waveforms without VBC

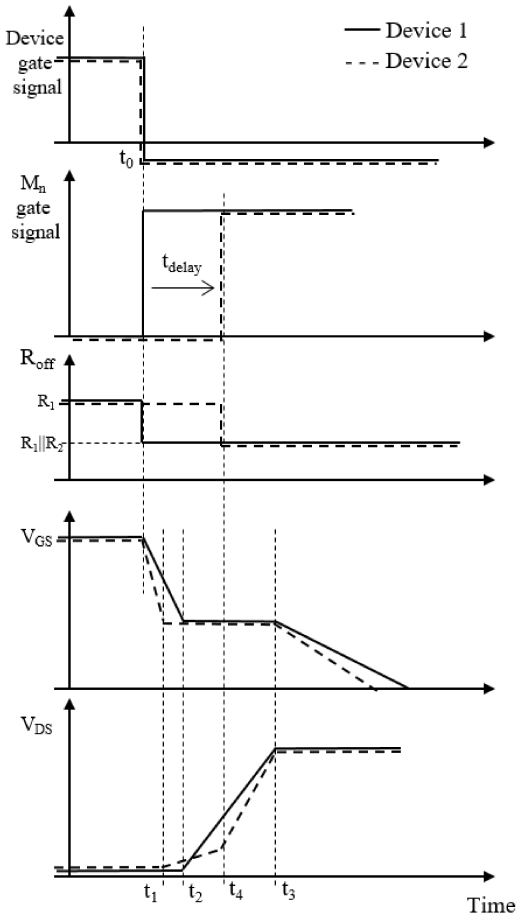

Figure 4. Switching waveforms with VBC

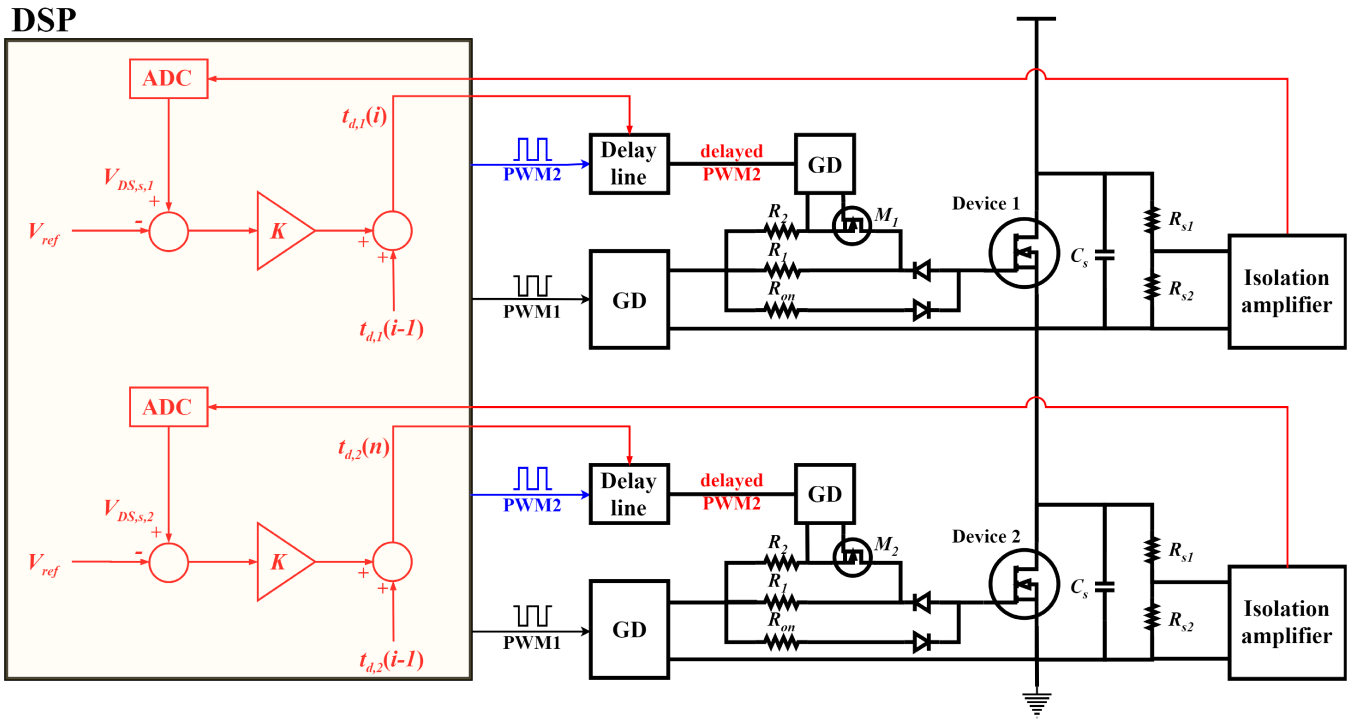

Figure 5. The proposed VBC with AGD control schematic of series connected SiC MOSFETs

then R_{off} becomes $R_1 \| R_2$. In consequence, R_{off} has two different resistance values by controlling M_n. It is known that higher gate resistance (R_g) reduces dv/dt with lower gate current, and lower R_g increases dv/dt with higher gate current. Different dv/dt affects to the voltage unbalance in device series connection. By modulating R_{off}, dv/dt can be adjusted to achieve voltage balancing.

Fig. 2 shows circuit configuration of device series connection with AGD. Two SiC MOSFETs, Device n (n=1, 2), are connected in series and the proposed AGDs are connected to the gate side. Fig. 3 and 4 show the basic principle of the VBC with AGD. As shown in Fig. 3, the two devices are turned off at t_0 while the M_n is turned on at the same time. It results in the decrease of R_{off} from R_1 to $R_1 \| R_2$. Without the VBC, the voltages will be unbalanced. Even though the two devices are turned off simultaneously, dv/dt of the two devices will be different due to the differences in the parasitic parameters of MOSFETs. In order to balance the voltages, dv/dt can be controlled by modulating R_{off} values. Basically, the idea is to delay the M_n gate signal of the device whose voltage needs to be decreased. For example, $V_{DS,2}$ is required to be decreased to balance voltages in Fig. 3. Therefore M_2 gate signal is delayed as shown in Fig. 4. The signal is delayed by t_{delay} which means R_{off} of device 2 keeps higher value (R_1) during $t_1 - t_4$. It results in low dv/dt during the period. Then, the dv/dt is increased at t_4 to achieve voltage balancing. The gate signal of the two main devices are not adjusted. Only M_n gate signals are delayed to control dv/dt by modulating the value of R_{off}.

III. Voltage Balancing Control with Active Gate Driver

The proposed VBC with AGD control schematic is shown in Fig. 5. The PWM signals for SiC MOSFETs (PWM1) and auxiliary switches (PWM2) are generated by DSP. The two PWMs are complementary. The device voltage sensing part consists of a isolation amplifier and a voltage divider (R_{s1}, R_{s2}) to scale down the device voltages. The measured voltages are converted to digital signal through analog to digital converter (ADC) in DSP.

The converted scaled down device voltages ($V_{DS,s,n}$) are compared with reference voltage (V_{ref}). The voltage difference between $V_{DS,s,n}$ and V_{ref} is multiplied by gain (K) to calculate the delay time to compensate the unbalanced voltage in current switching cycle. Then, the calculated time delay is added to the time delay of previous switching cycle ($t_{d,n}(i-1)$) to obtain the updated time delay ($t_{d,n}(i)$). The following equation is the updated time delay;

$$t_{d,n}(i) = t_{d,n}(i-1) + K(V_{DS,s,n} - V_{ref})$$

,where i is the order of switching cycle. K is designed as positive value unless $V_{DS,s,n} - V_{ref}$ is negative which means the time delay of PWM is not required. In this case, K is set as zero in DSP. An 8-bit programmable timing element is used to digital delay line. Fig. 6 shows waveforms of the complementary PWM signals and a delayed PWM signal. DSP controls the delay time in every switching cycle depending on the calculated delay time ($t_{d,n}(i)$). A 20 ns delay is shown in Fig. 6 as an example.

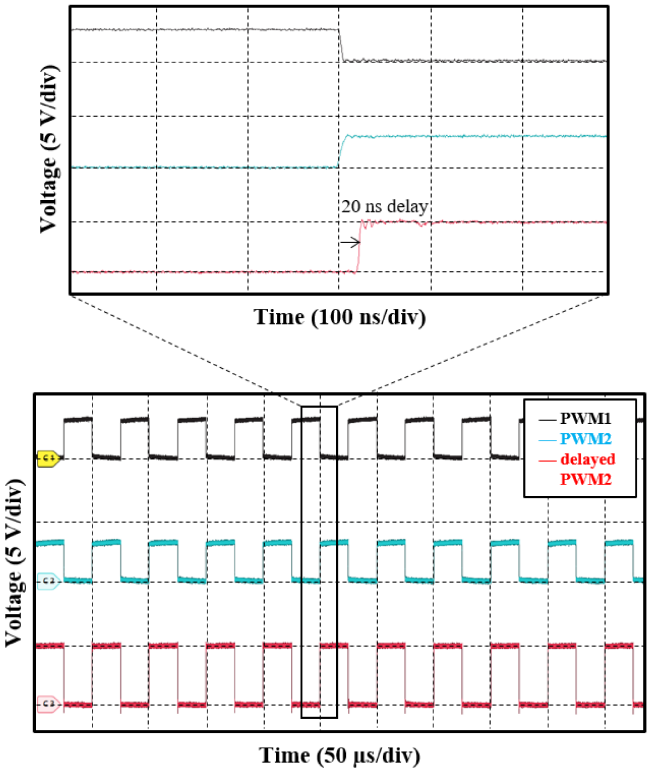

Figure 6. Complementary PWM signals and a 20 ns delayed PWM with delay line

IV. Experimental Result

The test circuit configuration of device series connection is shown in Fig. 2. A Rohm semiconductor 650 V SiC MOSFET (SCT3120AL) is adopted for this test [16]. System parameters of the voltage balancing test circuit are listed in Table I. A system DC voltage is 700 V, and a load current is designed as 5.9 A with 118 Ω load resistor. A switching frequency of the system is 20 kHz.

Table I. Test circuit parameters

Parameters	Value	Parameters	Value
DC voltage	700 V	Load current	5.9 A
Load resistance	118 Ω	Switching frequency	20 kHz
R_{on}	5 Ω	C_s	440 pF
R_1	200 Ω	R_{s1}	750 kΩ
R_2	1 Ω	R_{s2}	2.2 kΩ

R_1 is designed as large resistance to make the difference of R_1 and $R_1 \| R_2$ larger which affects to the difference of dv/dt. Even though R_1 is large, R_{off} is a small value which is $R_1 \| R_2$ (1.005 Ω) during most of turn-off transient. Therefore, it is expected that the increase of switching loss due to the AGD is negligible. A TI DSP TMS320F28335 is used in this test. A sample rate of ADC in DSP is designed as 400 kHz. A test setup of the experiment is shown in Fig. 7 and elements of the experimental setup is listed in Table II.

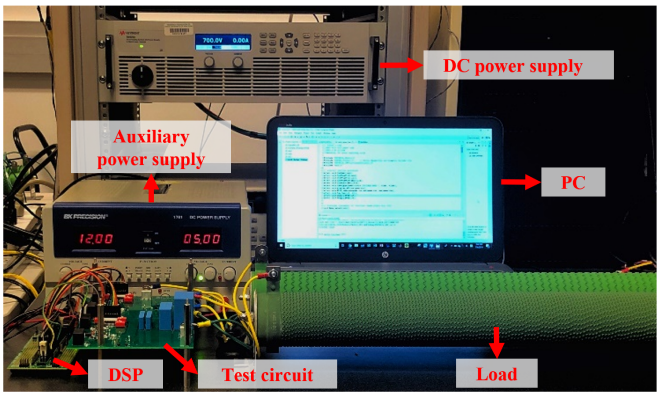

Figure 7. Experimental test setup

Table II. Elements of experimental setup

Elements	Part No.	Specification
SiC MOSFET	SCT3120AL	650 V, 21 A
SiC diode	C4D20120D	1200 V, 33 A
Delay line	DS1023S	1 ns/step
DSP	TMS320F28335	32 bit, 150 MHz
ADC	DSP (TMS320F28335)	12 bit resolution
Iso. amplifier	AMC1311	2.1 µs delay

Fig. 8 shows the unbalanced voltages at $V_{DS,1}$=220 V and $V_{DS,2}$=480 V in series connection without VBC. With the proposed VBC method, the voltage balancing is achieved as shown in Fig. 9 and 10. The voltages are balanced in 150 µs which is in three switching cycles at K=0.52 gain. With optimized gain K=0.87, the voltage balancing is achieved after one switching cycle (50 µs). The experimental results have verified the effectiveness of the proposed VBC with AGD.

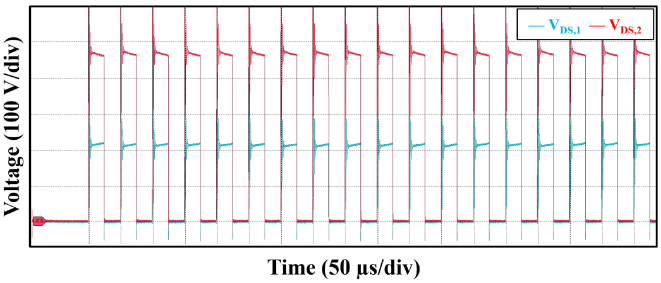

Figure 8. Unbalanced voltages without VBC

V. Conclusion and Future Work

An AGD control technique is proposed for voltage balancing in device series connection. The main idea of the proposed VBC is to modulate R_{off} with PWM signal time delay of

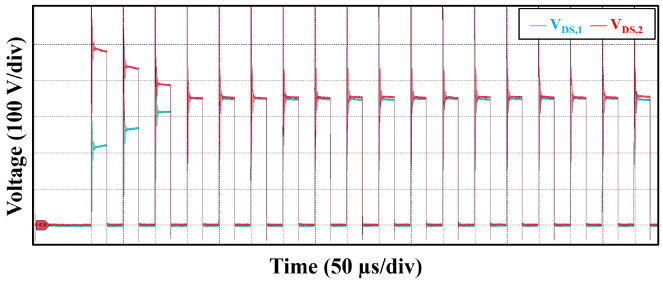

Figure 9. Balanced voltages with the proposed VBC at K=0.52

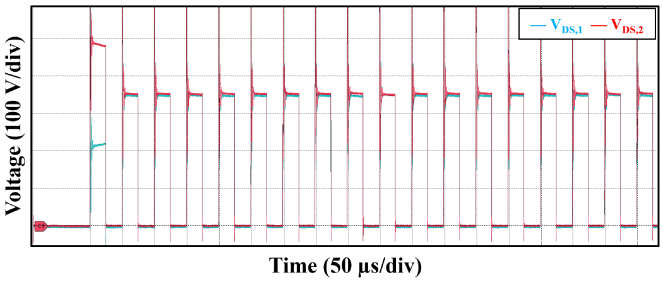

Figure 10. Balanced voltages with the proposed VBC at K=0.87

auxiliary MOSFET. The proposed method is experimentally validated with series connected SiC MOSFETs. The Rohm 650 V SiC MOSFET is used and DC voltage of the system is 700 V at 5.9 A load current. The voltage balancing is achieved after one switching cycle (50 µs) with optimal gain. For future work, switching loss analysis and higher switching frequency will be studied. The proposed VBC will be also tested with a higher number of series connected devices.

ACKNOWLEDGMENT

This material is based upon work supported by the National Science Foundation under grant no. ECCS 1711659.

REFERENCES

[1] M. Sasagawa, T. Nakamura, H. Inoue, and T. Funaki, "A study on the high frequency operation of DC-DC converter with SiC DMOSFET," pp. 1946–1949, June 2010.

[2] K. Vechalapu and S. Bhattacharya, "Performance comparison of 10 kV x2013;15 kV high voltage SiC modules and high voltage switch using series connected 1.7 kV LV SiC MOSFET devices," pp. 1–8, Sept 2016.

[3] N. Y. A. Shammas, R. Withanage, and D. Chamund, "Review of series and parallel connection of IGBTs," *IEE Proceedings - Circuits, Devices and Systems*, vol. 153, no. 1, pp. 34–39, Feb 2006.

[4] K. Wada and K. Shingu, "Voltage Balancing Control for Series Connected MOSFETs Based on Time Delay Adjustment Under Start-Up and Steady-State Operations," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 5495–5499.

[5] P. Wang, F. Gao, Y. Jing, Q. Hao, K. Li, and H. Zhao, "An Integrated Gate Driver with Active Delay Control Method for Series Connected SiC MOSFETs," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2018, pp. 1–6.

[6] S. Ji, F. Wang, L. M. Tolbert, T. Lu, Z. Zhao, and H. Yu, "An FPGA-Based Voltage Balancing Control for Multi-HV-IGBTs in Series Connection," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4640–4649, Sep. 2018.

[7] Z. Zhang, H. Gui, J. Niu, R. Chen, F. Wang, L. M. Tolbert, D. J. Costinett, and B. J. Blalock, "High Precision Gate Signal Timing Control Based Active Voltage Balancing Scheme for Series-Connected Fast Switching Field-Effect Transistors," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 925–930.

[8] A. Marzoughi, R. Burgos, J. Wang, and D. Boroyevich, "Dynamic voltage balancing method for fast-switching SiC MOSFETs with high dv/dt rates," in *2017 IEEE Southern Power Electronics Conference (SPEC)*, Dec 2017, pp. 1–6.

[9] C. Abbate, G. Busatto, and F. Iannuzzo, "High-Voltage, High-Performance Switch Using Series-Connected IGBTs," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2450–2459, Sept 2010.

[10] K. Vechalapu, S. Bhattacharya, and E. Aleoiza, "Performance evaluation of series connected 1700V SiC MOSFET devices," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2015, pp. 184–191.

[11] K. Vechalapu, S. Hazra, U. Raheja, A. Negi, and S. Bhattacharya, "High-speed medium voltage (MV) drive applications enabled by series connection of 1.7 kV SiC MOSFET devices," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 808–815.

[12] A. Negi, "Two-stage Active Gate Driver for SiC MOSFET," 2016.

[13] P. Nayak and K. Hatua, "Active Gate Driving Technique for a 1200 V SiC MOSFET to Minimize Detrimental Effects of Parasitic Inductance in the Converter Layout," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1622–1633, March 2018.

[14] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1986–1997, April 2014.

[15] I. Lee and X. Yao, "Active Gate Control for Series Connected SiC MOSFETs," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 453–457.

[16] SCT3120AL N-Channel Silicon Carbide Power MOSFET. [Online]. Available: `https://www.rohm.com/`