Distributed Spintronic/CMOS Sensor Network for Thermal Aware Systems

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***Abstract*—Recent developments in IC technology rely on device scaling and 3-D integration, resulting in billions of devices compacted into a small area. These trends degrade the system lifetime and reliability due to an increase in temperature caused by high power densities. Dynamically managing a system based on the thermal characteristics is important to mitigate this issue. An on-chip thermal aware system composed of hundreds of distributed thermal sensors is proposed. A hybrid spintronic/CMOS-based thermal sensor is described that exploits the thermal response and small area of an antiparallel magnetic tunnel junction. The sensor cell consumes as little as 500 pJ to read 1,024 thermal sensor nodes and generates a thermal map of a system composed of 32×32 thermal sensors. The sensor cell exhibits a thermal linearity (R^2) up to 0.983 and a thermal sensitivity of 1.91 mV/K over the commercial temperature range of 0^{o}C to 85^{o}C while consuming 32 μW.**

***Index Terms*—MTJ, thermal aware system, thermal sensor, spintronic, thermal management system.**

I. INTRODUCTION

Two primary methods are used to achieve next generation integrated systems, a large number of deeply scaled devices and die stacking. High power densities and thermal issues such as long heat conduction paths are produced, which, in turn, can dramatically degrade performance, reliability, and system robustness while increasing leakage currents [1], [2]. To manage the system workload and protect the system from overheating, methods such as allocating heat conduction paths and specialized cooling systems are used [3], [4]. These systems need to be supported with a temperature aware capability to allocate and properly respond to critical hot spots.

A thermal aware system can be achieved by distributing a large number of on-chip thermal sensors. These on-chip thermal sensors should be small in size, low power, high speed, temperature sensitive, and accurate over a wide temperature range. The on-chip thermal sensors should be appropriately placed to capture local hot spots. The location of the thermal sensors depends upon the sensor characteristics, system requirements, IC package, and cooling techniques [5].

A small number of thermal sensor nodes are typically located around an IC, particularly near potential hot spots to support a thermal aware system. For instance, Intel utilizes one thermal sensor per core in the Xeon 5400 series [6], while 25 thermal sensors are embedded within the IBM POWER6 processor [7]. The use of a few thermal sensors, however, limits the ability to fully monitor the significant spatial and dynamic temperature variations across an integrated system [8]. Thermal aware systems manage the locally distributed thermal sensor nodes around an IC, dynamically controlling the system workload [8], [9], [10]. These systems, however, utilize a software-based management system which do not respond to individual thermal sensor nodes. In addition, the response time of these software solutions is long and consumes significant power; hence hardware solutions are desirable. In this paper, an integrated system to support a thermal aware capability, shown in Figure 1, is proposed, where multiple thermal sensor nodes are distributed across an IC.

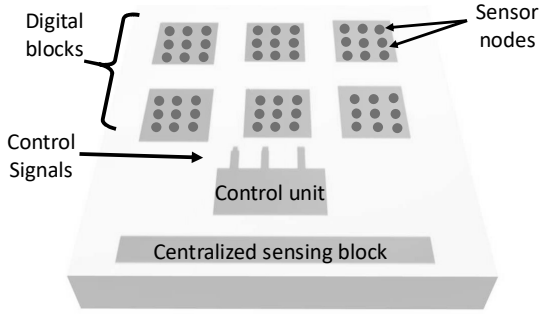

Fig. 1: Distributed thermal network system

The distributed thermal sensor nodes communicate with a centralized sensing unit which collects temperature information from the individual sensor nodes, producing a thermal map of the system. A hybrid spintronic/CMOS-based analog thermal sensor is proposed here where the high temperature sensitivity of the magnetic tunnel junction (MTJ) antiparallel resistance is exploited. The sensor output is compared with a reference source, as shown in Figure 3 [4]. The analog thermal sensor behaves as a threshold temperature-based sensor, triggering a signal if the temperature (or voltage) exceeds a certain reference temperature (or voltage).

Several papers discuss thermal sensors using spintronic technology [11], [12]. In [11], a patent describes the use of an MTJ as a thermal sensor by sensing the change in the resistance of an MTJ to temperature. [11] does not describe a thermal sensor, guidelines for using an MTJ as a thermal sensor, or the distinctive behavior of the P and AP resistance of an MTJ to temperature. In [12], the influence of temperature on the probability of device switching is noted. Sensing a change in the switching probability requires additional circuitry. In this work, the temperature is measured by a change in the antiparallel resistance.

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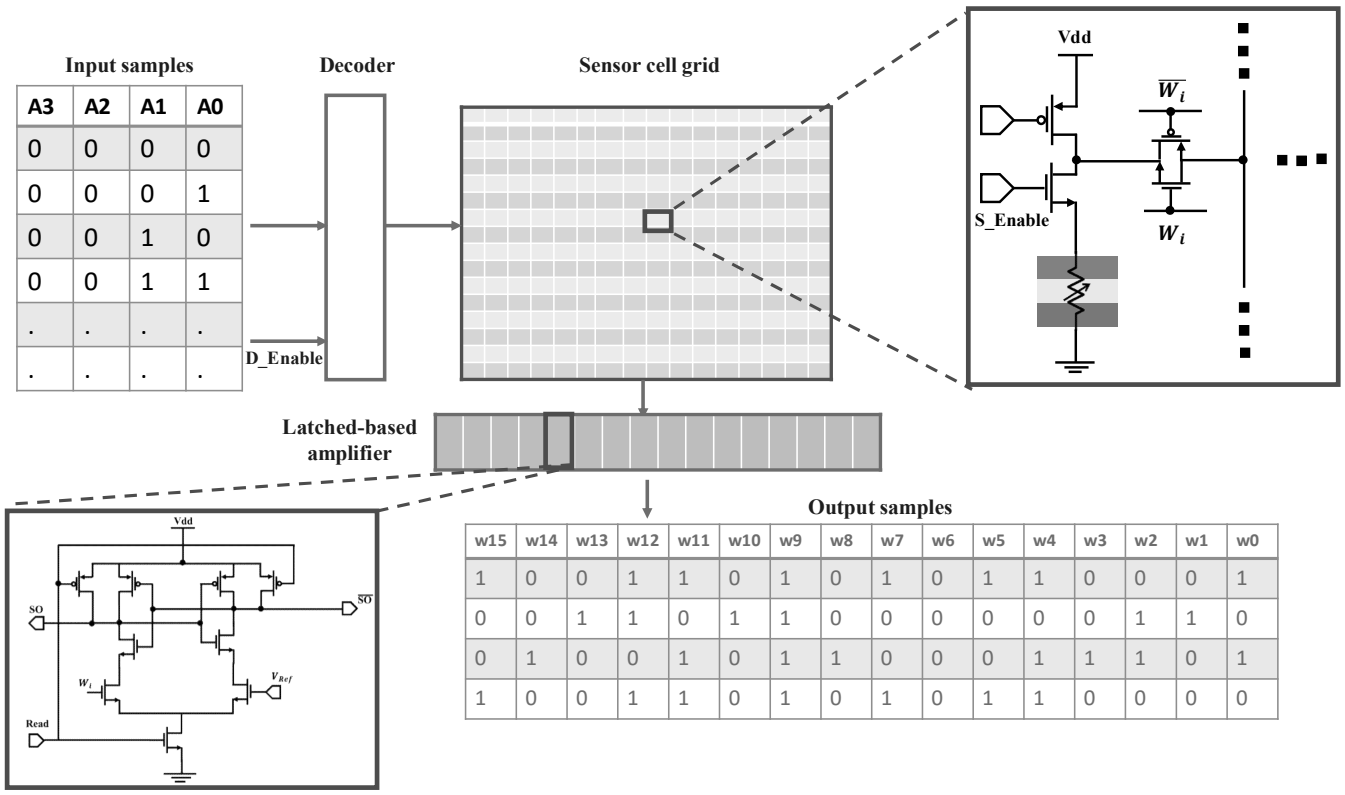


Fig. 2: Proposed thermal aware system. The system input chooses the row being read through a decoder. The decoder enables the transmission gate of the sensor cell to the read line. The read lines are connected to a latched-based amplifier which produces the system output.

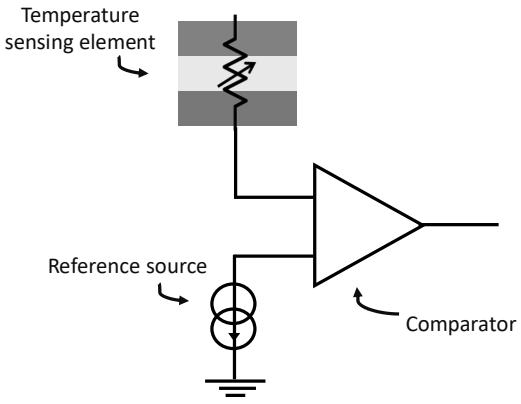


Fig. 3: On-chip analog thermal sensor

The proposed system includes a network of thermal sensor nodes distributed around an IC and additional circuitry, described in section II, that manages and controls the sensor signals and hence the system performance, as schematically shown in Figure 1. The paper is organized as follows. The proposed thermal aware system is described in section II, where the system architecture and circuit requirements are discussed. The use of an MTJ as a thermal sensor is discussed in section III. In addition, a comparison between a CMOS diode and transistor based thermal sensor with an MTJ/transistor temperature sensor is also provided in section III. Simulation results are presented in section IV followed by the conclusions in section V.

II. DISTRIBUTED THERMAL NETWORK

The proposed thermal aware system is a network of thermal sensor nodes communicating with a control unit that collects temperature data and produces a thermal map. This thermal network provides the monitored system with dynamic real-time thermal information. The proposed system architecture, read and data signaling, and related circuitry are discussed below. The system components are described in subsection II-A, the system signaling is illustrated in subsection II-B, and the fabrication characteristics of the system are reviewed in subsection II-C.

A. System architecture

The proposed system architecture, shown in Figure 2, is managed as a memory grid, where the sensor nodes are organized in a grid-based topology. To read a system of $m \times n$ sensor nodes with m columns and n rows, a $log_2\ n - to - n$ decoder and m amplifiers are required. The input to the system decoder identifies the row being read. Each row shares the same enable signal, while each column shares the same bit line. The enable signal, generated from the system decoder, passes the sensor node voltage to the bit line and is read through a sense amplifier. The proposed sense amplifier is latch-based, composed of two inverters controlled by a *Read* signal. The sensor node voltage is compared with a reference

voltage that sets a threshold temperature. The system output is in a binary format indicating whether the state of the sensor node is either below or above a threshold voltage.

B. System read and data signaling

The sequence of operations is as follows. During each read cycle, the enable signal controls the decoder to individually select one row. The output of each cycle is a vector of m sensor node reads. During each cycle, one row is read, and n cycles are required to read n rows. The system input is generated from a counter, and the system output is stored within a memory.

An example of the data signal waveform of a 4×4 data signal is shown in Figure 4. The decoder and sensor nodes are enabled by the Enable signal, where the decoder input data are annotated as $A0$ and $A1$. The output of the decoder enables the individual transmission gates. Each transmission gate connects the associated sensor node output to the bit line. The Read signal enables the sense amplifier to latch a bit line. In comparison with a reference voltage, the amplifier output is latched to either high or low. The output signals, $w0$, $w1$, $w2$, and $w3$, indicate the temperature status. By turning the Enable signal off, the system saves energy by isolating the power from the sensor nodes and decoder.

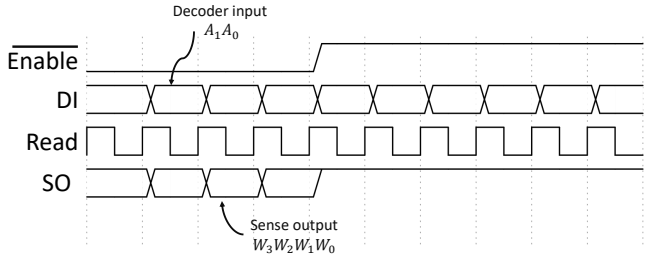
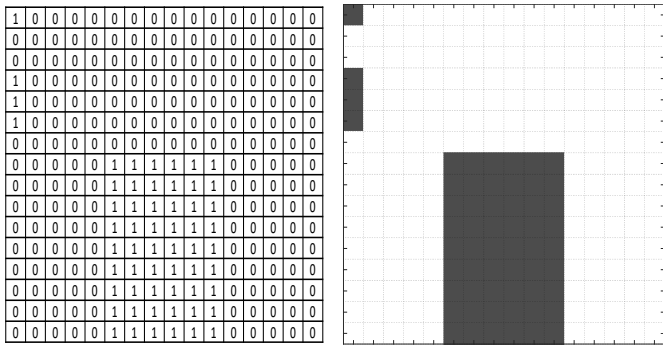


Fig. 4: System waveforms

The output of a distributed thermal network composed of 16×16 sensor nodes is illustrated in Figure 5b. The binary thermal map, shown in Figure 5a, reflects the location of the individual sensor nodes. The thermal map indicates if the temperature is above or below a predefined threshold temperature and hence determines in real-time the location of the critical hot spots.

C. System characteristics

The proposed system incorporates hybrid spintronic/CMOS devices. The spintronic circuit is based on a magnetic tunnel junction. An MTJ is a structure composed of two ferromagnetic layers separated by an insulator barrier [13]. The resistance of the device is controlled by the difference in the magnetization angle between the two layers. The device exhibits two stable states, a parallel (P) state (where the two layers are magnetized in the same direction) and an antiparallel (AP) state [14]. The MTJ is combined with CMOS to provide an efficient temperature sensing element. An MTJ/CMOS-based thermal sensor exhibits small size, low power, high linearity, and high sensitivity [15]. These capabilities support a thermal aware system composed of hundreds of distributed thermal sensor nodes.



(a) (b)

Fig. 5: 16×16 thermal map, (a) output sensor node readings, and (b) thermal map. The dark areas represent nodes with a temperature above the temperature threshold.

The MTJ is integrated between the metallic layers above the CMOS device layers, as shown in Figure 6, making this structure a good candidate for a local, distributed thermal sensor. MTJ fabrication is sufficiently mature for different technology platforms such as bulk-CMOS, FDSOI-CMOS, and FINFET CMOS [16]. Intel [17], GlobalFoundries [18], Samsung [19], and other large foundries are integrating MTJ technology with CMOS at different technology nodes. These advancements in fabrication can produce high quality MTJs for thermal sensing applications. In addition, MTJ memory can operate over a wide range of temperatures, -40^{o}C to 125^{o}C, in a stable manner for commercial, automotive, and military applications [20]. The ability of MTJ technology to be integrated with CMOS, operate over a wide, stable temperature range, and exhibit almost zero leakage current in the off state, with higher temperature sensitivity than conventional CMOS devices suggests an MTJ/CMOS temperature sensor is an effective candidate for next generation thermal aware systems [15].

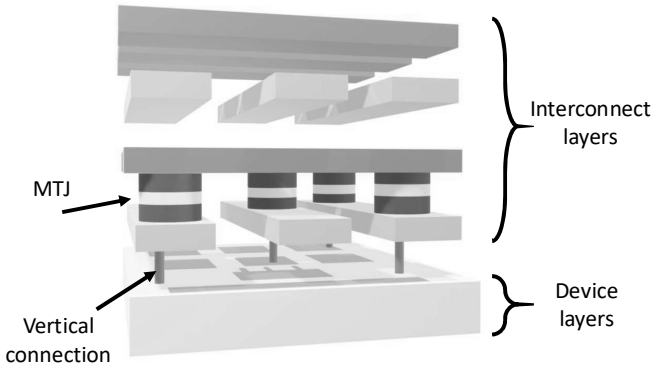


Fig. 6: MTJ, interconnect, and device layers

The use of an MTJ as a thermal sensor is supported by the high thermal sensitivity of the MTJ antiparallel resistance. The resistance of an MTJ changes almost linearly with high sensitivity with temperature in the antiparallel state (as compared to the parallel state) [21], [22], [23], [24]. The sensitivity of an MTJ to temperature is proposed in multiple MTJ structures such as, CoFeB/Al-O/CoFeB [21], [22], Fe/MgO/Fe [23], and CoFeB/MgO/CoFeB [24]. The thermal sensitivity of the

MTJ antiparallel resistance depends upon the device material structure, dimensions, and applied sense voltage.

The proposed temperature sensor cell is discussed in the following section. The physical, magnetic, and electrical behavior of an MTJ in addition to the proposed thermal sensor are reviewed. A comparison between the proposed temperature sensor and conventional CMOS sensors in terms of sensitivity, linearity, power consumption, and area is also provided.

III. INTEGRATED SOLUTIONS FOR THERMAL MONITORING

A variety of CMOS-based integrated electronic devices and circuits can produce a thermal response [25]. The most commonly used temperature sensor is the Brokaw bandgap circuit where a voltage or current produces a proportional-to-absolute temperature (PTAT) relationship [26], [27]. This circuit requires at least two large bipolar transistors to extract the PTAT signal. Other thermal sensors are based on a change in the threshold voltage of the diode or transistor with temperature [28]. This change in threshold voltage with temperature is exponential, requiring additional circuitry such as a threshold voltage extractor circuit [28] or look-up table [29] to accurately predict the temperature. Drawbacks of these technologies are high leakage currents, large device capacitance (which influences the circuit response), poor stability, and low sensitivity over a wide temperature range with thermal cycling [4]. The need for calibration prior to use and low sensitivity with device scaling are also common issues [4]. A spintronic device - the MTJ - is therefore suggested as a thermal sensing element for large scale distributed systems.

For an MTJ, the temperature influences the device magnetic anisotropy, antiparallel resistance, charge magnetic polarization, and thermal induced magnetic field [30]. The influence of both the sense voltage and temperature on an MTJ is discussed in subsection III-A. A comparison between four thermal sensors (a diode connected transistor, two paired transistors, a hybrid MTJ/transistor, and a hybrid MTJ/transistor with an active load) is described in subsection III-B.

A. MTJ as an integrated thermal sensor

A macrospin model, described in the Appendix, is used here. The model includes the influence of the sense voltage and temperature on the device tunneling magnetoresistance $TMR(T,V)$, layer spin polarization $P(T)$, saturation magnetization $M_S(T)$, device magnetic anisotropy constant $K(T)$, and voltage controlled magnetic ansitropy (VCMA) constant $\zeta_{VCMA}(T)$.

The influence of temperature on the conductance of an MTJ is the sum of two components, as described by (A.3); a spin dependent (elastic) term due to the thermal excitation of the spin polarized electrons, and a spin independent term (inelastic) due to scattering by defects and impurity states. The device antiparallel resistance decreases with increasing temperature. Under different sense voltages, the device exhibits a different sensitivity rate, as shown in Figure 7.

The sensing technique considers the effects of temperature and sense voltage on the thermal stability and resistance of an

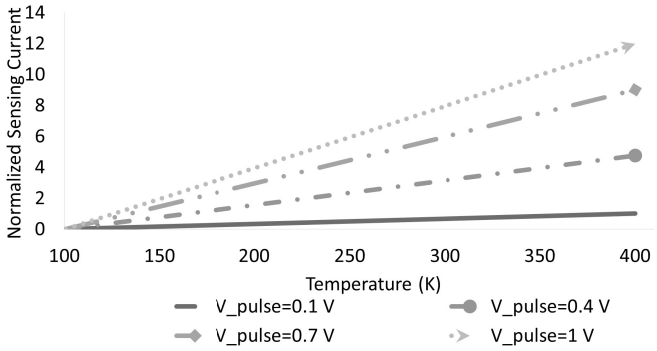


Fig. 7: Normalized sensing current of AP MTJ at different sense voltages [30]

MTJ. Hence, an MTJ operates in the stable AP state despite fluctuations in operating temperature and supply voltage. The thermal stability Δ of an MTJ determines the limits of the applied voltage and range of temperature over which the device can stably operate without switching [30]. Δ is the ratio of the magnetization energy of an MTJ and the thermal perturbation to the system, which is a function of temperature and applied voltage,

$$\Delta(T,V) = \frac{\Delta E(T,V)|_{MTJ}}{K_B T} = \frac{K_{eff}(T,V)v_{FM}}{K_B T}, \qquad (1)$$

where K_B is the Boltzmann constant, $\Delta E(T,V)|_{MTJ}$ is the system anisotropy energy of an MTJ, K_{eff} is the effective anisotropy constant, and v_{FM} is the volume of the FM layer. An MTJ with a high thermal stability factor is required for thermal sensing applications. An MTJ with a high thermal stability of 279 is achieved [31]

The proposed MTJ-based thermal sensor is illustrated in Figure 8, where a common source amplifier with a PMOS current source behaves as an active load. The active load bias and device size determine the circuit sensitivity. The increase in circuit sensitivity and linearity with temperature is compared in subsection III-B with CMOS-only thermal sensors.

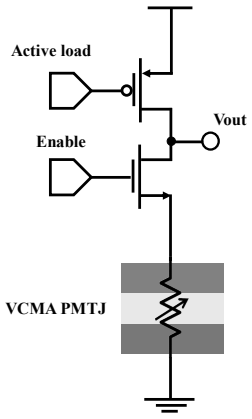
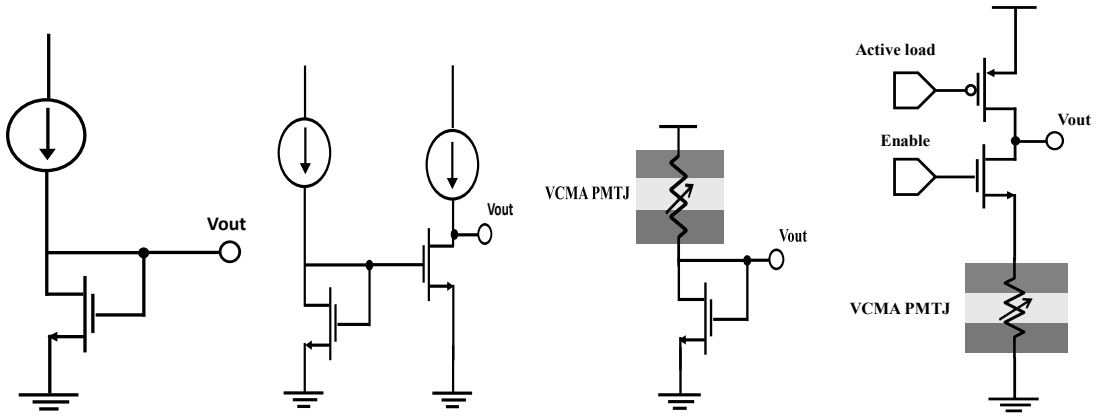


Fig. 8: Proposed MTJ/CMOS-based thermal sensor

B. Comparison with conventional integrated solutions

A hybrid MTJ/CMOS-based thermal sensor is proposed in this paper. The circuit considers the influence of temperature



(a) (b) (c) (d)

Fig. 9: Sensors, (a) diode connected transistor, (b) two paired transistors, (c) hybrid MTJ/transistor, and (d) hybrid MTJ/transistor with an active load

on both the threshold voltage of the transistor and the antiparallel resistance of the MTJ. A comparison between four different circuits clarifies the advantages of an MTJ combined with a CMOS device. The circuits are shown in Figure 9.

Circuits (a) and (b) are CMOS-only thermal sensors, where Circuit (a) is a diode connected transistor thermal sensor biased by a current source, and Circuit (b) is the same as Circuit (a) followed by a common source amplifier stage. In Circuit (b), the two transistors perform temperature sensing, which enhances the stability and linearity with temperature. Circuits (c) and (d) are MTJ/CMOS-based thermal sensors.

A comparison of these sensors is listed in Table 1. The simulation results are based on the MTJ macrospin compact model [30] of a VCMA PMTJ and the predictive transistor model (16 nm PTM) for CMOS transistors [32]. The CMOS transistors are sized the same (32 nm $\times$ 16 nm) and biased at the same current (31 nA) to establish a fair comparison.

The two CMOS-only thermal sensors, Circuits (a) and (b), exhibit good sensitivity with reasonable linearity. CMOS-only thermal sensors exhibit low linearity with temperature due to the exponential change in threshold voltage with respect to temperature. Incorporating an MTJ with CMOS increases the linearity of the thermal sensor, as listed in Table 1, where Circuits (c) and (d) exhibit higher linearity than CMOS-only thermal sensors. To increase the sensitivity of MTJ/CMOS-based thermal sensors, Circuit (d) is proposed where the active load voltage biases the circuit at the highest sensitivity and linearity. The sensitivity and linearity of the MTJ/CMOS thermal sensors outperform the CMOS-only thermal sensors due to the high linearity of the MTJ response to temperature.

In terms of power consumption, Circuit (d) exhibits the lowest power consumption since this sensor does not require additional current and uses the lowest on-current in comparison to the other sensors for the same supply voltage. The MTJ/CMOS-based thermal sensor is smaller since no current source is required.

As listed in Table 1, Circuit (d) exhibits the highest sensitivity and lowest power consumption. Circuit (d) is therefore considered as a system-wide temperature sensor in the proposed thermal aware system. In the following section, simulation results of the proposed system incorporating the hybrid MTJ/transistor thermal sensor node are presented. A comparison between the proposed thermal aware system in terms of energy consumption, delay, and system size is also described.

Table I: Comparison of the proposed temperature sensor and conventional CMOS sensors in terms of sensitivity, linearity, power consumption, and area

		Circuit (a)	Circuit (b)	Circuit (c)	Circuit (d)
Sensitivity (mV/K)	Commercial (0: 85)	0.51	0.51	0.4	1.91
	Industrial (-40:100)	1.03	1.03	0.64	3.78
	Automotive (-40:125)	1.08	1.08	0.77	3.97
	Military (-55:125)	1.35	1.35	0.81	4.8
Linearity	Commercial (0: 85)	0.985	0.985	1	0.983
	Industrial (-40:100)	0.953	0.953	0.999	0.96
	Automotive (-40:125)	0.941	0.941	0.999	0.947
	Military (-55:125)	0.919	0.919	0.996	0.936
Power Consumption@RT 27^{o}C(μW)		40	80	18	11.9
Area (μm^2)		4X	8X	1X	2X

IV. Simulation Results

The system operation works as follows. The sense amplifier sets the sensor node voltage. Based on the grid size and number of nodes, preamplifier stages or buffers increase the current, enhance the sensitivity, and isolate the sensor node signal. The signal path of the sensor node to the output, shown in Figure 10, is used to characterize system performance. The system characteristics are listed in Table II, where the power consumption includes the energy consumed in the sensor nodes, buffers, inverters, amplifiers, and decoder. The delay of the read operation is the time required to read each of the rows.

A read pulse of 1 ns is used to produce an output decision of one sensor node. The comparator delay is 0.03 ns. The accuracy of the system temperature is $\pm$3 K for a reference voltage with an accuracy of $\pm$1 mv. The area of each sensor node is 32 nm $\times$ 64 nm where the MTJ layer is between the second and third interconnect layer, as shown in Figure 6. The average sense current of a thermal sensor node is 11 μA. The sensor nodes need to be calibrated prior to use due to

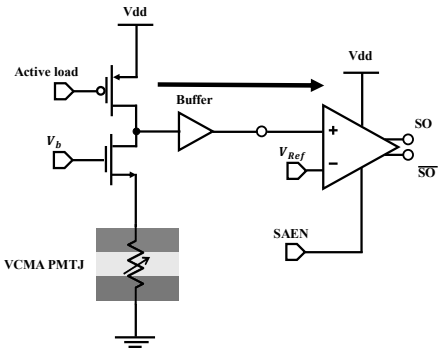


Fig. 10: Sensor signal path

the influence of manufacturing process variations. Different calibration schemes of multiple on-chip thermal sensors have been proposed [4]. The design, management, and control of these thermal sensors are the foci of this paper. The ability to fabricate an MTJ with a different antiparallel resistance (thermal sensitivity) has been achieved [23], and additional research is required to enhance the sensitivity of an MTJ to thermal and process variations.

Table II: Characteristics of the proposed distributed thermal network for different grid sizes

System size	Energy consumption (pJ)	Relative path delay to read the grid w.r.t. 4 × 4	System size #	
			Transistors	MTJs
4 × 4	1.32	1x	90	16
8 × 8	8.96	2x	304	64
16 × 16	65.50	4x	1,120	256
32 × 32	499	8x	4,980	1024

An example of the system output at three different reference voltages, 300 mV, 304 mV, and 306 mV, mapped to, respectively, threshold temperatures of 332 K, 343 K, and 350 K is shown in Figure 11. A multiplexer can be added to switch the reference signal between different voltages to vary the threshold temperature of the sensor nodes.

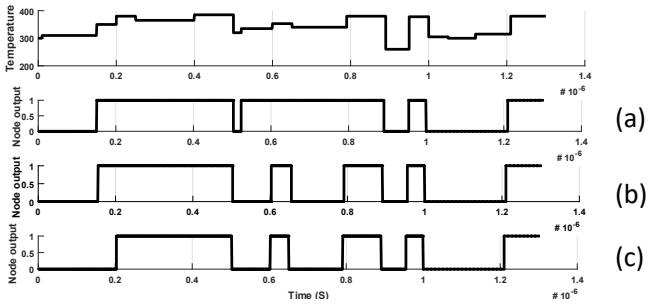


Fig. 11: System output, (a) V_{ref} = 300 mV which maps to a threshold temperature of T = 332 K, (b) V_{ref} = 304 mV and T= 343 K, and (c) V_{ref}= 306 mV and T = 350 K

A comparison between the proposed hybrid CMOS/MTJ thermal sensor and [12] in terms of system requirements, sensing scheme, energy, read accuracy, and temperature range is listed in Table III. The primary purpose of this paper is to describe a hybrid MTJ/CMOS-based thermal sensor and a related thermal aware system. A distributed thermal sensor network able to provide an updated spacial and temporal thermal map in real-time is also described in this paper.

Table III: Comparison between the proposed CMOS/MTJ thermal sensor and [12]

	Proposed thermal aware system	[12]
Sensing Scheme	Change in AP resistance to temperature	Change in probability of switching
Sensor node	One MTJ, two transistors, V_{dd}	Two MTJs, two transistors, V_{dd}, I_{bias}
System Requirement	Latch-based amplifier	Circuit to map probability of switching an MTJ to temperature
Energy	0.5 nJ (To read network of 32 × 32 cells)	8.5 nJ
Accuracy	3 K	1 K
Output	1 or 0 indicating above or below threshold temperature	Local temperature

The proposed system provides flexibility in choosing a threshold temperature. The system can also support a multi-threshold sensing scheme. This capability can be achieved by multiplexing the reference voltage. At each reference voltage, the system identifies whether the temperature at a sensor node is above or below a certain threshold temperature. As an example, with two different reference voltages, the system could identify the temperature at a sensor node within three different temperature regions (below T1, between T1 and T2, or above T2).

With hundreds of on-chip thermal sensor nodes distributed across a system, the ability to monitor local heat (characterizing the generated heat and thermal paths) is achieved. This capability for real-time spacial and temporal sensing provides significant information characterizing the thermal behavior which can be used to mitigate on-chip heat generation and distribution issues.

V. CONCLUSIONS

The need for a thermal aware system increases with device scaling and the size of the integrated system. A thermal aware system is proposed where a grid structure is composed of individual thermal sensor cells. The sensor nodes are based on hybrid spintronic/CMOS technology, where the antiparallel resistance of a magnetic tunnel junction exhibits a thermal linearity of 0.9 and thermal sensitivity of 4.8 mv/K over a temperature range of -55 ^{o}C to 125 ^{o}C. A system of 1,045 thermal sensors distributed in a 32 × 32 grid structure consumes approximately 500 pJ. This low energy and high sensitivity are appropriate for next generation thermal aware systems.

APPENDIX

MTJ macrospin model

A macrospin compact model which characterizes a voltage controlled magnetic anisotropy (VCMA) MgO—CoFeB perpendicular MTJ is described here [30]. The model considers the dynamic response of the device magnetic and electrical performance. The magnetization dynamics of the free ferromagnetic (FM) layer are described by the modified

Landau-Lifshitz-Gilbert equation. The expression describes the dynamic magnetic behavior of the FM layer as

$$\frac{\partial \vec{M}}{\partial t} = -\frac{\gamma \mu_o}{1+\alpha^2}[\vec{M} \times \vec{H}_{eff} + \alpha\ \vec{M} \times \frac{\partial \vec{M}}{\partial t}] + \gamma \sum \vec{\tau}_i, \quad \text{(A.1)}$$

where $\vec{M}$ is the normalized free layer magnetization, t is the time variable, $\vec{H_{eff}}$ is the effective magnetic field expressed in A/m, γ is the electron gyromagnetic ratio, $\gamma \approx -2\pi \times 27.99$ GHz/T, μ_o is the permeability of free space, α is the Gilbert damping factor, and $\vec{\tau}_i$ is the applied torque due to other perturbations such as current which exerts a spin transfer torque [33].

The macrospin model is developed in association with the static and dynamic micromagnetic analysis of the system energy. The applied effective magnetic field to the free layer $\vec{H_{eff}}$ is

$$\vec{H}_{eff} = \vec{H}_{UA} - \vec{H}_{dem} + \vec{H}_c + \vec{H}_{ext} - \vec{H}_{VCMA} + \vec{H}_{th}, \quad \text{(A.2)}$$

where $\vec{H_{UA}}$ is the uniaxial anisotropy field sometimes defined as $\vec{H_K}$, $\vec{H_{dem}}$ is the demagnetization field, $\vec{H_c}$ is the coupling field due to the other FM layer, $\vec{H_{ext}}$ is the applied external magnetic field, $\vec{H_{VCMA}}$ is due to VCMA, and $\vec{H_{th}}$ is the stochastic magnetic field due to thermal variations.

The MTJ antiparallel conductance is modeled as [34]

$$G_{AP}(T) = G_T\,[1 - P_1(T)P_2(T)\ ] + G_{SI}, \quad \text{(A.3)}$$

where $G_T = G_0\ (\sin(CT)/CT)$ is the thermal smearing factor, $G_0 = \left(3.16 \times 10^{10}\sqrt{\phi_B}/t_{ox}\right) exp(-1.025 \times \sqrt{\phi_B} \times t_{ox})$ is the parallel state conductance at zero voltage and zero temperature, T is the ambient temperature, ϕ_B is the average tunneling barrier height (in eV), t_{ox} is the thickness of the insulator barrier layer, and $C = 1.387 \times 10^{-4} t_{ox}/\sqrt{\phi_B}$ is a material dependent parameter [34]. $G_{SI} = ST^{4/3}$ is the inelastic spin independent conductance, and S is a fitting parameter. P_1 and P_2 are the spin polarization percentage of the two FM layers. The dependence of the spin polarization on temperature can be fitted as [35], [21]

$$P(T) = P(0)\,[1 - \beta_P T^{\alpha_P}\ ], \quad \text{(A.4)}$$

where β_P and α_P are fitting parameters related to the device dimensions and material properties.

The physical parameters are based on perpendicular magnetic anisotropy and VCMA MgO—CoFeB [30], [36], [37]. The experimentally extracted model parameters are listed in Table A.1.

Table A.1: MTJ physical parameters

Parameters	Description	Value
w_{FL}	FM width = radius	20 nm
t_{FL}	FM thickness	1.5 nm
t_{ox}	Barrier thickness	1.1 nm
Φ_{BL}	Barrier height	0.39 eV
V_h	Voltage @ half TMR	0.5 V
S	Spin independent conductance factor	1.1×10^{-12}
β_P	Fitting parameter for P	2.07×10^{-5}
α_P	Fitting parameter for P	2.3
β_M	Fitting parameter for M_S	1.5
T^*	Fitting parameter	1120 K
β_{Ki}	Fitting parameter	2.3
$\beta_{\zeta VCMA}$	Fitting parameter	2.83
N_z	Demagnetization tensor factor in Z	0.9343
N_{xy}	Demagnetization tensor factor in XY	0.015
K_{i0}	Interfacial MA at 0 K	$2.02 \times 10^{-3} J/m^2$
M_{S0}	Saturation magnetization at 0 K	$1457 \times 10^3 A/m$
TMR_0	TMR at 0 K	3
ξ_{VCMA0}	VCMA factor at 0 K	48.9×10^{-15} J/(V.m)

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