Robust Control of Solid State Transformer using Dynamic Phasor based model with *dq* transformation

M. Monika*, R. Meshram, S. Wagh, N. M. Singh and A.M. Stanković

***Abstract*—A high frequency solid-state transformer (SST) proposed by FREEDM centre is an interesting alternative to conventional distribution transformer in microgrids as it supports additional functionalities such as active-reactive power flow control, fault current limitation and voltage regulation. This paper proposes a dynamic phasor based robust control of SST through the modular control of each stage. The control problem is formulated in frequency domain by representing the system states with time varying Fourier coefficients or dynamic phasors (DP). This formulation transforms the oscillating waveforms of ac circuits to constant or slowly varying variables, hence allow the use of PI controller to track the sinusoidal references. For rectifier and inverter stages of SST, *dq* transformation is applied on DP which facilitates the design of PI controller to smoothen out the ripples in the output voltage waveform. The controller gains are tuned to reject input and load disturbances and attenuate measurement noise using loop shaping and pole assignment technique. The robustness of the controller is assured analytically against parametric uncertainties using small gain theorem. Simulation results are provided to support the proposed control scheme. Hardware-in-Loop (HIL) simulation is carried out on critical stages using Opal-RT and dSPACE simulators to confirm the effectiveness of the proposed scheme.**

***Index Terms*—Dynamic phasors (DP), *d-q* transformation, Hardware-in-Loop (HIL), robust control, small gain theorem, solid state transformer (SST)**

I. Introduction

The conventional grid augmented with the microgrid has numerous advantages. During the peak load demands, the excess capacity requirement of conventional grid is supported by microgrid that supplies power, and during power outages or grid failures microgrid isolates its generation nodes and power loads from the disturbance. Microgrid offers close proximity between power generation and load, so that the varying load may affect the performance of the microgrid. In addition, microgrid may suffer from power quality problems such as voltage sag/swell, harmonics and flickers because of the intermittent nature of the renewable sources and the use of power electronic converters. The issues of varying loads and intermittent renewable sources can be mitigated by replacing the distribution transformer with the SST proposed by Future Renewable Electric Energy Delivery and Management (FREEDM) systems center [1]. The SST provides additional functionalities such as bidirectional power flow, power quality and fault current limitation over traditional transformer [2]. In addition, with proper controllers, it maintains required voltage profile for any input source voltage variation or for given load variations. There exist numerous proposed topologies for SST. In [3], a comparison of various representative SST topologies reveal that the three-stage, dual active bridge (DAB) based topology, a schematic of which is given in [4], provides all the desired SST functionalities which are required to replace a distribution transformer in a microgrid. To understand the impact of unreliable input source characteristics of renewable sources and effect of load variations in weak micro-grid, a dynamic model of various stages and components of SST is essential. The switched models are not suitable for most types of control problems because of the excessive computational effort and the lack of focus on control quantities.

The average model of SST along with its control strategy is developed and analyzed for voltage sag, regenerative mode and load change in [5]. However, the standard average model is unable to describe the switching ripple which is usually present in the state variable of power converters. This restricts the use of the average model in designing the switching ripple based control scheme as explained in [6]. In addition to this, the standard state space averaging does not find application in a wide range of power circuits whose states have predominantly oscillatory behavior.

The generalized averaging method proposed in [7], also called dynamic phasor (DP) approach, is used to model the converters with ac stages. In this method, the circuit waveform, x(t) is demodulated to its components over the interval $[t-T, t]$ with Fourier series representation [8]. The DP model, though approximate, provides time-invariant models for multi-scale nature of hybrid systems. A complete DP model of 3-stage SST is developed in [4].

Different control strategies are adopted by various authors for design of controllers for SST-related converters. In [8], the dynamic phasor-based PI control is proposed for the full bridge single phase inverter and detailed comparative analysis with the average model is discussed, whereas [12] investigates the limitations of PI controller and proposes two methods, PI plus feed-forward control and PI plus resonant control, to improve the regulation of the output voltage of DAB converter driving single phase inverter. In [4], combined control of 3-stage SST is achieved through modular control which is implemented using PI controllers with direct voltage control strategy whereas in [11], the voltage regulation issue is addressed through internal model control (IMC) technique.

This paper addresses the voltage regulation issue of 3-stage SST using robust PI controller. The combined control is achieved by adopting modular control at each stage. The main contributions of this research are:

1) The research exploited the advantages of the *dq* transformation on DP for the improved controller design as

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compared to its time domain counterpart.

2) Although, the loop shaping and pole assignment techniques are commonly used for tuning of PI controller gains, first time it has been adopted for DP-*dq* model of SST to have effective response for rejection of load disturbances, attenuation of measurement noise and robustness, which are some of the major issues in microgrid.
3) Irrespective of ample literature available on small gain theorem, the proposed research provides a novelty in application of small gain theorem to demonstrate the robustness of the DP-*dq* based PI controllers of SST against parametric uncertainties which is one of the key concerns for microgrid architecture.
4) For experimental results, the paper proposes HIL simulation in which Opal-RT acts as the plant and dSPACE as controller generating real time control inputs for the plant.

The paper is organized as follows: Section II discusses the need of DP based model for SST and its advantages over the average model, it also elaborates the need of *dq* transformation for the converters with ac stages and the linearized model for small signal stability analysis. In Section III, the control scheme for the voltage regulation of the 3-stage SST is proposed and the detail design of the controller for each stage of SST is explained. In addition, the robustness of the controller against parametric variation is assured using small gain theorem for tuning of controller gains. In Section IV, the control approach is evaluated using the simulation results of the 3-stage SST for the voltage sag, parametric and load variation along with attenuation of measurement noise. Also the proposed control scheme and results are verified through HIL implementation. Finally, Section V summarises the contribution of this work.

II. Model Development of SST

The SST under consideration converts single phase 7.2KV, 50Hz ac voltage to 230V, 50 Hz, single phase ac with DAB being the intermediate stage[13]. The dc/dc DAB converter changes 3.8KV dc voltage to 400V DC. The real power transfer is from leading phase angle bridge to the lagging phase angle bridge [14]. The actual topology of the rectifier comprises of three cascaded rectifier which are connected to three high voltage high frequency dc/dc converters. The output of each DAB is connected in parallel. In this section, a dynamic phasor based model with *dq* transformation is developed for the combined SST. The DP-*dq* based model is developed using the modular cascade dynamic phasor model of 3-stage SST as derived in [4]. The general expressions for the modular cascade DP model of 3-stage SST are expressed by (1)-(3). In this model, the state variables and switching functions are the dynamic phasors. The DP based model allows the use of PI controller instead of proportional-resonant controller [15] even for the tracking of sinusoidal references.

$$\dot{x}_{SST} = f(x_{SST}, S_{SST}) \tag{1}$$

$$[x_{SST}] = \begin{bmatrix} x_{rect} & x_{DAB} & x_{inv} \end{bmatrix}^T \tag{2}$$

$$[S_{SST}] = \begin{bmatrix} S_{rect} & S_{D1} & S_{D2} & S_{inv} \end{bmatrix}^T \tag{3}$$

The following subsection explicates the need of *dq* transformation and the development of the small signal model.

A. Necessity of dq transformation

To improve the response and to smoothen out the small ripples in the output voltage waveform, *dq* transformation is used for the stages which have ac and dc interactions. The additional feature of the *dq* modeling is, the control of active and reactive power components as they are functions of the components of voltage and current. Synchronization with the ac grid using phase-locked-loop (PLL), the GAM based *dq* modeling performs an amplitude demodulation that transforms the ac variables into dc variables [16].

In ABC to DQ0 frame transformation the second harmonic appears in the *d* and *q* axes under unbalanced conditions which slows down the simulation process considerably [17]. However, in DP-*dq* transformation the variables are always dc-like under both balanced and unbalanced conditions. The selection of *dq* frame allows to conveniently express the *d* and *q* components of voltage and current vectors in DPs. The *dq* model for rectifier is derived from its dynamic phasor model as given in [4]. The general relation between the *dq* variables and the dynamic phasors is given as:

$$\langle x \rangle_1^R = \frac{x_q}{2}, \qquad \langle x \rangle_1^I = -\frac{x_d}{2} \tag{4}$$

Using the transformation of (4) on the generalised dynamic phasor model of rectifier and inverter developed in [4] and [11], the DP-*dq* model is obtained as:

$$\frac{\mathrm{d}i_{gd}}{\mathrm{d}t} = \omega i_{gq} + \frac{1}{L_g}\left[v_{gd} - v_{cfrd} - R_g i_{gd}\right] \tag{5}$$

$$\frac{\mathrm{d}i_{gq}}{\mathrm{d}t} = -\omega i_{gd} + \frac{1}{L_g}\left[v_{gq} - v_{cfrq} - R_g i_{gq}\right] \tag{6}$$

$$\frac{\mathrm{d}i_{frd}}{\mathrm{d}t} = \omega i_{frq} + \frac{1}{L_{fr}}\left[v_{cfrd} - S_{rd}V_{dcH} - R_{fr} i_{frd}\right] \tag{7}$$

$$\frac{\mathrm{d}i_{frq}}{\mathrm{d}t} = -\omega i_{frd} + \frac{1}{L_{fr}}\left[v_{cfrq} - S_{rq}V_{dcH} - R_{fr} i_{frq}\right] \tag{8}$$

$$\frac{\mathrm{d}v_{cfrd}}{\mathrm{d}t} = \omega v_{cfrq} + \frac{1}{C_{fr}}\left[i_{gd} - i_{frd}\right] \tag{9}$$

$$\frac{\mathrm{d}v_{cfrq}}{\mathrm{d}t} = -\omega v_{cfrd} + \frac{1}{C_{fr}}\left[i_{gq} - i_{frq}\right] \tag{10}$$

$$\frac{\mathrm{d}V_{dcH}}{\mathrm{d}t} = \frac{1}{C_{dcH}}\left[\frac{1}{2}\left\{S_{rq}i_{frq} + S_{rd}i_{frd}\right\} - \frac{V_{dcH}}{R_L}\right] \tag{11}$$

$$\frac{\mathrm{d}i_{fid}}{\mathrm{d}t} = \omega i_{fiq} + \frac{\left[S_{id}V_{dcL0} - v_{cfid} - R_{fi} i_{fid}\right]}{L_{fi}} \tag{12}$$

$$\frac{\mathrm{d}i_{fiq}}{\mathrm{d}t} = -\omega i_{fid} + \frac{\left[S_{iq}V_{dcL0} - v_{cfiq} - R_{fi} i_{fiq}\right]}{L_{fi}} \tag{13}$$

$$\frac{\mathrm{d}v_{cfid}}{\mathrm{d}t} = \omega v_{cfiq} + \frac{1}{C_{fi}}\left[i_{fid} - \frac{v_{cfid}}{R_L}\right] \tag{14}$$

$$\frac{\mathrm{d}v_{cfiq}}{\mathrm{d}t} = -\omega v_{cfid} + \frac{1}{C_{fi}}\left[i_{fiq} - \frac{v_{cfiq}}{R_L}\right] \tag{15}$$

B. Small Signal Model

The small signal model concept explained in [18] represents the deviations in the state variables from their initial value X because of small perturbation in control signal, d i.e. duty cycle from its initial value D. The small signal DP based model of SST developed in [4] forms the basis for the DP-*dq* based model for rectifier and inverter and it is expressed by (16) and (17) respectively.

$$\begin{bmatrix}\Delta\dot{i}_{gd}\\ \Delta\dot{i}_{gq}\\ \Delta\dot{i}_{frd}\\ \Delta\dot{i}_{frq}\\ \Delta\dot{v}_{cfrd}\\ \Delta\dot{v}_{cfrq}\\ \Delta\dot{v}_{dcH0}\end{bmatrix}=\begin{bmatrix}-\frac{R_g}{L_g} & \omega & 0 & 0 & -\frac{1}{L_g} & 0 & 0\\ -\omega & -\frac{R_g}{L_g} & 0 & 0 & 0 & -\frac{1}{L_g} & 0\\ 0 & 0 & -\frac{R_{fr}}{L_{fr}} & \omega & \frac{1}{L_{fr}} & 0 & \frac{4cos(\pi D_r)}{\pi L_{fr}}\\ 0 & 0 & -\omega & -\frac{R_{fr}}{L_{fr}} & 0 & \frac{1}{L_{fr}} & \frac{4sin(\pi D_r)}{\pi L_{fr}}\\ \frac{1}{C_{fr}} & 0 & -\frac{1}{C_{fr}} & 0 & 0 & \omega & 0\\ 0 & \frac{1}{C_{fr}} & 0 & -\frac{1}{C_{fr}} & -\omega & 0 & 0\\ 0 & 0 & \frac{2cos(\pi D_r)}{\pi C_{dcH}} & -\frac{2sin(\pi D_r)}{\pi C_{dcH}} & 0 & 0 & -\frac{1}{R_L C_{dcH}}\end{bmatrix}\begin{bmatrix}\Delta i_{gd}\\ \Delta i_{gq}\\ \Delta i_{frd}\\ \Delta i_{frq}\\ \Delta v_{cfrd}\\ \Delta v_{cfrq}\\ \Delta v_{dcH0}\end{bmatrix}+\begin{bmatrix}0\\ 0\\ \frac{4V_{dcH0}sin(\pi D_r)}{L_{fr}}\\ \frac{4V_{dcH0}cos(\pi D_r)}{L_{fr}}\\ 0\\ 0\\ -\frac{2\left[I_{frq}cos(\pi D_r)+I_{frd}sin(\pi D_r)\right]}{C_{dcH}}\end{bmatrix}[\Delta d_r] \quad (16)$$

$$\begin{bmatrix}\Delta\dot{i}_{fid}\\ \Delta\dot{i}_{fiq}\\ \Delta\dot{v}_{cfid}\\ \Delta\dot{v}_{cfiq}\end{bmatrix}=\begin{bmatrix}-\frac{R_{fi}}{L_{fi}} & \omega & \frac{-1}{L_{fi}} & 0\\ -\omega & -\frac{R_{fi}}{L_{fi}} & 0 & \frac{-1}{L_{fi}}\\ \frac{1}{C_{fi}} & 0 & \frac{-1}{R_L C_{fi}} & \omega\\ 0 & \frac{1}{C_{fi}} & -\omega & \frac{-1}{R_L C_{fi}}\end{bmatrix}\begin{bmatrix}\Delta i_{fid}\\ \Delta i_{fiq}\\ \Delta v_{cfid}\\ \Delta v_{cfiq}\end{bmatrix}+\begin{bmatrix}\frac{4sin(2\pi D_i)V_{dcL0}}{L_{fi}}\\ \frac{4cos(2\pi D_i)V_{dcL0}}{L_{fi}}\\ 0\\ 0\end{bmatrix}[\Delta d_i] \quad (17)$$

III. Control Design Strategies

A. General PI control

This research employs robust PI controllers that are tuned using the DP-*dq* based small signal models of converters. In this paper, the PI controller design for the proposed scheme is based on pole assignment and loop shaping technique [19]. Three major factors i.e. reduction of load disturbances, measurement noise and robustness in addition to voltage regulation are being addressed while designing the controller.

In this technique, the controller design is based on the desired shape of Bode plot of the loop transfer function. The system's robustness is defined using stability, gain and phase margins, which imposes limits on the loop transfer function near the crossover frequencies ω_{gc} and ω_{pc}. To have good tracking of signals and attenuation of load disturbances, a large gain of L is required at low frequencies whereas attenuation of measurement noise is achieved by keeping the gain of the loop transfer function low at high frequencies.

In proposed control scheme shown in fig. 1, the combined

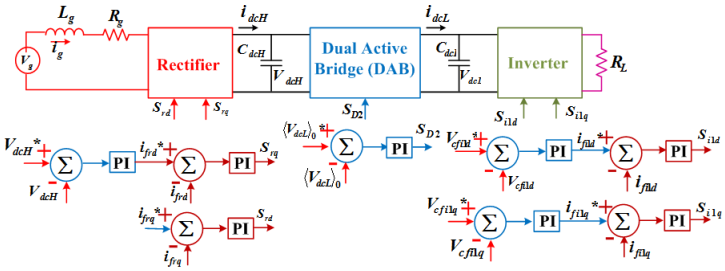


Fig. 1: Control Scheme of 3-Stage SST

control of 3-Stage SST is obtained by implementing the modular control for each stage of SST. The DP-*dq* based model of SST is used for the controller design. The complete control is a combination of two PI control strategies i.e. direct voltage control at DAB stage and nested loop control for rectifier and inverter stage. The detailed control design is explained in the following subsections.

B. Rectifier and Inverter Control Scheme

The design of the inner current controller and outer voltage controller is based on the DP-*dq* based small signal model of the rectifier and inverter as given in (16) and (17). For rectifier, the outer voltage loop tracks the dc output voltage and generates a reference for the *d*-axis current, the reference for the *q*-axis current is set as zero whereas for inverter the direct and quadrature references for the outer voltage loop are generated by using phase-locked-loop (PLL)-based synchronization with the desired ac voltage. The outer voltage loop generate the references for the inner current loops. A prefilter is used to reject the variations and the ripple in the voltage.

The flow chart as shown in Fig. 2 represents the methodology adopted for tuning of the controller gains for rectifier and inverter. The complete design process is divided in three stages.

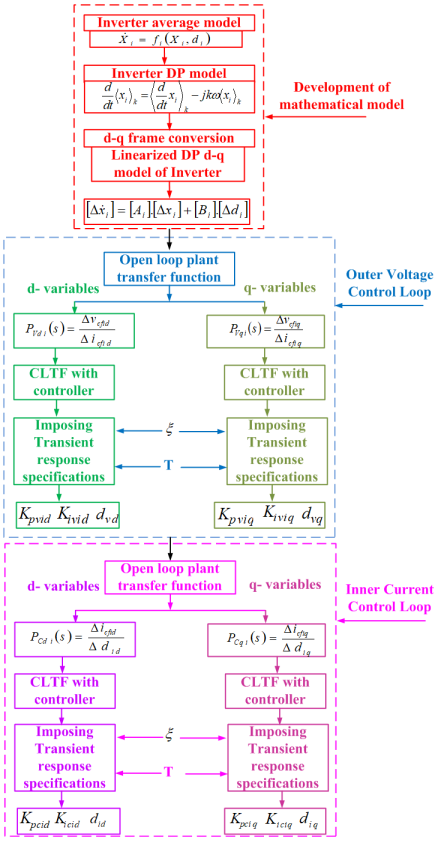


Fig. 2: Flow chart for inverter controller design

In stage one, the linearized small signal DP-*dq* model of

converter is developed. Stage two involves the evaluation of the outer loop voltage controller gains based on the desired design specifications. In this stage, the *d* and *q* axis current references are generated. In stage three, the inner current controller gains are evaluated for tracking the *d* and *q* axis current references generated by outer voltage loop.

Using the small signal model of rectifier and inverter, the generalised expressions for voltage and current controller gains are obtained as:

$$K_{PV} = \frac{T_{iV}T_V}{K_V T_{OV}^2}, \quad T_{iV} = 2\zeta_V T_{OV} - \frac{T_{OV}^2}{T_V} \tag{18}$$

$$K_{PC} = \frac{T_{iC}T_C}{K_C T_{OC}^2}, \quad T_{iC} = 2\zeta_C T_{OC} - \frac{T_{OC}^2}{T_C} \tag{19}$$

where $\frac{1}{T_{OV}}$ and $\frac{1}{T_{OC}}$ are the desired bandwidth, ζ_V and ζ_C are the desired damping coefficient. For rectifier, $K_V = \frac{R_L \times D_r^*}{2}$ and $T_V = R_L \times C_{dcH}$ and $K_C = \frac{V_{dcH}^*}{R_{fr}}$ and $T_C = \frac{L_{fr}}{R_{fr}}$ and for inverter the values are: $K_V = R_L$, $T_V = R_L \times C_{fi}$, $K_C = \frac{1}{R_{fi}}$ and $T_C = \frac{L_{fi}}{R_{fi}}$.

C. DAB Control Scheme

The proposed direct voltage control scheme for DAB is implemented with a single voltage control loop to track the output voltage. The algorithm for evaluating controller gains is given as:

1) Obtain the linearized DP model of DAB around the selected equilibrium point.
2) Deduce the transfer function from the secondary bridge duty ratio to DC voltage. The duty ratio of the primary bridge is kept constant.
3) Introduce the compensation for the computational delay.
4) For the desired phase margin, evaluate the crossover frequency.
5) For the desired performance specification evaluate the controller gains.

Based on the algorithm, for maximum integrator gain and desired phase contribution [20], the proportional gain and the integral time constant are obtained using the DP based small signal model of DAB developed in [4] :

$$K_{PV} = \frac{\omega_c}{K_V}, \quad T_{iV} = \frac{10}{\omega_c} \tag{20}$$

D. Robust Control

The design of robust controller is based on addressing the voltage regulation issue under parametric uncertainties [21]. The robustness of the controller is ascertained using small gain theorem as explained in [21] and [22]. To ensure the robustness of the controller, the small gain theorem is implemented using the following algorithm:

1) Obtain the magnitude plots for the multiplicative uncertainty, for $\pm 25\%$ perturbations in the nominal value of parameters (i.e. inductance, capacitance and resistance).
2) Define a weighing function $W_m(s)$ such that its magnitude plot is positioned above all the plots of multiplicative uncertainties. This establishes the upper bound for parametric uncertainty.
3) Obtain the magnitude plot of the inverse of multiplicative weighing function and of complimentary sensitivity function.
4) The robustness of the controller is assured if the plot of complimentary sensitivity function is positioned below the plot of the inverse of multiplicative weighing function.

IV. Performance Evaluation

Using the simulation parameters specified in Table 1, a 3-stage SST model is developed in MATLAB/Simulink, and the effectiveness of controller is validated in three different operating scenarios.

1) Input voltage variation indicative of the voltage sag/swell of the microgrid.
2) Unity power factor (resistive) load change.
3) Robustness against model uncertainties.
4) Effect of measurement noise

TABLE I: Simulation Parameters

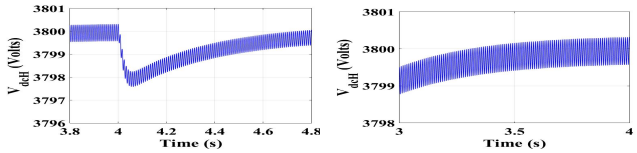
Parameter	Specification
Grid side line resistance (R_g)	37 ohms
Grid side line inductance (L_g)	121 mH
Rectifier filter resistance (R_{fr})	11 ohms
Rectifier filter inductance (L_{fr})	170 mH
Rectifier filter Capacitance (C_{fr})	0.04 μF
HVDC link capacitor (C_{dcH})	42 μF
Grid side rectifier voltage (V_g)	7200 V(rms)
HVDC link capacitor voltage (V_{dcH})	3800 V
Transformer resistance (R_t)	0.4 ohms
Transformer inductance (L_t)	250μH
LVDC link capacitor (C_{dcL})	540 μF
LVDC link capacitor voltage (V_{dcL})	400V
Inverter filter resistance (R_{fi1})	0.07ohms
Inverter filter inductance (L_{fi1})	1.07 mH
Inverter filter capacitance (C_{fi1})	30 μF
Inverter filter capacitor voltage (V_{fi1})	230V (rms)
Load resistance in inverter circuit (R_{L1})	35 ohms

A. Input Voltage Variation

In this section, the performance of the controller is observed for step change in the input voltage. Fig.3, 4 and 5 (a) show the controlled response of each stage along with the corresponding change in the duty ratio, for 10% decrease in the input voltage. The step change is introduced at $t = 4sec$. It is observed that the output voltage is regulated at modular stages and when combined cascade model is considered, the effect of the input voltage variation on the inverter is negligible as the previous stages (i.e. rectifier and DAB) regulate and maintain constant dc voltage input to the inverter. With the DP-*dq* control, the output voltage ripple is approximately 1V (peak to peak) which is considerably small. In addition to the reduction in ripple content, the advantage of DP-*dq* model over average-*dq* model is the simple algebraic transformation between the DP and *dq* variables as compared to complicated calculation of angle θ required for average to *dq* variable transformation.

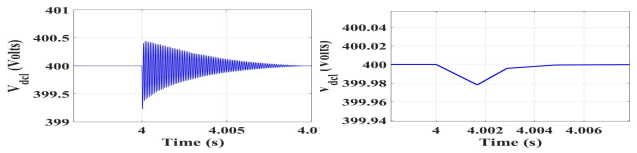
B. Load variations

Fig.3, 4 and 5 (b) show the response of the individual stages of the SST under load change. At each stage the output



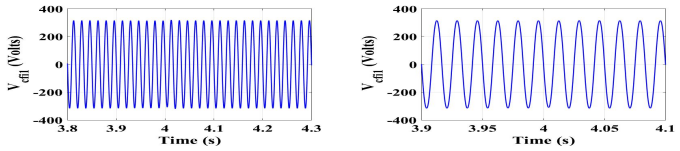
(a) (b)

Fig. 3: Output voltage of rectifier stage for (a) input voltage variations (b) load change



(a) (b)

Fig. 4: Output voltage of DAB stage for (a) input voltage variations (b) load change



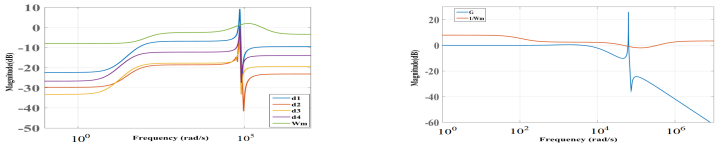
(a) (b)

Fig. 5: Output voltage of inverter stage for (a) input voltage variations (b) load change

voltage is maintained constant for 10% step change in the load resistance, with the corresponding change in duty ratio. At the onset of the load transient, the duty cycle changes near-instantly to regulate the output voltage of the inverter and stabilises when the load current reaches to its steady state. The cascade effect on DAB and rectifier is negligible. The output voltage and the current of both the converters is maintained at the desired value.

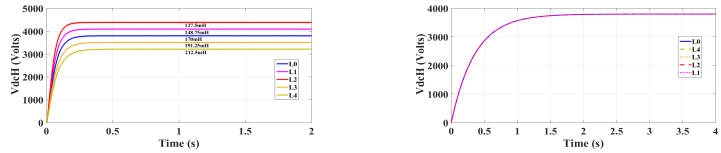
C. Robustness

The robustness of the controller for the combined model is observed for the perturbations in the operating point. The small-gain theorem has been used as a tool for robustness analysis. To ascertain the robustness of the controllers, the resistance, inductance and capacitance parameter nominal values are perturbed by $\pm 25\%$ The bode plots of uncertainty functions and bounds shown in Fig.6 indicate the robustness of the controllers analytically. For robust control, the magnitude plot of complimentary sensitivity function must be positioned below the plot of inverse of stable uncertainty weighting function ($W_m(j\omega)$) which is indicated by Fig.6b. The current and voltage response of the individual stage and combined model is observed for parametric variations. The output voltage at individual stages of SST is maintained constant and the stable response of the combined SST demonstrates the robustness of the controllers as portrayed in Fig.7. Here, the uncontrolled and controlled response of rectifier are compared under parametric variations. From the response, it can be seen that the rectifier output remain unaffected under parametric uncertainties.



(a) (b)

Fig. 6: Bode plot for DAB controller indicating robustness using(a) uncertainty bounds and multiplicative uncertainty function (b) complimentary sensitivity function

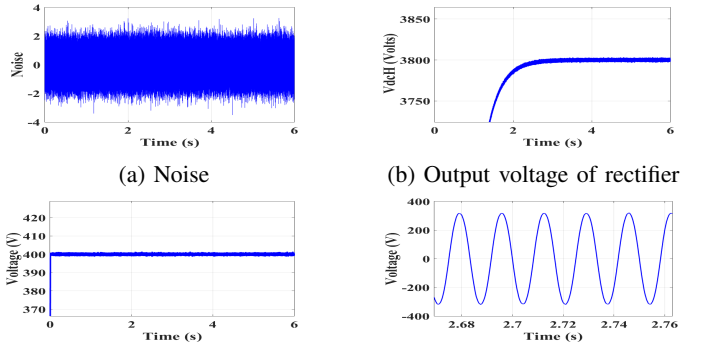


(a) (b)

Fig. 7: Output voltage response of rectifier for changes in inductor value indicating robustness (a) uncontrolled response (b) controlled response

D. Attenuation of measurement noise

The random noise of variance 0.5 and sample time of 0.0001 is added in the output to check the effectiveness of the controller. With the designed controllers, the measurement noise is considerably attenuated. Fig.8 shows the response of various stages of SST against the measurement noise.



(a) Noise (b) Output voltage of rectifier

(c) Output voltage of DAB (d) Output voltage of inverter

Fig. 8: Performance of SST with measurement noise

E. Hardware-in-Loop Experimental Results

The performance of SST under load and input voltage variations is verified via real time simulation being carried out with HIL using Opal-RT and dSPACE. The real time simulation response is observed to regulate HVDC link voltage of 3800V for rectifier, LVDC link voltage of 400V for DAB and 230V RMS for inverter for $\pm 10\%$ variations in input voltage and load. The experimental setup required for HIL interface is demonstrated in Fig. 9. Fig.10 show the response of DAB as a representative case of SST with real time simulation.

The responses are in close agreement with the MATLAB/Simulink results. Fig. 11 shows the oscilloscope response of inverter as a representative case for the three stages of SST.

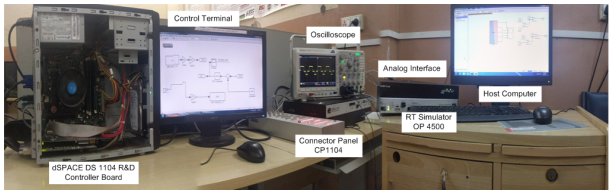
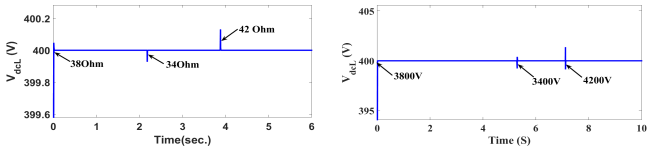
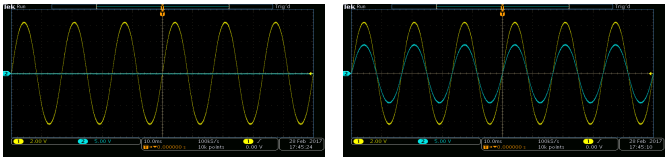


Fig. 9: Hardware-in-Loop test bed



(a) (b)

Fig. 10: HIL performance of DAB output voltage for(a) load variations (b) voltage variations



(a) Inverter output voltage (b) Inverter load voltage and current

Fig. 11: Oscilloscope readings of Inverter

V. Conclusions and Future Scope

This paper develops a mathematical model for rectifier and inverter in phasor domain with *dq* transformation, and uses phasor model for the DAB. The goal of the approach is to synthesise a robust PI controller that achieves high dynamic performance. The proposed model and the control strategy are analysed under the input voltage variation, step change in the load and parametric variations. The proposed control scheme of dynamic phasor–based nested PI control with *dq* transformation for the ac/dc converters improves the effectiveness of the controller as compared to the DP-based direct voltage control. In addition the ripple voltage is significantly reduced and the dynamic performance is considerably improved over average model. The design of PI controller gains using loop shaping technique assures the robustness and rejection of the load disturbances and the measurement noise. The small gain theorem is used to establish the robustness of the designed controllers. We see two directions for future work - extending the controller design to address the destabilising characteristics of constant-power loads that are proliferating in distribution networks, and coordination among multiple SSTs in a microgrid. We believe that the work presented here provides useful pointers for both tasks.

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