Perspective: Magneto-electric antiferromagnetic spin-orbit logic devices

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Abstract: As electronic integrated circuits are scaled to ever smaller sizes, they run into the obstacle of excessive power dissipation. Spintronic devices hold the promise of alleviating this problem via improved energy efficiency. Research effort around a promising class of such devices based on antiferromagnetic materials and magnetoelectric switching is reviewed.

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Integrated circuits were, and continues to be, scaled in the number of logic gates, in accordance with Moore's law [1]. In this process, integrated circuit technologies encounter the hurdle of increasing power dissipation [2]. Solution to the problems of power density and the limits to device size may be provided by computing devices with lower switching energy and possessing the property of non-volatility. One class of such of 'beyond CMOS' devices is based on magneto-electric (ME) switching [3-9]. In this work we review several such devices incorporating antiferromagnetic materials.

In the field of antiferromagnetic devices concepts, attention has shifted to the magneto-electric (ME) spin field effect transistor (MEFET) [4,5,7-15]. The ME field effect transistor (MEFET) resembles the conventional CMOS device, with some differences. The spin polarization of the semiconductor channel, by the boundary polarization of the ME gate, layer through the proximity effect, is the typical premise of most, if not all, of the ME transistor schemes [5,7]. Yet ferromagnetism is not required for these spintronic devices. Although magnetic electrodes at the source and drain could improve the device on/off ratio, there is no need for magnetization reversal, of the ferromagnetic contact(s) shown in Figure 1. These devices are nonvolatile, because once in the single domain state, the boundary polarization is either "up" or "down" and this leads to polarization of the current in the semiconductor channel. A number of different versions of MEFET have been proposed, but the simplest option is a single source, single drain version as shown in Figure 1.
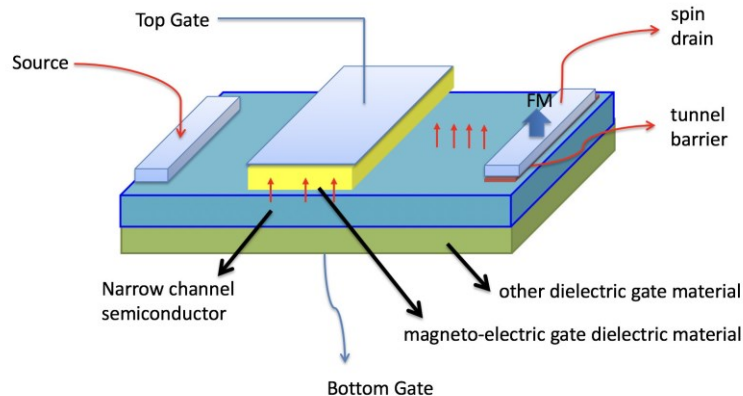

Figure 1. The basic top and bottom gated magneto-electric spin-FET (MEFET) with a ferromagnetic (FM) source or drain. The orientation of the ferromagnetic source or drain is not altered as part of the device operation but left fixed. The narrow channel conductor/semiconductor is any suitable material with a 2-dimensional semiconductor channel. Adapted from [8]. Reproduced, with permission, copyright 2020 Institute of Physics Publishing.

A significant advantage to the MEFET is that such schemes avoid the complexity and detrimental switching energetics associated with ME exchange-coupled ferromagnetic devices, instead being based solely on the switching of a dielectric magneto-electric. As a result, switching speed is limited only by the switching dynamics of the antiferromagnetic ME material under an applied voltage [6,8,9,13,14,16]. With coherent rotation, as the domain switching mechanism, the

switching speed might be as fast as 5 to 6 ps [16]. Moreover, these ME devices promise to provide a unique field effect spin transistor (spin-FET) that could lead to more compact circuits as well as an interface for input/output to other emerging computational devices. Assuming coherent rotation of the antiferromagnetic domains, then faster write speeds (<20 ps per element) [6,16], at a lower cost in energy (<20 aJ per element) [6,8,9] are possible for the MEFET, because there is no ferromagnetic domain reversal. These ME field effect transistors (ME-FET) do differ from the conventional field transistor in that the ME-FET must be both top and bottom gated, to provide an electric field across the magneto-electric layer, so the result is that this is a 4, not 3 terminal transistor [4,5,7-9,13], as illustrated in Figure 1. This MEFET device may, in principle, operate with an applied gate voltage of as low as around 100 mV. In addition, MEFET devices have an inherent memory due to the non-volatile AFM ordering of the ME and should have a sharp turn-on voltage [4,5,7-9,13]. All of these are useful features of logic components. This device also has
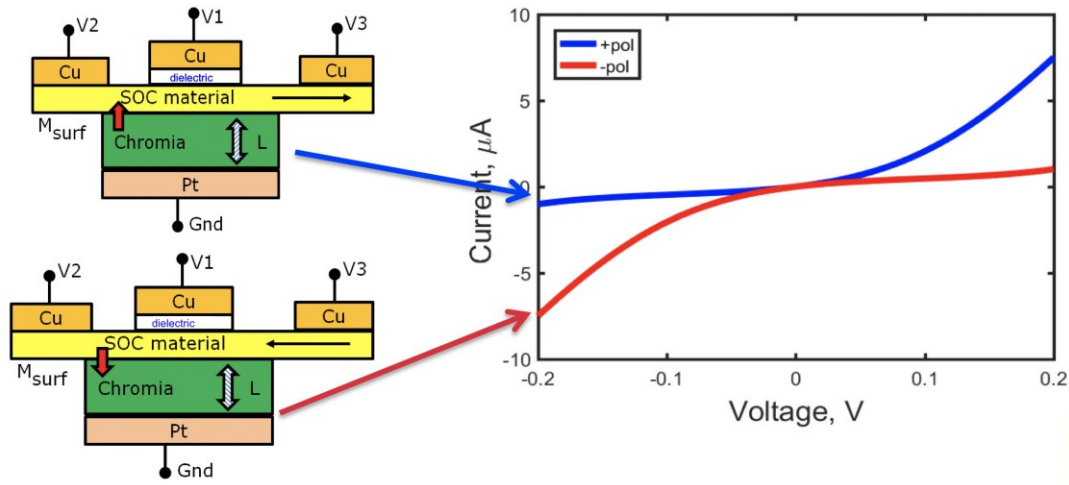

Figure 2. The cross-sectional views show the scheme of anti-ferromagnet spin orbit read (AFSOR) logic. upper) The state with positive V1 applied and the surface or interface magnetization of the magneto-electric gate M_{surf} pointing up. lower) The state with negative V1 applied and surface magnetization M_{surf} pointing down. The graph shows source to drain current versus voltage (adapted from [5,7]). Reproduced, with permission, copyright 2018 IEEE.

a potential on-off current ratio of ~ 10^6 [8,9], making the device comparable to CMOS logic devices.

The exchange coupling between the ME boundary polarization spin vectors, oriented in the 'up' or 'down' direction, and the semiconductor channel is expected to be significant for a material with large spin orbit coupling [5,7]. If the semiconductor channel has large spin-orbit coupling, then the device behaves, as schematically illustrated in Figure 2, and a combination of the spin-orbit coupling and the exchange with the boundary polarization creates a topologically protected current [5,7] in the absence of ferromagnetism. The MEFET majority gate, antiferromagnet spin orbit read (AFSOR) logic device type of Figure 2, requires, including clocking, only 6 components [8].

A variant of the antiferromagnet spin orbit read (AFSOR) logic device type of Figure 2, where inversion symmetry is not as strictly broken, results in a nonvolatile spintronic version of multiplexer (spin-MUX) logic [5,7-9], illustrated in Figure 3. The ME spin-FET multiplexer (spin-
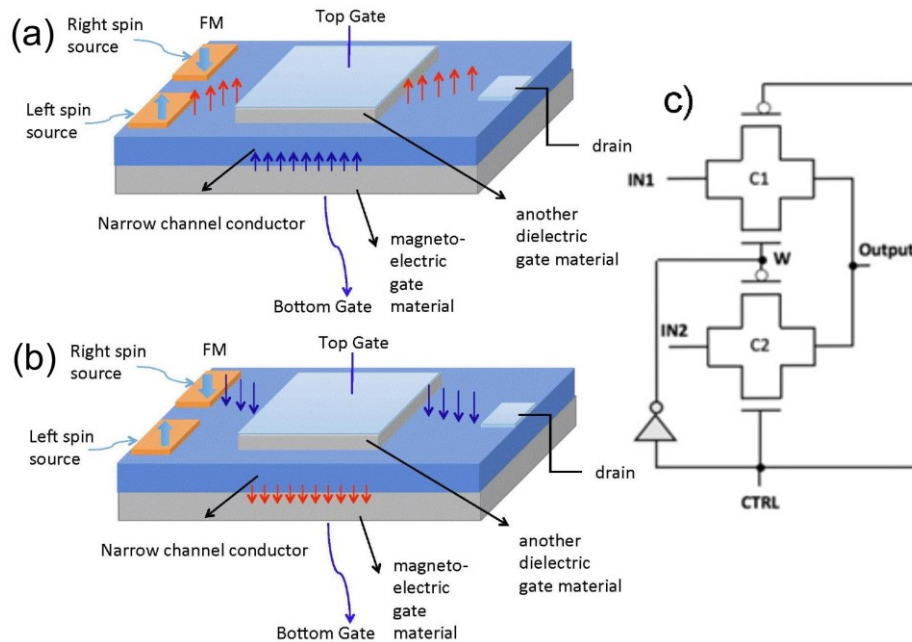
Figure 3. The nonvolatile ME spinFET multiplexer (spin-MUX), can also be constructed with ferromagnetic source contacts. The orientation of the ferromagnetic sources is not altered as part of the device operation but left fixed. The thin channel conductor/semiconductor is polarized (a) up or (b) down. The CMOS equivalent is schematically indicated in (c). Adapted from [5,7]. Reproduced, with permission, copyright 2018 IEEE.

MUX) of Figure 3 also exploits changes to the direction of a spin current, through the manipulation of the spin-orbit splitting of the electronic bands of the semiconductor channel through a "proximity" magnetic field derived from a voltage-controlled ME material [5,7,8,14]. This is somewhat akin to an 'inverse' anomalous Hall effect transistor [14]. A suitably chosen semiconductor channels with large spin-orbit coupling, one might obtain a transverse spin Hall current, as well as a spin current overall. The nonvolatile ME spinFET multiplexer (spin-MUXER) based full-adder, could be quite compact, requiring as few as 8 device elements [8].

The MEFET of Figure 4, the split gate MEFET, does allow for even more compact gates, however. For example, one might start out with the XNOR gate but a MEFET device, of the style of Figure 2, but where the chromia gate is polarized in series either up or down would make a two input (gate) device. This style of split gate device reduces the component count of the XNOR to just two devices, including the pull-up [8]. The silicon CMOS majority gate typically requires 13 components. The MEFET majority gate, anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4, requires, including clocking, only 6 components [8].

The three critical components of the efficient technology, i.e. non-volatility, low power and potentially high switching speed, are a significant attraction to using devices based on ME materials. The ME materials also provide a unique way to read out and transmit the information – through roughness insensitive boundary spin polarization [17-22], which is intrinsically coupled to the antiferromagnetic order [23,24]. The ME spintronic devices, which avoid the necessity of switching a ferromagnet [5,7,8,9], a bottleneck for energy-efficiency and operation speed, are much sought after, as we have already indicated. The spin-wave spectrum, of an antiferromagnet,

reveals much higher spin-wave frequencies in comparison to those in ferromagnets. For example, optical manipulation has shown THz response for $KNiF_3$ [25,26], NiO [27], and CuB_2O_4 [28]. Switching of the AFM order parameter might thus be performed at ultra-fast frequencies, potentially reaching the THz regime. Thus, using ME antiferromagnets potentially allows for an increase in the switching speed by nearly three orders of magnitude compared to conventional magnetic memory and logic devices. This is an implementation of spintronics without
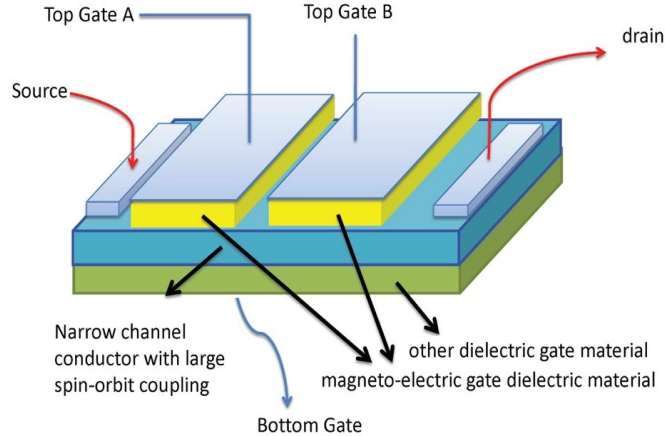

Figure 4. The scheme for a split top gated MEFET based on the anti-ferromagnet spin orbit read (AFSOR) of Figure 2, for more compact logic gate circuits. Note the common bottom gate as well as top gates. Adapted from [8]. Reproduced, with permission, copyright 2020 Institute of Physics Publishing.

ferromagnetism, as the electrical switching of the AFM order parameter is accompanied by reversal of boundary magnetization, which allows for a plethora of functionalities and a wide range of device concepts.

Voltage-controlled boundary magnetization of ME antiferromagnets is the key functional element for these potentially revolutionary devices. Boundary magnetization is a generic property at the interface of all ME single-domain antiferromagnets [23,24]. In the archetypical ME antiferromagnet chromia (α-Cr_2O_3), an AFM single domain state can be selected out of two degenerate AFM 180-degree domains by magneto-electrically lifting the degeneracy [29]. Isothermal switching between the single domain states is achieved when an electric field, $\underline{E}$, and a small symmetry breaking magnetic field, $\underline{H}$, are simultaneously applied such that the magnitude of the product $\underline{E} \bullet \underline{H}$ overcomes a critical threshold [24,30]. Note that the symmetry breaking H-field can be scaled down to arbitrary small values when the applied E-field is scaled up accordingly.

Early on, in the development memory and logic device concepts, there was the magnetic tunnel junction structure [3,31,32] built around magneto-electric effects, and exchange bias, but the slow switching speed of the ferromagnet was clearly a major impediment. Even the magnetoelectric (ME) magnetic tunnel junctions (MTJ) devices [3,4,31,32] have several important advantages compared to more conventional based on magnetic tunnel junctions (MTJs) and spin transfer torque (STT) or spin orbit torque (SOT), used in for example, magnetic random-access memories (MRAM) [33,34]. The magneto-electric MTJ's (ME-MTJ) operation is based on switching of a free ferromagnetic layer, resulting in the change of the magnetoresistance of a stack of materials. The speed of this operation is determined by the time required to rotate the

magnetization of the nanomagnet which is typically a few nanoseconds. This is more than two orders in magnitude slower than charging a capacitor and requires about two orders of magnitude more energy, as is implemented in the complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET) [6]. ME devices use the same mechanism as charging a capacitor. Although the switching of an ME-MTJs is much slower than CMOS, ME-MTJs devices hold a promise to be switched with an even smaller energy due to lower switching voltage.

Other ME devices, like the composite–input ME–based logic technology (CoMET) [35] also had major limits on switching speed. The CoMET style devices are limited by the switching speed of the ferroelectric and domain wall motion. The basis of these devices is that an input switches a ferroelectric material, in contact with a ferromagnet with in-plane magnetic anisotropy, placed on top of an intra-gate ferromagnet interconnect with perpendicular magnetic anisotropy. The operational idea was that the input voltage nucleates a domain wall, while the current would drive the domain wall to the output end of the device. A similar ME device structure was proposed [36], but now using spin-orbit coupling. Both of these device concepts should have long delay times because of the slow switching speed of the ferromagnetic layer, and in the case of the CoMET device, the additional complications of the slow speed of ferromagnetic domain wall propagation. While using higher currents might drive the domain wall at faster velocities, this will come at an energy cost. Also using spin orbit coupling, the nonvolatile magneto-electric spin-orbit (MESO) [37,38] and inverse Rashba-Edelstein magneto-electric neuron (IRMEN) [39,40] logic device concepts were proposed using a magneto-electric layer for electrical control of exchange bias of a laterally scaled spin valve. The delay time MESO and IRMEN logic devices will still limited by the switching speed of the ferromagnetic layer.

The future is uncertain, primarily because the applicable mechanisms for ME antiferromagnetic domain reversal have not been conclusively determined. If the mechanism is coherent rotation the ME device is certainly viable as the device switching speed is expected to be in the range of tens of ps or less [6,16], as noted above. If the domain reversal proceeds by domain wall propagation then the switching speed will be in the region of 1 to 10 ns, or more [16,41]. In the latter case memory applications are certainly to be considered, but logic operations competitive with CMOS would not be possible.

Anomalous Hall effect (AHE) devices have now been fabricated [19-21], with a nominally non-magnetic Hall bar on top of ME antiferromagnetic chromia. These devices have a demonstrated readout mechanism for the memory state, via an AHE-like signal [19-21]. This is in fact a variation of the spin Hall magnetoresistance. While the overall Hall voltage ratio is very small, at least for the devices demonstrated thus far, these devices do demonstrate that ME devices can be constructed so as to fabricate a spintronics device without any ferromagnet. Semiconductors, with large spin orbit coupling are anticipated to have far higher values of the Hall voltage.

In summary, recent years have seen a surge of research activity in various concepts of spintronic devices based on magneto-electric (ME) switching and often involving spin-orbit effects. These devices, if successfully implemented, have a high chance of providing spin logic with unparalleled energy efficiency and competitive switching speed.

Acknowledgements

References:

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics* **38**, 114-117 (1965).

[2] M. T. Bohr and I. A. Young, "CMOS Scaling Trends and Beyond," *IEEE Micro*. **37**, 20-29 (2017).

[3] C. Binek, B. Doudin, "Magnetoelectronics with magnetoelectrics", *J. Phys. Condens. Matter* **17**, L39-44 (2005).

[4] P. A. Dowben, C. Binek, and D. E. Nikonov, "Potential of nonvolatile magnetoelectric devices for spintronic applications", Chapter 11 in <u>Nanoscale Silicon Devices</u>; edited by Shuni Oda and David Ferry; Taylor and Francis (London) (2016) pp 255-278, ISBN 9781482228670

[5] P. A. Dowben, C. Binek, K. Zhang, L. Wang, W.-N. Mei, J. P. Bird, U. Singisetti, X. Hong, K. L. Wang, D. Nikonov, "Towards a Strong Spin-Orbit Coupling Magnetoelectric Transistor", *IEEE Journal of Exploratory Solid-State Computational Devices and Circuits* **4,** 1-9 (2018); doi: 10.1109/JXCDC.2018.2809640

[6] D. E. Nikonov and I. A. Young, "Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits," *IEEE J. Exploratory Solid-State Comput. Devices Circuits* **1**, 3-11 (2015).

[7] D. E. Nikonov, C. Binek, X. Hong, J. P. Bird, K. L. Wang, P. A. Dowben, "Magneto-Electric Logic Devices Using Semiconductor Channel with Large Spin-Orbit Coupling", U.S. Patent 10,361,292 B2, issued July 23, 2019

[8] N. Sharma, J. P. Bird, Ch. Binek, P. A. Dowben, D. Nikonov, and A. Marshall, "Evolving Magneto-electric Device Technologies", *Solid State Science and Technology* (2020), in press

[9] N. Sharma, A. Marshall, J. Bird, P. A. Dowben, "Verilog-A based Compact Modeling of the ME-FET device", 2017 Fifth Berkeley Symposium on *Symposium & Steep Transistors Workshop (E3S) IEEE Xplore* (2018) INSPEC Accession Number: 17453928; doi: 10.1109/E3S.2017.8246186

[10] S. Cao, Z. Xiao, C.-P. Kwan, K. Zhang, J. P. Bird, L. Wang, W.-N. Mei, X. Hong, P. A. Dowben, "Moving towards the magnetoelectric graphene transistor", *Appl. Phys. Lett.* **111**, 182402 (2017)

[11] R. Choudhary, P. Kumar, P. Manchanda, D. J. Sellmyer, P. A. Dowben, A. Kashyap, R. Skomski, "Interface-induced spin polarization in graphene on chromia", *IEEE Magn. Lett.* **7**, 4 (2016)

[12] J. Kelber, C. Binek, P. A. Dowben, K. Belashchenko, "Magneto-electric voltage controlled spin transistors", US patent 9,379,232 B2 issued 28-Jun-2016

[13] C. Pan, and A. Naeemi, "Complementary Logic Implementation for Antiferromagnet Field-Effect Transistors", *IEEE J. Exploratory Solid-State Computational Devices and Circuits* **4**, 69 (2018)

[14] H. Takenaka, S. Sandhoefner, A. A. Kovalev, and E. Y. Tsymbal, "Magnetoelectric control of topological phases in graphene", *Phys. Rev. B* **100**, 125156 (2019)

[15] S. C. Stuart, B. Gray, D. Nevola, L. Su, E. Sachet, M. Ulrich, D. B. Dougherty, "Magnetoelectric oxide films for spin manipulation in graphene", *Phys. Status Solidi RRL* **10**, 242-247 (2016).

[16] A. Parthasarathy, S. Rakheja, "Dynamics of magnetoelectric reversal of an antiferromagnetic domain", *Physics Review Applied* **11**, 034051 (2019)

[17] S. Cao, X. Zhang, N. Wu, A. T. N'Diaye, G. Chen, A. K. Schmid, X. Chen, W. Echtenkamp, A. Enders, Ch. Binek, P. A. Dowben, "Spin Polarization Asymmetry at the Surface of Chromia", *New Journal of Physics* **16**, 073021 (2014).

[18] X. He, Y. Wang, N. Wu, A.N. Caruso, E. Vescovo, K. D. Belashchenko, P. A. Dowben, C. Binek, "Robust isothermal electric control of exchange bias at room temperature", *Nat. Mater.* **9**, 579-585 (2010); doi:10.1038/nmat2785

[19] T. Kosub, M. Kopte, F. Radu, O. G. Schmidt, D. Makarov, "All-electric access to the magnetic-field-invariant magnetization of antiferromagnets", *Phys. Rev. Lett.* **115**, 097201 (2015)

[20] T. Kosub , M. Kopte, R. Hühne, P. Appel, B. Shields, P. Maletinsky, R. Hübner, M. O. Liedke, J. Fassbender, O. G. Schmidt, D. Makarov, "Purely antiferromagnetic magnetoelectric random access memory", *Nat. Commun.* **8,** 13985 (2017)

[21] J.-L. Wang, W. Echtenkamp, A. Mahmood, C. Binek, "Voltage controlled magnetism in Cr_2O_3 based all-thin-film systems", *J. Magn. Magn. Mater.* **486**, 165262 (2019)

[22] N. Wu, X. He, A. Wysocki, U. Lanke, T. Komesu, K. D. Belashchenko, C. Binek and P. A. Dowben, "Imaging and control of surface magnetization domains in a magnetoelectric antiferromagnet", *Phys. Rev. Lett.* **106** (2011) 087202

[23] A. F. Andreev, "Macroscopic magnetic fields of antiferromagnets", *JETP Lett.* **63**, 758-762 (1996); doi: 10.1134/1.566978

[24] K. D. Belashchenko, "Equilibrium Magnetization at the Boundary of a Magnetoelectric Antiferromagnet", *Phys. Rev. Lett.* **105**, 147204 (2010); doi: 10.1103/PhysRevLett.105.147204

[25]   D. Bossini, S. Dal Conte, Y. Hashimoto, A. Secchi, R. V. Pisarev, Th. Rasing, G. Cerullo and A. V. Kimel, "Macrospin dynamics in antiferromagnets triggered by sub-20 femtosecond injection of nanomagnons", *Nat. Comm.* **7**, 10645 (2016).

[26] D. Bossini, S. Dal Conte, G. Cerullo, O. Gomonay, R. V. Pisarev, M. Borovsak, D. Mihailovic, J. Sinova, J. H. Mentink, Th. Rasing, A. V. Kimmel, "Laser-driven quantum magnonics and terahertz dynamics of the order parameter in antiferromagnets", *Phys. Rev. B* **100**, 024428 (2019); doi: 10.1103/PhysRevB.100.024428

[27] S. Baierl, J. H. Mentink, M. Hohenleutner, L. Braun, T. M. Do, C. Lange, A. Sell, M. Fiebig, G. Woltersdorf, T. Kampfrath, R. Huber, "Terahertz-Driven Nonlinear Spin Response of Antiferromagnetic Nickel Oxide", *Phys. Rev. Lett.* **117**, 197201 (2016); doi: 10.1103/PhysRevLett.117.197201

[28] D. Bossini, K. Konishi, S. Toyoda, T. Arima, J. Yumoto, M. Kuwata-Gonokami, "Femtosecond activation of magnetoelectricity", *Nature Physics* **14**, 370 (2018); doi: 10.1038/s41567-017-0036-1

[29] T. H. O´Dell, "The electrodynamics of magneto-electric media", *Philosophical Magazine* **7**, 1653-1669 (1962); doi: 10.1080/14786436208213701

[30] S. Mu, A. L. Wysocki, K. D. Belashchenko, "First-principles microscopic model of exchange-driven magnetoelectric response with application to Cr_2O_3", *Phys. Rev. B* **89**, 174413 (2014); doi: 10.1103/PhysRevB.89.174413

[31] M. Bibes, A. Barthélémy, "Multiferroics: Towards a magnetoelectric memory", *Nat. Mater.* **7**, 425-426 (2008)

[32] X. Chen, A. Hochstrat, P. Borisov, W. Kleemann, "Magnetoelectric exchange bias systems in spintronics", *Appl. Phys. Lett.* **89**, 202508 (2006)

[33] K. L. Wang, J. G. Alzate, P. Khalili Amiri, "Low-power non-volatile spintronic memory: STT-RAM and beyond", *J. Phys. D: Appl. Phys.* **46**, 074003 (2013); doi:10.1088/0022-3727/46/7/074003

[34] A. V. Khvalkovskiy, D. Apalkov, S. Watts, R. Chepulskii, R. S. Beach, A. Ong, X. Tang, A. Driskill-Smith, W. H. Butler, P. B. Visscher, D. Lottis, E. Chen, V. Nikitin and M. Krounbi, "Basic principles of STT-MRAM cell operation in memory arrays", *J. Phys. D: Appl. Phys.* **46**, 074001 (2013); doi:10.1088/0022-3727/46/7/074001

[35] M. G. Mankalale, Z. Liang, Z. Zhao, C. H. Kim, J. -P. Wang, S. S. Sapatnekar, "CoMET: Composite-input magnetoelectric- based logic technology", *IEEE J. Explor. Solid-State Computat.* **3,** 27 (2017).

[36] M. Kazemi, "An electrically reconfigurable logic gate intrinsically enabled by spin-orbit materials: An electrically reconfigurable logic gate intrinsically enabled by spin-orbit materials", *Sci. Rep.* **7**, 15358 (2017)

[37] S. Manipatruni, D. E. Nikonov, R. Ramesh, H. Liu, I. A. Young, "Spin-orbit logic with magnetoelectric nodes: A scalable charge mediated nonvolatile spintronic logic", arXiv:1512.05428 (2015/2017)

[38] S. Manipatruni1, D. E. Nikonov, C.-C. Lin, T. A. Gosavi, H. Liu, B. Prasad, Y.-L. Huang, E. Bonturim, R. Ramesh, I. A. Young, "Scalable energy-efficient magnetoelectric spin–orbit logic", *Nature* **565**, 35 (2019); doi: 10.1038/s41586-018-0770-2

[39] A. W. Stephan, J. Hu, S. J. Koester, "Performance Estimate of Inverse Rashba-Edelstein Magnetoelectric Devices for Neuromorphic Computing", *IEEE J. Exploratory Solid-State Computational Devices and Circuits* **5,** 25 (2019); doi: 10.1109/JXCDC.2019.2903286

[40]   A. W. Stephan, Q. Lou, M. Niemier, X. S. Hu, S. J. Koester, "Nonvolatile Spintronic Memory Cells for Neural Networks", arXiv:1905.12679v1 [cs.ET] 29 May 2019

[41] K. D. Belashchenko, O. Tchernyshyov, A. A. Kovalev, and O. A. Tretiakov, "Magnetoelectric domain wall dynamics and its implications for magnetoelectric memory", *Appl. Phys. Lett.* **108**, 132403 (2016); doi: 10.1063/1.4944996