

Development of dynamic phasor based higher index model for performance enhancement of dual active bridge

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ABSTRACT

Renewable energy integration and control in microgrid demands computationally efficient model along with effective control methodology for switched converters. The dual active bridge (DAB) being an integral part of the microgrid suffers from the stability issues. This research proposes dynamic phasor (DP) based higher index model of DAB and demonstrates the effect of appropriate selection of model on performance. To evaluate the system stability for performance objectives of voltage regulation, suppression of measurement noise, sinusoidal disturbances and robustness, a robust control strategy based on loop shaping technique for DP model of DAB is proposed. Comparison of the responses of the higher index model with existing DP model with dc and index 1 terms makes apparent the benefits of the proposed model. The Hardware-in-Loop (HIL) simulation using Opal-RT and dSPACE simulators is carried out for validation of the proposed control scheme.

1. Introduction

Switched converters play a central role in present ecosystem of renewable energy and its utilization. The switched conversion circuit must meet three design targets [1]: high performance voltage regulation, bi-directional power flow capability and galvanic isolation for safety regulations. All these targets are met in DAB, a dc to dc converter. The DAB converter which was originally proposed in [2] is a high efficiency buck and boost, bidirectional dc to dc converter isolated by a high-frequency transformer. It is used to convert electric energy between a low voltage battery and a high voltage DC bus. The interfacing of several DC sources and loads is possible due to multi-port operation feature of DAB. The adoption of DAB in power distribution system (photo-voltaic and wind energy, energy storage such as super-capacitor and battery) and hybrid and electric vehicle demands superior dynamic behavior.

Analysis of the dynamic behavior of DAB when interacting with grid and renewables necessitates computationally efficient model. Detailed models provide very accurate simulation results. However, these are unsuitable for controller design [3] as these result in time varying systems without stationary equilibrium points. The state-space averaging (SSA) method as proposed in [4] is the preferred choice for the power electronic converter modeling as this gives faster simulation. However, this method replaces the switching function with its fast

average and thus is incapable of representing the switching ripples in converters, hence have reduced model accuracy. This restricts the use of average model in designing the switching ripple based control schemes as explained in [5].

The solution exists with the dynamic phasor (DP) model, based on generalized averaging method (GAM). In this method, the periodic or near periodic waveforms are represented by their time varying Fourier coefficient called dynamic phasors. The DP approach approximates a periodically switched system with a continuous system. The phasor models have many useful features as explained in [6]. Inclusion of higher harmonic frequency terms in the DP model increases the number of system states considerably, hence most of the modelling approaches available in literature are based on GAM with first harmonic approximation (FHA). This truncation of the Fourier series at the first harmonic leads to the large signal modelling error as suggested in [7]. It proposes the DAB operation with improvement in the modulation strategies by including more general terms as dual, extended, and triple phase shift modulation. A reduced-order large and small signal average-value model (RAVM) for DAB is proposed in [8] considering conduction and transformer power losses as well as the input/output filters, which requires much less computations than detailed models. Another modelling technique for DAB based on an improved FHA (I-FHA) method is proposed in [9]. This method introduces a correction factor to compensate for the inaccuracy in conventional FHA modeling technique. In

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literature, various authors have proposed linear control methods using PI controllers for addressing the voltage regulation issue of DAB. In [1] the performance limits of PI controller are investigated for harmonic model of DAB, whereas [10] analyses performance of PI controller for DAB as one of the stages of solid-state transformer (SST) by developing its average model. In [11], the DP model for DAB is proposed and the voltage regulation is achieved using PI controller. In [12], the need of wide bandwidth sensors for the measurement of high frequency transformer current is eliminated by estimating it using reduced order PI observer and then feed forwarding it to voltage control loop for desired performance, whereas [13] proposes DP based IMC-PI controller for voltage regulation of SST(DAB being one of the stages). In [14] the modeling of DC subsystem consisting of one primary and N-1 load side DABs is proposed using GAM. The scalability issue of the GAM model is addressed by preserving the decoupling of the relevant state equations. The voltage regulation of the primary converter is achieved through PI control. To achieve a wide stability region, [15] proposes a nonlinear interconnection and damping assignment passivity-based control (IDA-PBC) for port-controlled phasor Hamiltonian (PCPH) model of SST to attain load and input disturbance rejection. However, in most of the approaches the performance objective is only the voltage regulation for the design of PI controller. This research aims to design a robust control scheme for DAB and highlights the performance enhancement with appropriate selection of model for DAB.

The main contributions of the research are:

1. Although ample literature is available on DP based modelling of the DAB converter, all are based on the FHA. The novelty of this research is the development of DP based higher index model of DAB.
2. Designing a robust control scheme based on the DP model of DAB with index 1 using loop shaping technique to evaluate the system stability for the performance objectives of voltage regulation, robustness, attenuation of measurement noise and rejection of sinusoidal disturbances.
3. Demonstration of the effect of appropriate selection of model on stability by comparing the response of the existing DP model of DAB with DC and index 1 terms as proposed in [16] and [17] with the higher index DP model of DAB based on GAM proposed in this paper.
4. Experimental validation of the proposed scheme through HIL simulation using Opal-RT and dSPACE simulators.

The paper is organized as follows: Section 2 describes application of the concepts of DP for the development of the higher index model of DAB. Section 3 explains the loop shaping method for the controller design and the small gain theorem for the robustness of the controller. Section 4 assess the effectiveness of the controller for the desired performance objectives. Section 5 analyses the open loop and the closed loop performance of DAB in comparison with higher index model and it also explores the effect of adding the higher index terms in the model and on the dynamic performance. Section 6 explains the hardware-in-loop implementation of the system and validates the results. Section 7 outlines the brief conclusions.

2. Development of higher index DP model

2.1. Dynamic phasors

The generalized averaging method proposed in [18] is referred as the DP approach wherein a complex time varying signal is demodulated to its components in the interval $(t - T, t)$ with a Fourier series representation. DP based models signify a conciliation between the high model reliability of detailed models and the fast simulation run times of SSA models [3]. In DP approach, the complex time domain waveform $x(t)$ is approximated in the interval $(t - T, t)$ with a Fourier series representation as:

$$x(\tau) = \sum_{k=-\infty}^{\infty} X_k(t) e^{jk\omega_s \tau} \quad (1)$$

where $\omega_s = \frac{2\pi}{T}$, T is the sampling frequency and $X_k(t)$ is the k th time varying Fourier coefficient in complex form called as DP and k is the set of selected Fourier coefficients which provide a good approximation as explained in [19] of the original waveform (e.g. $k = 0, 1, 2, 3 \dots n$). The relation between derivative of variable $x(t)$ and the derivatives of k th Fourier coefficient is expressed as:

$$\left\langle \frac{dx}{dt} \right\rangle_k = \frac{d}{dt} \langle x \rangle_k + j k \omega_s \langle x \rangle_k \quad (2)$$

Another key property of dynamic phasors is, the product of two time-domain variables equals a discrete time convolution of the two dynamic phasor sets of the variables, expressed as:

$$\langle xy \rangle_k = \sum_{l=-\infty}^{\infty} (X_{k-l} Y_l) \quad (3)$$

The systems with control objectives of reduction of harmonic distortion and switching losses are appropriately modelled using DP approach in [5]. The concepts presented in this section form a basis for developing DP based higher index model of DAB.

2.2. Higher index model of DAB

This section proposes a higher index DP model of DAB. The design specifications of DAB as shown in Fig. 1, comprises of a high voltage H-Bridge connected to the 3.8 KV D.C. source, a high frequency transformer and a low voltage H-bridge connected to either load or the fuel cell or PV source. The DAB converter regulates the LVDC link voltage at 400 V.

The output voltage of DAB converter is controlled using phase shift modulation (PSM) with fixed 50% duty ratio and fixed switching frequency [16]. The phase shift angle between the two bridges is ϕ and the duty ratio of the lagging bridge is expressed as: $d_2 = \frac{\phi}{\pi}$ with real power flow directed from leading bridge to the lagging bridge. The development of the higher index DP based model of DAB is centered on its state space model and the concepts presented in Section 2.1. The generalized higher index model of DAB is represented as:

$$\langle \dot{i}_{tp} \rangle_k^R = k\omega \langle i_{tp} \rangle_k^I + \frac{\langle SD1 \rangle_k^R \langle v_{dcl} \rangle_0}{L_t} - \frac{R_t \langle i_{tp} \rangle_k^R}{L_t} - \frac{\langle SD2 \rangle_k^R \langle v_{dcl} \rangle_0}{L_t} \quad (4)$$

$$\langle \dot{i}_{tp} \rangle_k^I = -k\omega \langle i_{tp} \rangle_k^R + \frac{\langle SD1 \rangle_k^I \langle v_{dcl} \rangle_0}{L_t} - \frac{R_t \langle i_{tp} \rangle_k^I}{L_t} - \frac{\langle SD2 \rangle_k^I \langle v_{dcl} \rangle_0}{L_t} \quad (5)$$

$$\langle \dot{v}_{dcl} \rangle_0 = \frac{1}{C_{dcl}} [\langle SD2 \rangle_0 \langle i_{tp} \rangle_0 + 2 \sum_{k=1}^n (\langle SD2 \rangle_k^R \langle i_{tp} \rangle_k^R + \langle SD2 \rangle_k^I \langle i_{tp} \rangle_k^I) - \langle v_{dcl} \rangle_0 / R_L] \quad (6)$$

The generalized switching functions with higher index terms for both the bridges are expressed in Table 1.

The higher index model of DAB is derived using (4)–(6) by considering only odd harmonic terms as for the symmetrical waveforms the even harmonics are mostly absent. Hence, considering $k = 0, 1, 3, 5$, the model is expressed by (7). The controller design methodology using a linearized DP based small signal model [20] of DAB expressed by (19) is explained in the following section.

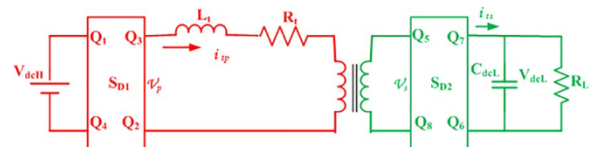


Fig. 1. DAB schematic.

$$\begin{bmatrix} \langle \dot{i}_{tp} \rangle_1^R \\ \langle \dot{i}_{tp} \rangle_1^I \\ \langle \dot{i}_{tp} \rangle_3^R \\ \langle \dot{i}_{tp} \rangle_3^I \\ \langle \dot{i}_{tp} \rangle_5^R \\ \langle \dot{i}_{tp} \rangle_5^I \\ \langle \dot{v}_{dcl} \rangle_0 \end{bmatrix} = \begin{bmatrix} \frac{-R_t}{L_t} & \omega & 0 & 0 & 0 & 0 & \frac{-\langle S_{D2} \rangle_1^R}{L_t} \\ -\omega & \frac{-R_t}{L_t} & 0 & 0 & 0 & 0 & \frac{-\langle S_{D2} \rangle_1^I}{L_t} \\ 0 & 0 & \frac{-R_t}{L_t} & 3\omega & 0 & 0 & \frac{-\langle S_{D2} \rangle_3^R}{L_t} \\ 0 & 0 & -3\omega & \frac{-R_t}{L_t} & 0 & 0 & \frac{-\langle S_{D2} \rangle_3^I}{L_t} \\ 0 & 0 & 0 & 0 & \frac{-R_t}{L_t} & 5\omega & \frac{-\langle S_{D2} \rangle_5^R}{L_t} \\ 0 & 0 & 0 & 0 & -5\omega & \frac{-R_t}{L_t} & \frac{-\langle S_{D2} \rangle_5^I}{L_t} \\ \frac{2\langle S_{D2} \rangle_1^R}{C_{dcl}} & \frac{2\langle S_{D2} \rangle_1^I}{C_{dcl}} & \frac{2\langle S_{D2} \rangle_3^R}{C_{dcl}} & \frac{2\langle S_{D2} \rangle_3^I}{C_{dcl}} & \frac{2\langle S_{D2} \rangle_5^R}{C_{dcl}} & \frac{2\langle S_{D2} \rangle_5^I}{C_{dcl}} & \frac{-1}{R_t C_{dcl}} \end{bmatrix} \begin{bmatrix} \langle i_{tp} \rangle_1^R \\ \langle i_{tp} \rangle_1^I \\ \langle i_{tp} \rangle_3^R \\ \langle i_{tp} \rangle_3^I \\ \langle i_{tp} \rangle_5^R \\ \langle i_{tp} \rangle_5^I \\ \langle v_{dcl} \rangle_0 \end{bmatrix} + \begin{bmatrix} \frac{\langle S_{D1} \rangle_1^R}{L_t} \\ \frac{\langle S_{D1} \rangle_1^I}{L_t} \\ \frac{\langle S_{D1} \rangle_3^R}{L_t} \\ \frac{\langle S_{D1} \rangle_3^I}{L_t} \\ \frac{\langle S_{D1} \rangle_5^R}{L_t} \\ \frac{\langle S_{D1} \rangle_5^I}{L_t} \\ 0 \end{bmatrix} \langle v_{dch} \rangle_0 \quad (7)$$

3. Controller design

The objective of the controller design is to analyze the stability of the system against input and load disturbances, model uncertainties and also to attain zero steady state error. This section discourses the methodology for the design of robust controller using loop shaping technique.

3.1. Loop shaping method

The loop shaping approach as explained in [21] involves to guarantee certain specifications related to sensitivity and complementary sensitivity functions by appropriate modeling of the singular values of the open loop response. The principle of loop-shaping method is to specify the open-loop response of the process on the basis of a specification related to several closed-loop transfer functions, that is to convert the desired specifications on the closed-loop system into constraints on the open-loop gain $L(s) = C(s)G(s)$. These constraints on open loop gain are used as the boundary conditions for design of controller $C(s)$. The shaping of the loop transfer function $L(s)$ is achieved using any of the classical controllers i.e. PID controllers or lead/lag compensators, Linear quadratic regulator (LQR) state feedback or Linear quadratic gaussian (LQG)/LQR output feedback controllers. For designing the feedback control law, the following performance objectives or the closed loop specifications as given in [22] are converted in to the open loop constraint:

1. Reference tracking: The constraint for the tracking error to be $k_{RT} \ll 1$ times smaller than the reference over the range of frequencies $[0, \omega_{RT}]$ as seen in [22] is expressed as:

$$\left| \frac{E(j\omega)}{R(j\omega)} \right| \leq k_{RT}, \quad \forall \omega \in [0, \omega_{RT}] \quad (8)$$

where $E(s)$ and $R(s)$ are the error signal and reference in 's' domain respectively. This leads to the constraint on the loop transfer function as:

$$|L(j\omega)| \geq 1 + \frac{1}{k_{RT}}, \quad \forall \omega \in [0, \omega_{RT}] \quad (9)$$

where k_{RT} is the reference tracking factor. Since, the references are the low frequency signals, the (8) requires the gain of the sensitivity function to be small in this region of frequencies which can be accomplished by a large gain of the $L(s)$.

Table 1
Switching functions of DAB for index 'k'.

Bridge 1	Bridge 2
$\langle S_{D1} \rangle_0 = 0$	$\langle S_{D2} \rangle_0 = 0$
$\langle S_{D1} \rangle_k^R = 0$	$\langle S_{D2} \rangle_k^R = -2 \sin(k\pi d_2)/k\pi$
$\langle S_{D1} \rangle_k^I = -2/k\pi$	$\langle S_{D2} \rangle_k^I = -2 \cos(k\pi d_2)/k\pi$

2. Disturbance rejection: The closed loop specification required to attenuate the input disturbances appearing in the output by at least $k_D \ll 1$ over the range of frequencies $[\omega_{D1}, \omega_{D2}]$ is expressed as:

$$\left| \frac{Y(j\omega)}{D(j\omega)} \right| \leq k_D, \quad \forall \omega \in [\omega_{D1}, \omega_{D2}] \quad (10)$$

This leads to the constraint on $L(s)$ as:

$$|L(j\omega)| \geq 1 + \frac{|P_0(j\omega)|}{k_D}, \quad \forall \omega \in [\omega_{D1}, \omega_{D2}] \quad (11)$$

where k_D is the disturbance rejection factor.

3. Noise rejection: For attenuating the measurement noise by at least $k_N \ll 1$ over the range of frequencies $[\omega_N, \infty]$ the required specification is:

$$\left| \frac{Y(j\omega)}{N(j\omega)} \right| \leq k_N, \quad \forall \omega \in [\omega_N, \infty] \quad (12)$$

This leads to the constraint on $L(s)$ as:

$$|L(j\omega)| \leq \frac{k_N}{1 + k_N}, \quad \forall \omega \in [\omega_N, \infty] \quad (13)$$

where k_N is the noise attenuation factor.

4. Robustness to the parametric uncertainties: All mathematical models of a physical system suffer from inaccuracies that result from non-exact measurements or from the general inability to apprehend all phenomena that are involved in the dynamics of the system under consideration. This misalliance between the model and the system is called an uncertainty. The robust controller takes into account these uncertainties which are specified as additive and multiplicative uncertainty [22] and expressed as:

$$\Delta_a(s) = P(s) - P_0(s) \quad (14)$$

$$\Delta_m(s) = \frac{P(s) - P_0(s)}{P_0(s)} \quad (15)$$

where $P_0(s)$ is the nominal process transfer function, $P(s)$ is every admissible process transfer function, $\Delta_a(s)$ and $\Delta_m(s)$ are the additive and multiplicative uncertainty functions respectively which are characterized by sufficiently large stable uncertainty weighing functions $W_a(s)$ and $W_m(s)$ such that for every $P(s)$:

$$\left\{ \begin{array}{l} |\Delta_a(j\omega)| \leq W_a(\omega) \\ |\Delta_m(j\omega)| \leq W_m(\omega) \end{array} \right\} \quad \forall \omega \quad (16)$$

The robustness of the controller is defined using robust stability theorem which is a special case of small gain theorem [22]. It states that:

- (a) If $|\Delta_m(j\omega)| \cdot |T_0(j\omega)| < 1$ for all $\omega \in \Re$ then the controller $C(s)$ internally stabilizes the perturbed plant $P(s)$.
- (b) The controller $C(s)$ provides robust stability against multiplicative uncertainty, for the plant set P if and only if

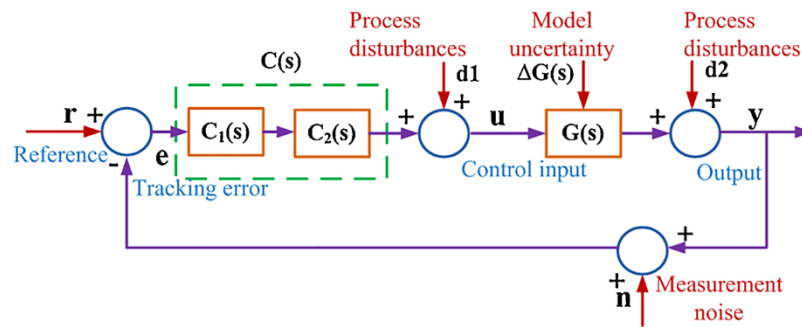


Fig. 2. Feedback system for DAB.

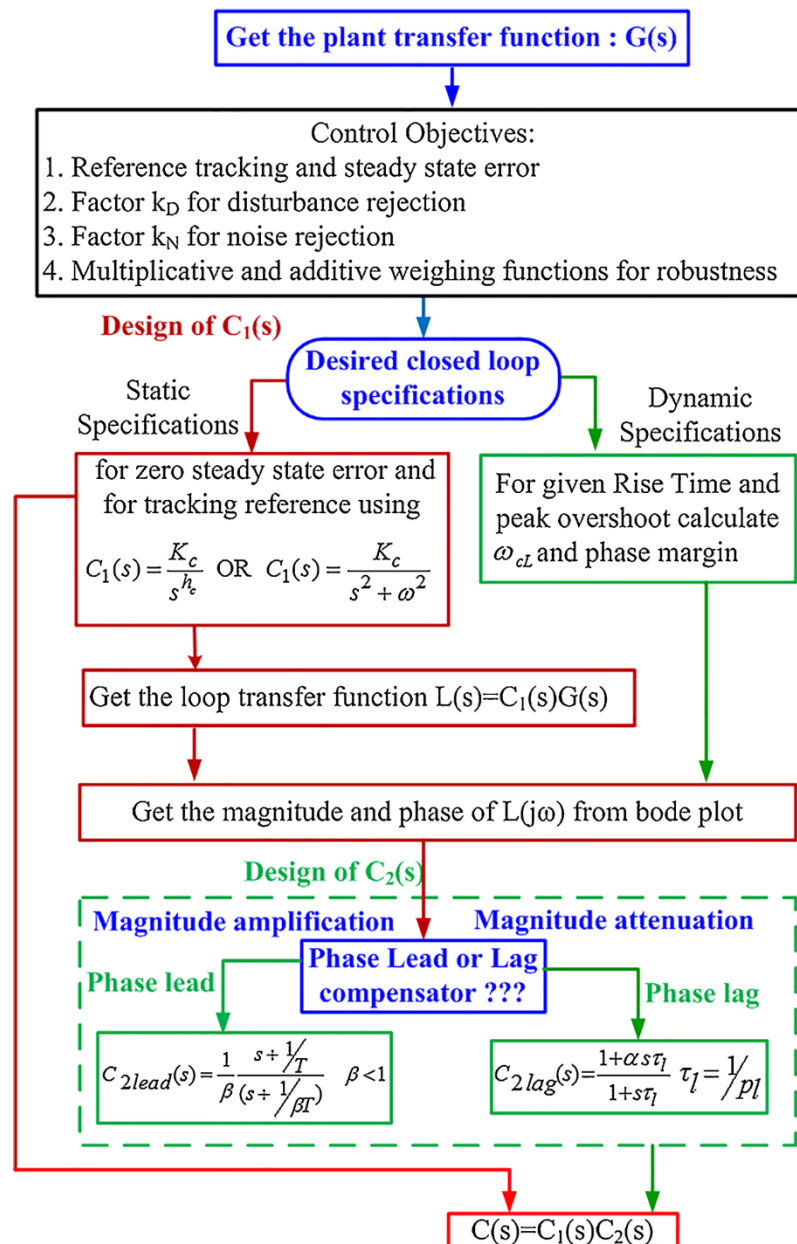


Fig. 3. Loop shaping control algorithm for DAB.

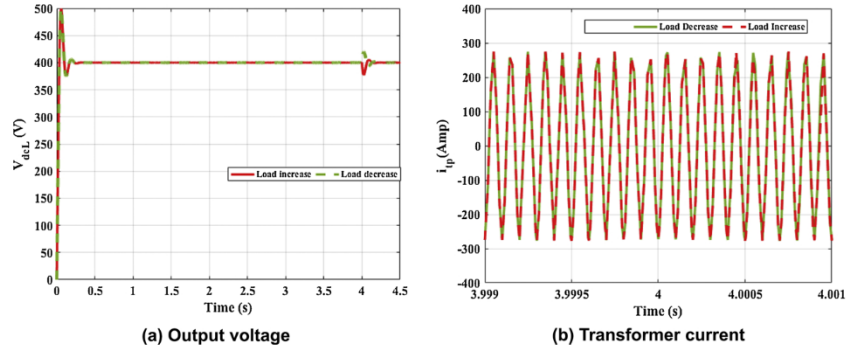


Fig. 4. Response of DAB with lag compensator for load disturbances.

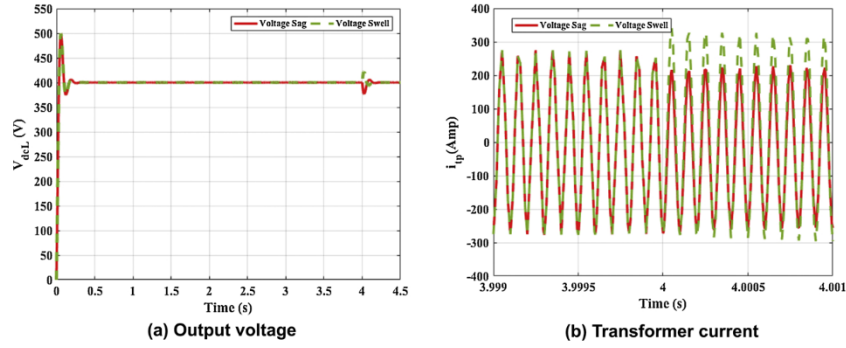


Fig. 5. Response of DAB with lag compensator for input voltage variations.

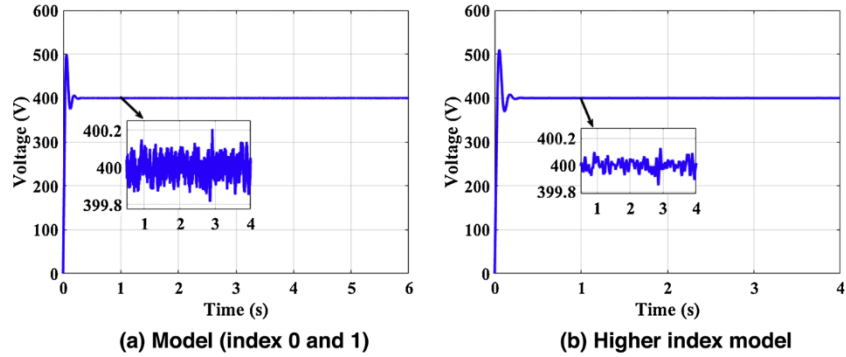


Fig. 6. Voltage response of DAB with lag compensator for measurement noise.

$\|W_m \cdot T_0\|_\infty < 1$, where T_0 is the complimentary sensitivity function.

3.2. Control algorithm

The standard form of the feedback system is depicted in Fig. 2.

The controller $C(s)$ which meets all the desired specifications is a cascade of two controllers, $C_1(s)$ which satisfies all the static specifications which include reference tracking, disturbance and noise rejection and $C_2(s)$ which satisfies all the dynamic specifications which include rise time and peak overshoot. The flow chart shown in Fig. 3, explains the algorithm for the design of controller $C(s) = C_1(s)C_2(s)$ using loop shaping technique.

The controller design demands transfer function of DAB which is obtained from the small signal model expressed by (19). The closed loop specifications for the controller design are:

1. Static specification: To maintain an output voltage of 400 V DC with zero steady state error, to reject the sinusoidal disturbances at the

input and attenuate the measurement noise with the disturbance rejection factor (k_D) and noise attenuation factor (k_N) as 0.1 respectively.

2. Dynamic performance: To attain a rise time of 0.045 seconds and the peak overshoot of 15%.

Since DC reference is to be tracked with zero steady state error, the static controller is an integral controller. For noise attenuation, the factor k_N is set as 0.1. This leads to the bound on the loop transfer function $L(s) = C_1(s)G(s)$ which is given by

$$|L(j\omega)| \leq \frac{k_N}{1 + k_N}, \quad \forall \omega \in [\omega_N, \infty] \quad (17)$$

as $L(j\omega)_{dB} \leq -20.8$ dB. Hence the controller gain is adjusted to satisfy this bound.

The system is subjected to an input sinusoidal disturbance of the form $d(t) = a \sin(2\pi ft)$ with $a = 0.1$ and $f = 0.1$. For good performance the error must remain below a maximum value e_{max} which in this case is considered as 0.01. The sensitivity function $S(s) = \frac{1}{1 + L(s)}$ must exhibit

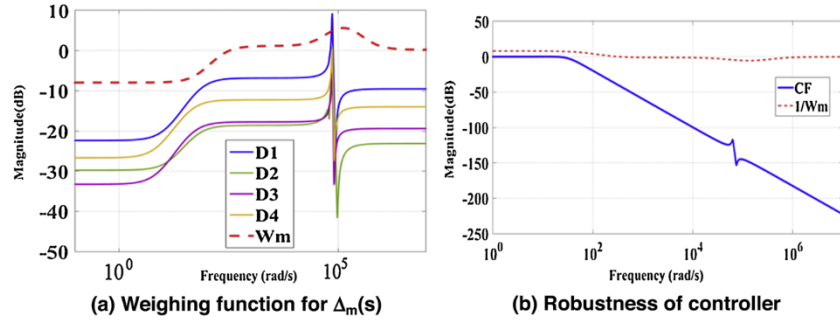


Fig. 7. Magnitude plots showing multiplicative uncertainty and robustness.

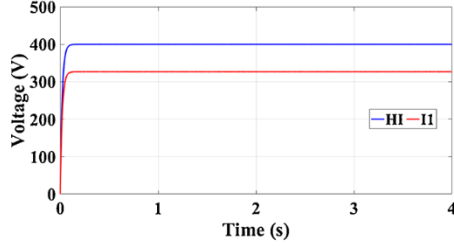


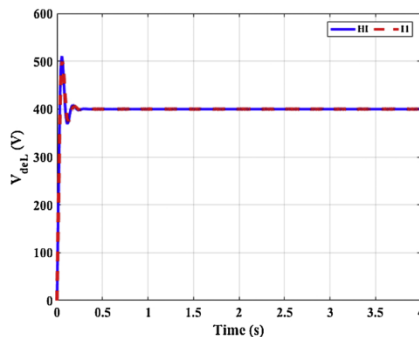
Fig. 8. Voltage response of DP based model (index 0 and 1) and higher index model.

rejection behaviour at the $\omega = 2\pi f$ which is possible only when loop transfer function has high gain at this frequency. Thus specification on error imposes bound on the loop transfer function as

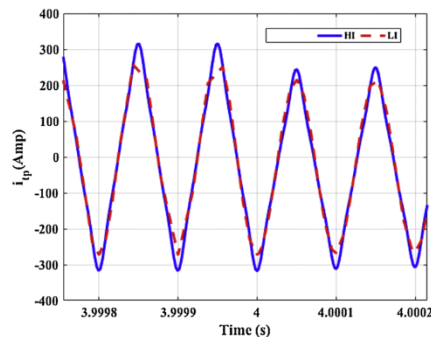
$$|L(j\omega)| > \frac{a}{e_{\max}} \quad (18)$$

The minimum required loop gain at the sinusoidal disturbance frequency is 20.2 dB. Hence the controller gain is adjusted to satisfy this bound in the low frequency region. The final controller gain is a trade off between the noise and disturbance rejection which can be selected only through trail and error. The mapping of above specifications on open loop leads to a cascade controller comprises of lag compensator with integral control. The performance of the designed controller is evaluated and analyzed in following sections.

$$\begin{bmatrix} \langle \Delta i_{tp} \rangle_1^R \\ \langle \Delta i_{tp} \rangle_1^I \\ \langle \Delta v_{dcl} \rangle_0 \end{bmatrix} = \begin{bmatrix} -\frac{R_L}{L_t} & \omega & \frac{2 \sin(\pi D_2)}{\pi L_t} \\ -\omega & -\frac{R_L}{L_t} & \frac{2 \cos(\pi D_2)}{\pi L_t} \\ -\frac{4 \sin(\pi D_2)}{\pi C_{dcl}} & -\frac{4 \cos(\pi D_2)}{\pi C_{dcl}} & -\frac{1}{R_L C_{dcl}} \end{bmatrix} \begin{bmatrix} \langle \Delta i_{tp} \rangle_1^R \\ \langle \Delta i_{tp} \rangle_1^I \\ \langle \Delta v_{dcl} \rangle_0 \end{bmatrix} + \begin{bmatrix} \frac{2V_{dcl0} \cos(\pi D_2)}{L_t} \\ \frac{-2V_{dcl0} \sin(\pi D_2)}{L_t} \\ \frac{4[I_{tp1} \sin(\pi D_2) - I_{tp1} R \cos(\pi D_2)]}{C_{dcl}} \end{bmatrix} [\Delta d_2] \quad (19)$$



(a) Output voltage



(b) Transformer current

Fig. 9. Comparison of DAB response considering higher index terms.

4. Performance evaluation

In this section, the closed loop performance of DAB is observed by developing its simulink model. The simulation parameters considered for the DAB are: Input voltage (V_{dch}) = 3800 V, output voltage (V_{dcl}) = 400 V, transformer resistance (R_t) = 0.4Ω, Load resistance (R_L) = 38Ω, transformer inductance (L_t) = 250 μH, LVDC link capacitor (C_{dcl}) = 540 μF and frequency = 10,000 Hz. The effectiveness of the controller is assessed under four cases: (i) Load and sinusoidal input disturbances (ii) Input voltage variations (iii) Measurement noise and (iv) Robustness.

4.1. Effect of load disturbances

Fig. 4 depicts the response of DAB against the load change. A step change of $\pm 10\%$ in the load resistance is introduced at $t = 4$ s. It is observed that the output voltage reaches to the reference value after a very short period transient.

4.2. Performance under input voltage variations

In this subsection, the performance of the controller is observed for step change in the input voltage. Fig. 5 shows the corresponding variations in output voltage and transformer current of DAB when $\pm 10\%$ variations is introduced at $t = 4$ s in the input voltage. The output voltage is maintained constant at 400 V.

4.3. Effect of measurement noise

Fig. 6 shows the effect of measurement noise on the output voltage. The random noise of variance 0.5 and sample time of 0.0001 is added in the output to check the effectiveness of the controller. It is observed that the noise in the output is attenuated as per the design specification of a factor of 0.1.

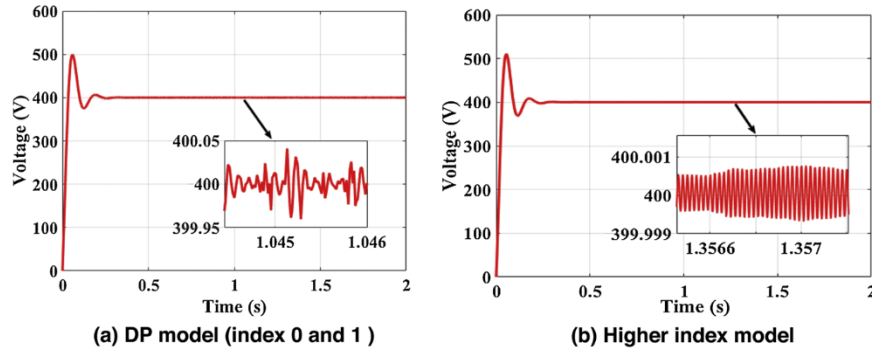


Fig. 10. Voltage response with sinusoidal input disturbances.

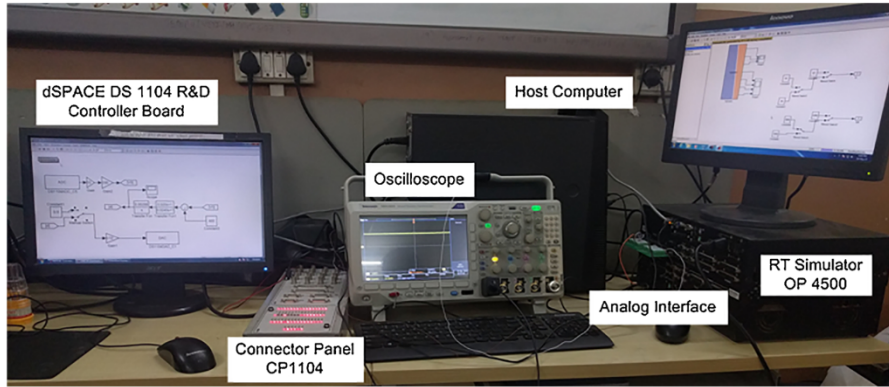


Fig. 11. Experimental setup for DAB.

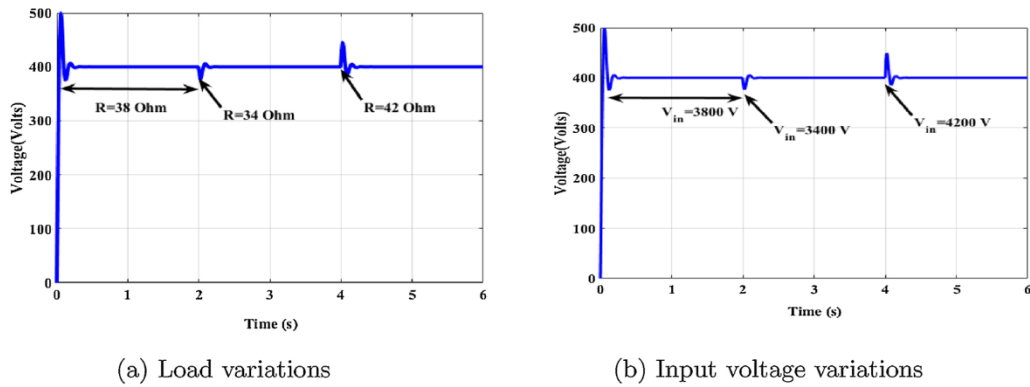


Fig. 12. HIL performance of DAB output voltage.

4.4. Robustness

The robustness of the controller is analyzed using small gain theorem, which implies that for robust control, the magnitude plot of complementary sensitivity function must lie below the plot of inverse of stable uncertainty weighting function ($W_m(j\omega)$) which is indicated by Fig. 7b. The robustness of the controllers is tested by introducing $\pm 25\%$ perturbations in the nominal value of parameters (i.e. inductance, capacitance and resistance). The bode plot of multiplicative uncertainty function and bounds shown in Fig. 7a indicates the robustness of the controller which is validated by the stable output voltage response under parametric variations.

5. Performance analysis

This section focuses on the comparative analysis of the DP based model of DAB with index 0 and 1 with higher index model of DAB. The analysis aims to link the enhanced performance with the appropriate selection of model.

5.1. Comparison of open loop responses

Fig. 8 shows the uncontrolled response of DP based model (index 0 and 1) with higher index model considering duty ratio as the exogenous signal. It is observed that the steady state error is more in the case of DP

based model (index 0 and 1) as compared to the higher index model. This concludes the effectiveness of the higher index model over DP based model (index 0 and 1). The simulation results are in line with the findings of [7].

5.2. Comparison of closed loop responses

The higher index model is a close approximation of detailed model. It has the advantage of fast simulation time. Fig. 9 shows the comparison of DP based higher index model with index 0 and 1. It is observed that the higher index model gives more insight in to the state variables and thus the stability is enhanced using the higher index model. Fig. 9b shows the transformer current with higher index terms.

To show the effect on the stability, the system is subjected to an input sinusoidal disturbance of the form $w(t) = a \sin(2\pi ft)$ where $a = 0.1$ and $f = 0.1$ Hz. The output voltage response is obtained for both the models i.e. model(0 and 1 index) and higher index model. Figs. 6 and 10 show that the attenuation of measurement noise as well as the rejection of the disturbances with the higher index model is improved as compared to the model approximated by 0 and 1 index. This proves the enhanced stability with higher index model.

6. Hardware-in-loop implementation

For real time simulations, RT-LAB environment of Opal-RT with RT toolbox and dSPACE Control desk is used for implementing the proposed system with controller. The experimental setup required for HIL interface is demonstrated in Fig. 11 where Opal-RT OP4500 replicates the DAB model and the dSPACE DS1104 mimic the controller [23].

OP4500 has 32-analog and 64-digital I/O channels to exchange data in real time and two 3.33 GHz cores for parallel computation. Red Hat LINUX operating system based targets are controlled through a Windows based host computer using a TCP/IP connection. The interfacing between the OP4500 and DS1104 is managed through fast Analog and Digital inputs and outputs of OP4500 and DAC and ADC of DS1104.

The performance of DAB under input voltage and load variations is verified via HIL simulation using Opal-RT and dSPACE. Fig. 12 depicts the real time response of DAB which is in close agreement with the MATLAB/simulink response.

7. Conclusions

This paper derives a higher index dynamic phasor model of DAB and analyzes its effects on the stability in comparison with the model approximated by dc and index 1 terms. The capabilities of the proposed robust control scheme based on the DP model of DAB are illustrated by meeting the performance objectives of voltage regulation, robustness, suppression of measurement noise and sinusoidal disturbances. The robustness of the compensator to the model uncertainties is evaluated using small gain theorem. Comparison of results with the conventional model advocates the advantages of the DP based model. The HIL

implementation of the system validates the design and the simulated results.

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