Evolving Magneto-electric Device Technologies

N. Sharma[1], J. P. Bird[2], Ch. Binek[3], P. A. Dowben[3], D. Nikonov[4], and A. Marshall[1]

[1] Department of Electrical Engineering, The Erik Johnson School of Engineering and Computer Science, University of Texas at Dallas, Richardson TX 75080
[2] Department of Electrical Engineering, 230 Davis Hall, University at Buffalo, Buffalo, NY, 14260, U.S.A.
[3] Department of Physics and Astronomy, Jorgensen Hall, University of Nebraska, Lincoln, NE, 68588, U.S.A.
[4] Intel Corp., MS RA3-252, 2501 NW 229th Avenue, Hillsboro, OR 97124 U.S.A.

Andrew.Marshall@utdallas.edu

Abstract

Here, several classes of magneto-electric devices, and their possible implementations as CMOS replacements, are discussed. We consider how these devices can provide considerable improvements in functionality over CMOS when employed in novel circuit architectures. In the context of the magneto-electric device technologies discussed here, we detail the expansion of benchmarking into some of the newer beyond-CMOS technologies. This has required circuit level simulations, using Cadence Spectre or Spice, and VerilogA based models of the ME-MTJ devices have been used for circuit validation. This has been done as part of a global effort to develop comparative benchmarking standards across logic families, even as new benchmarking methodologies are being developed, while maintaining the familiar CMOS benchmarks.

Keywords—Beyond-CMOS, CMOS, Spintronics, Magneto-Electric Magnetic Tunnel Junction (ME-MTJ); Magneto-Electric Field effect transistor (ME-FET), Logic, Full-adder, VerilogA

1. Introduction

For the last four decades, complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FET) [1] underpinned the breathtaking progress of microelectronics and information technology in general. This progress was enabled by the exponential scaling of transistor sizes according to the Moore's law [2]. Possible quantum limits to the scaling were comprehended [3], [4]. In addition to size limitations arising from quantum mechanics, this analysis showed an untenable value of power dissipated in computation (which grew exponentially with size). This understanding increased the urgency of finding and the research activity on beyond-CMOS devices [5, 6].

The initial expectation was to identify the beyond-CMOS device which would be a 'drop-in replacement' to CMOS, i.e., will have the same physical functionality and circuit structure ('microarchitecture'). Unfortunately, at early stages of research this discouraged beyond-CMOS devices too dissimilar from CMOS, as many such device concepts do not form good CMOS-like logic gates. It was then realized that such devices are subject by conceptually similar quantum limits as CMOS.

Attention was turned to less traditional devices based on other computing variables (i.e., physical quantities encoding the computing state): electric polarization, magnetization/spin, strain, etc. [7]. It was shown that spin based devices can be on a substantially different scaling curve, requiring lower switching energy *versus* size [4]. Such circuits, however, needed to be structured differently, e.g. generally based on majority gates. This type of circuits proved to be more compact and efficient than typical CMOS gates [7].

As a result, there is a wide variety of beyond-CMOS devices, which can be generally split into two distinct types: charge-based and non-charge-based. In general, charge based devices usually resemble CMOS, and are often both the easiest to understand, and the most likely to be closer to commercialization.

Charge based devices include:

(a) Tunnel FETs (TFET) [8] based on the effect of quantum tunneling [9]. They feature steep subthreshold voltage slopes (<60 mV/decade) but behave, from an electrical point of view, very much like CMOS. These devices required supply voltage is significantly lower than in CMOS, at about 0.25 to 0.5 V, and TFETs are projected to have higher drive current and smaller capacitance, which results in higher switching speed than CMOS at the same voltage. Many of these devices are III-V broken gap heterojunctions. TFETs are now close to a "plug-in" replacement for CMOS logic, requiring only minor design modifications compared to CMOS.

(b) Graphene [10-12], carbon nanotube, or 2D material devices [12-15], which can resemble CMOS. Some such devices are in fact tunnel FETs.

Non-Charge-based:

(c) Ferroelectric FETs [12, 16-19]. These are non-volatile devices due to a ferroelectric layer in the gate. Some such devices, such as negative-conductance FET [20], can be volatile, but use a ferroelectric layer to obtain a steeper subthreshold slope.

(d) Metal-insulator transition FETs [21].

(e) Piezoelectric FETs [22].

(d) Spintronic (aka nanomagnetic) devices [7, 23] operate on the principle of switching the magnetic (or spin polarization) in devices. This class of devices is promising for several reasons. It is non-volatile and thus can save in transitions to and from the power gated 'sleep' states of a chip [24]. That also means an easier integration with memory and compute-in-memory opportunity. Many spintronic devices have been proposed since early in the millennium. The point

here, though, is not to cover all the beyond-CMOS technologies. Because each design concept must be considered individually, even to cover all the spintronic device concepts is beyond the scope of this review. The most promising spintronic devices are based on magneto-electric phenomena [7, 25], both in terms of switching speed and switching energy. Specifically we will focus on Magneto-electric Magnetic Tunnel Junction (MEMTJ) [7, 19, 25-33], and Magneto-electric Field Effect Transistor (MEFET) [32, 34-37].

An early attempt to benchmark beyond-CMOS FETs (in this case, carbon nanotubes) was reported in 2006 [38], where the nanotubes were benchmarked and correlated to inverter delay performance. This early work predicted that the performance enhancement of carbon nanotube FETs over Si MOSFETs would not be as large as the prediction for the saturated current (I_D^{sat}) would suggest, due to non-ideal current-voltage characteristics. Benchmarking of circuits has been used since the earliest days of integrated circuits, and, with continued feature size reduction, has become more significant than ever. Digital benchmarking is the process of quantifying the relative performance, power and area of different integrated-circuit (IC) processes in performing a particular set of computing tasks. Mostly, for CMOS logic, this is the performance of inverter chains or ring oscillators, simple logic gates, such as NAND gates and NOR gates. Some slightly more complex circuits, such as adder circuits, are also compared (as are ALUs, or Arithmetic and Logic Units, although the ALU rarely gives improved results over the full-adder, and is more complex in its benchmarking set-up). CMOS technology has been benchmarked since it became a viable process option, over 45 years ago [38-40]. More recently cross correlation of digital circuitry and device characteristics have been refined [41, 42]. Benchmarking of analog and mixed signal circuits has also been important [43], though with analog the application has an impact on the performance needs, making benchmarking more complex.

The latest beyond-CMOS devices require benchmarking, to determine in what aspects they can be advantageous compared to conventional CMOS FETs. The issue of how to assess which of the numerous beyond-CMOS technology to pursue, remains profound. Its main difficulty stems from the need to compare existing and functional CMOS devices at the most scaled sizes to the potential of beyond-CMOS devices, if they can be successfully optimized and scaled to such sizes in the future. An attempt of benchmarking beyond-CMOS devices within the Nanoelectronic Research Initiative (NRI) of the Semiconductor Research Corporation (SRC) was made by Bernstein et al. [5]. The selected several benchmarking circuits for digital logic and used the device parameters provided by their proponents. Torres et al. [44] also added to the body of work on benchmarking beyond-CMOS devices. More recently, Nikonov and Young [7, 23, 45] created a theoretical framework to compare circuit performance of a wide range of beyond-CMOS devices in a transparent and uniform manner, i.e. with the same approach and assumptions made about each option. Later benchmarking of beyond-CMOS devices using circuit simulators like Spice and Spectre have been pursued, improving accuracy significantly. We illustrate the value of this sort of benchmarking below, by comparing one class of magneto-electric devices, the Magneto-electric Magnetic Tunnel Junction (MEMTJ) [7, 19, 25-33], to another class, the Magneto-electric Field Effect Transistor (MEFET), in the context of possible logic circuit implementations.

2. Background

Magnetoelectric materials, where a net magnetic moment is induced by an electric field, may be key to voltage controlled spintronic devices of many types, most notably (as discussed below) to spintronic devices that do not exploit ferromagnetism. The starting point for these devices is the magneto-electric effect, where an applied electric field E results in the induction of net

magnetization M [46]. The magnetoelectric effect, and notably the linear magnetoelectric effect, is derived systematically from a series expansion of the density of the Gibbs free energy. From the free energy one obtains relationships for polarization and magnetization [32, 46-50], where electric field and magnetization are coupled by a magnetoelectric constant (α_{ij}) so that $\alpha_{ij} = \partial P_i / \partial H_j = \partial \mu_o M_i / \partial E_j$. In the context of the magneto-electric tunnel junction devices discussed here, a large magnetoelectric susceptibility (α_{ij}) is desirable [32, 46-48, 50], so that a small applied electric field results in a large magnetization response. In fact, the transistor devices, described here, actually function well because of the highly spin polarized nature of the boundary (surface), in the single magneto-electric antiferromagnetic domain state. This high spin boundary polarization was predicted independently by Andreev [51] and Belashchenko [52] and has been experimentally confirmed, for magnetoelectric chromia, by a wide variety of techniques [53-58].

The linear magnetoelectric response for isothermal electric control of exchange bias is hampered by the small value of the linear magnetoelectric effect. The actual value of the magnetoelectric constant (α_{ij}) is on the scale of 4.13 ps/m, in the case of the inorganic antiferromagnetic magnetoelectric Cr_2O_3 [59]. The consequence of the interface polarization, which reverses with the antiferromagnetic order parameter of the magnetoelectric is actually the key to the operation of a magneto-electric device. But this reversal domain (and successful exchange bias control) is clearly a non-linear effect [53, 55, 60, 61], as seen in Figure 1. As many have found, isothermal switching between the single domain states is achieved when the magnitude of the product $E\,H$, for an electric field, E, and a symmetry breaking magnetic field, H, overcomes a critical threshold.

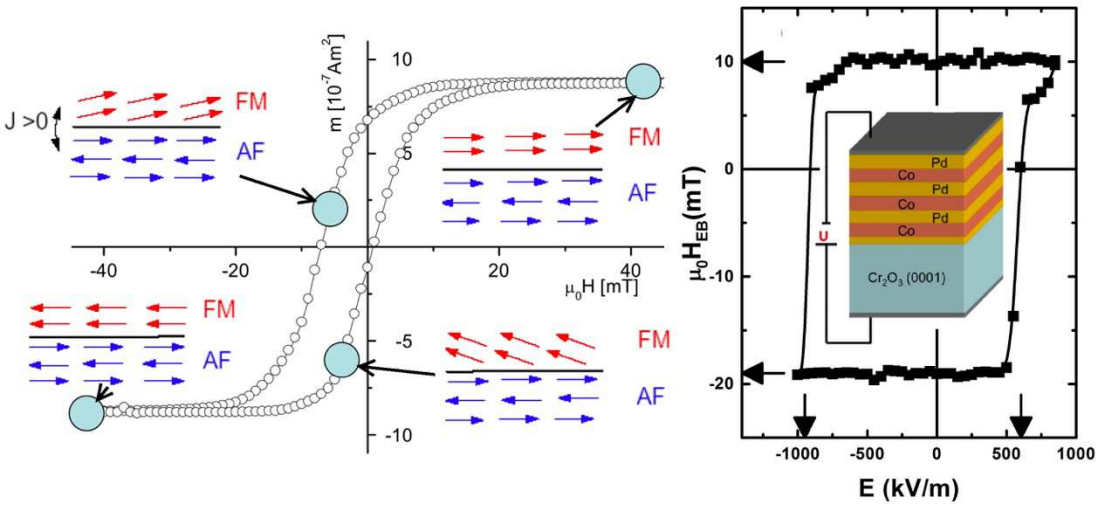


Figure 1. Hysteresis loop of the exchange bias, $\mu_0 H_{EB}$, seen with a pinned CoPd multilayer thin film on chromia (Cr_2O_3), measured at T = 303 K (on the right). Exchange bias, of a magnetization curve between a ferromagnet and antiferromagnet, is schematically shown at the left. Adapted from [55, 60].

The magneto-electric tunnel junctions described below (vide infra) depend on exploiting the exchange bias between a ferromagnet and the antiferromagnetic magneto-electric, which is typically also very dielectric. Exchange bias is a coupling phenomenon at magnetic interfaces, especially antiferromagnetic-ferromagnetic interfaces, and is typically evident when a shift of the ferromagnetic hysteresis loop occurs (as indicated in Figure 1) along the magnetic-field axis. The magnitude of the exchange bias is quantified by the $\mu_0 H_{EB}$ shift [53, 62], as indicated in Figure 1.

It should be noted that the magneto-electric materials, a design parameter in the devices described here, is actually not essential for magneto-electric effects. Many multiferroics (ferromagnetic-ferroelectric materials combinations, for example), also exhibit magneto electric phenomena [48], that is say there is a magnetic response to an applied electric field, as do dielectric systems with large spin-orbit coupling [19], and ferrimagnets.

3. Some Basic Magneto-electric Devices

An early logic device, built around magneto-electric effects, and the exchange bias between the dielectric antiferromagnetic magneto-electric and a ferromagnetic layer, was the magnetic tunnel junction structure [26, 28]. This consists of two ferromagnetic (FM) layers separated by a non-magnetic insulator where the device resistance is determined by the relative orientation of the magnetization of the two FM layers. The basic MEMTJ is a three terminal voltage controlled device, which has the potential for both logic and memory. The voltage controlled switching, of the magneto-electric boundary layer, is non-volatile and allows for low power operation. The fixed and free magnetic layers are separated by a thin tunnel dielectric (such as MgO), as a tunneling barrier, between the two ferromagnetic layers [38]. The lower FM layer (in Figure 2) has its magnetic state pinned by the exchange bias generated in the underlying (non-magneto-electric) antiferromagnet (AFM). This is the "fixed" electrode. The upper ("free") FM is capped with a dielectric magneto-electric such as chromia, which is exchange biased to the free FM layer, thus responsible for achieving switching functionality.

The principle innovative feature of this device is control of the magnetic state of the free ferromagnetic layer by means of the exchange bias produced by the magneto-electric's boundary magnetization. The magnetization of the free layer is exchange coupled to the Cr_2O_3 (or other magneto-electric) interface magnetization (Figure 2). We change the direction of this magnetization, by applying a suitable electric field in (~1 V/μm in chromia [15, 63]), in the reverse direction, while maintaining a fixed magnetic field. Hence a positive electric field will orient the spins in one direction while a negative field will induce the opposite spin [64]. A bias voltage applied across a magneto-electric layer, like chromia Cr_2O_3, reverses the interface magnetization, which in turn switches the magnetization of the free layer [32, 53, 54]. A lot of thought has been given to how this might be implemented in logic elements [30, 33, 65-68], and to some extent benchmarked against CMOS [31, 66]. The disadvantage is that while much faster than many spintronic devices, there is a long delay time in device operation, due to the slow speed of switching a ferromagnet.

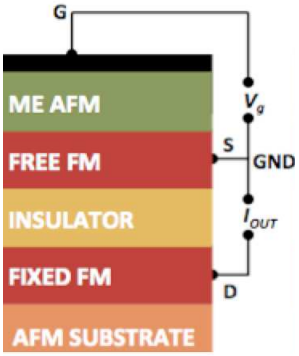


Figure 2. The Magneto-electric Magnetic Tunnel Junction (MEMTJ) device is a voltage-controlled magnetic tunnel junction where free magnetic layer magnetization is controlled by a magnetoelectric interface, separating the read and write aspects of the device. From [15, 29-31, 65, 66].

Other magneto-electric devices, like the composite–input magnetoelectric–based logic technology (CoMET) [69] have lower bounds on their switching speed. CoMET devices are limited by the switching speed of the ferroelectric and domain wall motion. The basis of these devices is that an input switches a ferroelectric material, in contact with a ferromagnet with in-plane magnetic anisotropy, placed on top of an intra-gate ferromagnet interconnect with perpendicular magnetic anisotropy. The input voltage nucleates a domain wall while a current is used to drive the domain wall to the output end of the device. A similar magneto-electric device structure, but now using spin-orbit coupling, has also been proposed [70]. There is a concern that both these device concepts will have long delay times, due to the slow switching speed of the ferromagnetic layer, and in the case of the CoMET device, the additional complications of the slow speed of ferromagnetic domain wall propagation. While using higher currents to drive the domain wall at faster velocities might be possible, this will come at an energy cost. Also using spin orbit coupling, but now explicitly also using a magneto-electric layer for electrical control of exchange bias of a laterally scaled spin valve is the nonvolatile magneto-electric spin-orbit (MESO) logic [71], but the delay time is still limited by the switching speed of the ferromagnetic layer.

A non-magnetic Hall bar on top of magneto-electric chromia has now been demonstrated as a readout mechanism for a memory state via the anomalous Hall effect [56, 57, 61]. While the overall Hall voltage ratio is very small, at least so far for such devices, these prototype elements demonstrate that magneto-electric devices can be constructed so as to fabricate a spintronics device without any ferromagnet. Overall, this indicates that spintronic devices, unencumbered by the long delay times associated with switching a ferromagnetic layer, can achieve switching speeds similar to CMOS, at a device dimension of 15 nm x 15 nm [72]. None of these devices really address the practical issues of how to realize on/off current ratios that are large enough for practical applications, and the devices must also be optimized to be able to cascade device elements to be able to generate complex logic functions [67, 73, 74].

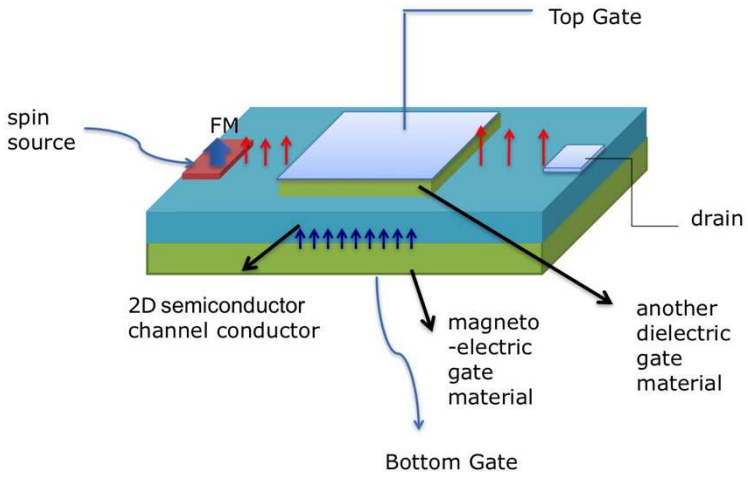


Figure 3. The basic top gated magneto-electric spin-FET (MEFET) with a ferromagnetic (FM) source and drain. The narrow channel conductor/semiconductor is any suitable material (e.g: graphene, InP, GaSb, PbS, MoS_2, WS_2, $MoSe_2$, WSe_2, etc.). Adapted from [30, 32].

More recently, attention [19, 32, 36, 37, 68, 75-77], has shifted to the magneto-electric spin field effect transistor (MEFET). The magneto-electric field effect transistor (MEFET) is, in physical appearance similar to a conventional CMOS device. Magnetization switching is not required, although magnetic electrodes at the source and drain could improve device fidelity, where the spin current along the semiconductor channel depends on the direction of orientation of the chromia spin vectors, the channel spin vectors are either oriented in the 'up' or 'down' direction. The MEFET is available in several versions, however, the simplest option is a single source, single drain version as shown in Figure 3. This is a 4-terminal device with source, drain, gate and back gate terminals [78]. There are generally two dielectrics in these device, one of which being chromia while the other is a common insulator such as alumina (Figures 3 and 4). Magneto-electric transistor schemes are based on polarization of the semiconductor channel, by the boundary polarization of the magneto-electric gate, layer through the proximity effect [19].

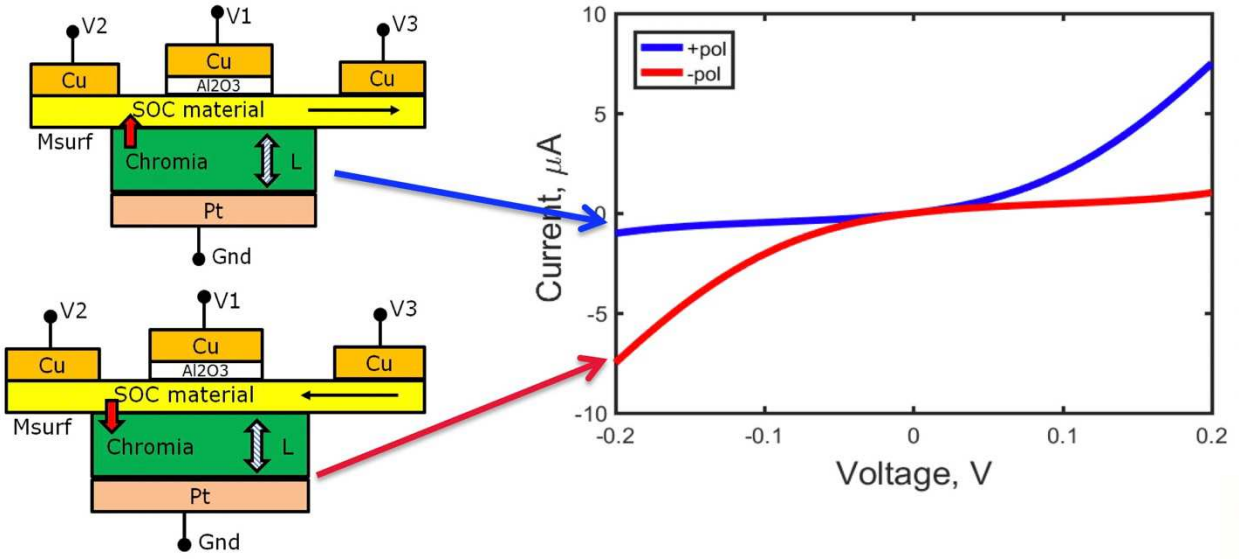


Figure 4. The cross-sectional views show the scheme of anti-ferromagnet spin orbit read (AFSOR) logic. upper) The state with positive V1 applied and the surface or interface magnetization of the magneto-electric gate M_{surf} pointing up. lower) The state with negative V1 applied and surface magnetization M_{surf} pointing down. The graph shows source to drain current versus voltage (adapted from [19, 37]).

The advantage to the MEFET is that such schemes avoid the complexity and detrimental switching energetics associated with magneto-electric exchange-coupled ferromagnetic devices, instead being based solely on the switching of a magneto-electric. As a result, switching speed is limited only by the switching dynamics of that magneto-electric material of the voltage controlled spintronic devices [56-58, 79]. With coherent rotation, as the domain switching mechanism, the switching speed might be as fast as 5 to 6 ps [79]. Moreover, these magneto-electric devices promise to provide a unique field effect spin transistor (spin-FET)-based interface for input/output of other novel computational devices. This is spintronics without a ferromagnet, with faster write speeds (<20 ps/full-adder) [68, 79], at a lower cost in energy (<20 aJ/full-adder) [68], greater temperature stability (operational to 400 K or more), and scalability, requiring far fewer device elements (transistor equivalents) than CMOS, as will be discussed here. These magneto-electric field effect transistors (ME-FET) do differ from the conventional field transistor in that the ME-FET must be both top and bottom gated, son the result is that this is a 4, not 3 terminal transistor [36, 68, 77]. This device could, in principle, operate at applied gate voltages around 100 mV,

possesses inherent memory due to the non-volatile AFM ordering of the ME and has a sharp turn-on voltage [38, 63]. This device also has a potential on-off ratio of ~ 10^6 [64], which is comparable to CMOS and advantageous for implementing logic functions.

With spin orbit coupling, the magneto-electric boundary polarization can have an exchange interaction with a semiconductor channel and a spin current can be generated, especially if the semiconductor channel is very thin, i.e. a 2D material [19]. If the semiconductor channel retains large spin orbit coupling, then the spin current, mediated by the gate boundary polarization, may be enhanced and, to some extent, topologically protected. The latter implies that each spin current has a preferred direction, as indicated in Figure 4. Exploiting this phenomena, the anti-ferromagnet spin-orbit read (AFSOR) logic device structure (Figure 4) has interesting advantages: the potential for high and sharp voltage 'turn-on'; inherent non-volatility of magnetic state variables; potentially large on/off ratios; and multistate logic and memory applications. The design will provide reliable room-temperature operation with large on/off ratios (>10^7), well beyond that achievable using magnetic tunnel junctions [19, 77].

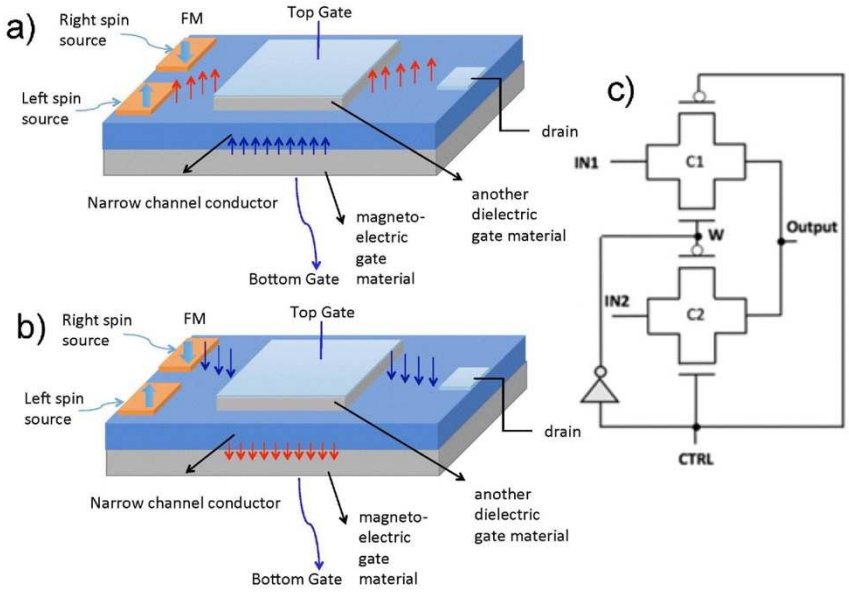


Figure 5. The nonvolatile ME spinFET multiplexer (spin-MUX), can also be constructed with ferromagnetic source contacts. The thin channel conductor/semiconductor is polarized (a) up or (b) down. The CMOS equivalent is schematically indicated in (c). Adapted from [19, 37].

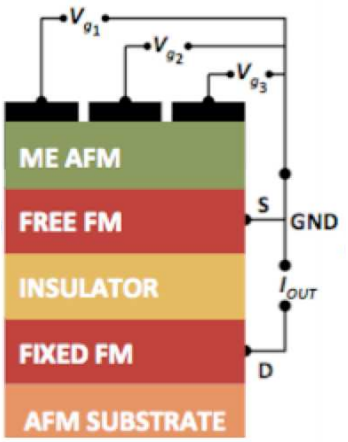
A variant of Figure 4, where inversion symmetry is not as strictly broken, results in a nonvolatile spintronic version of multiplexer (MUX) logic [65, 78]. The magneto-electric spin-FET multiplexer (Figure 5) also exploits the modulation of the spin-orbit splitting of the electronic bands of the semiconductor channel through a "proximity" magnetic field derived from a voltage-controlled magneto-electric material. Here, by using semiconductor channels with large spin-orbit coupling, we obtain a transverse spin Hall current, as well as a spin current overall. Depending on the magnitude of the effective magnetic field in the narrow channel, two different operational regimes are expected. Like the AFSOR magneto-electric spin FET, the magneto-electric spin-FET multiplexer in Figure 5 uses spin-orbit coupling in the channel to modulate spin polarization and hence the conductance (by spin) of the device [78]. There is a source-drain voltage and current difference, between the two FM source contacts, due to the spin-Hall effect when spin-orbit

coupling is present. This output voltage can be modulated by the gate or gates, which influences the spin-orbit interaction in the channel. To increase the spin fidelity of current injection at the source end, a suitable tunnel junction layer could be added between the magnetic source and the 2D semiconductor channel [19, 77]. This, however, is expected to result in a diminished source-drain currents.

The devices described above are by no means all the magnetoelectric devices that have been considered. Indeed there are multiple variations just on the devices described here. These variations on these magneto-electric devices do much to facilitate the implementation of these magneto-electric devices as CMOS "plug-in" replacement logic, as discussed below. The basic devices that can be created from CMOS are the inverter, NAND and NOR gates. Secondary and more complex gates can all be created from these. The basic devices [27, 28, 30, 31, 65, 66, 74, 80, 81], that can be created from the ME-MTJ are the inverter/buffer, majority/minority AND/NAND, OR/NOR and XNOR gates. In CMOS the buffer, majority, minority, AND, OR and XNOR are secondary gates, requiring more complex designs or multiple gates. The MEFET also can be made manifest in a number basic devices that include: Inverter/Buffer, Nand/And, Mux/Demux, and XOR. This large library of basic gates [19, 27-32, 37, 65, 66, 74, 80, 81], is common to many beyond-CMOS technologies, and opens up an avenue for beyond-CMOS devices, for reduced component count circuits, and relatively faster performance circuits. In addition, since area is thus also lower than CMOS, interconnect delay is reduced, and logic density is improved.

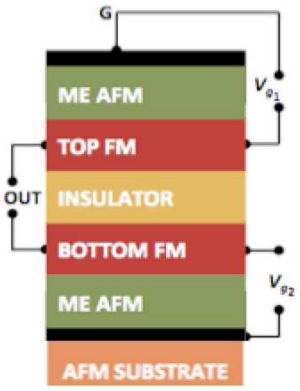
4. Logic with Magnetic Tunnel Junction Magneto-Electric Devices

The Magneto-Electric Magnetic Tunnel Junction (MEMTJ), of Figure 2, has been studied for a number of years [27, 28, 30, 31, 65, 66, 74, 80], 81]. The logic state is represented by the relative orientation of the spin vectors in two ferromagnetic layers (FM). In addition to the schematic configuration for the MEMTJ shown in Fig. 2, which can form both an inverter and a buffer device, there are two other basic gates that can be made with the technology. These are the majority gate (Figure 6) [30, 31, 65, 66], and the exclusive NOR (XNOR) gate (Figure 7) [30, 31, 65, 66]. It is interesting to note that for CMOS the Majority gate and XOR/XNOR are complex gates, requiring the use of several NAND or NOR gates. The majority gate is generated by splitting the gate of the inverter MEMTJ into three. The AFM layer is engineered so that only when at least two of the three split gates are at a “high” input voltage will the output switch the antiferromagnetic domain state, based on the principle, that there is a minimum antiferromagnetic domain state dimension, and the device is smaller than the minimum antiferromagnetic domain state dimension, thought to be about 3 μm [54]. The XNOR version of the ME-MTJ is constructed by modifying the MTJ geometry as indicated in Fig. 3, which shows that the main modification has been to replace the passive antiferromagnetic layer that pins the fixed FM in Fig. 1 with a separate ME layer. The device therefore has two magneto-electric layers, the exchange bias generated by each of which is determined by the separate voltages Vg1 & Vg2. In the case where the polarity of these two inputs is opposite (i.e. “1” & “0” or “0” & “1”), the magnetization of the two FMs will be parallel, leading to low MTJ resistance and an output state of “0”. For similar inputs (i.e. “0” & “0” or “1” & “1”), however, the opposite holds; the two FMs will be antiparallel alignment and the MTJ resistance will be high (logic level “1”). Overall, this is simply the XNOR function (see the truth table in Fig. 3).



A	B	C	F	
0	0	0	0	AND Logic A fixed to 0
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	OR logic A fixed to 1
1	0	1	1	
1	1	0	1	
1	1	1	1	

Figure 6. MEMTJ based majority gate and truth table. Adapted from [30, 31, 65, 66].



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Figure 7. MEMTJ based XNOR (and truth table). Adapted from [30, 65, 66].

Applying the optimum circuit for benchmarking achieves a significant performance improvement, and in some cases can make what would appear to be a non-competitive technology viable. While benchmarking can be done on simple gates, a true comparative performance is not achieved until a more representative circuit is defined. The smallest digital circuit that typically covers both CMOS and beyond-CMOS technologies is the full-adder. The full-adder has many applications, particularly in microprocessors and arithmetic and logic units. The inputs to the full-adder are a carry-in, from the prior adder stage, and two digital inputs, A and B. The full-adder has two outputs, a sum and a carry-out. If at least two of the three inputs are a logic level '1', then the carry-out will be a '1'. If an odd number of the three inputs are a logic level '1', then the sum output will be a logic level '1'. Usually for the purposes of simulation, it is assumed that the adder will be a 32-bit adder, allowing two 32-bit words to be added.

The conventional full-adder can be designed in two ways in CMOS: The first involves using basic logic gates, typically NAND gates. Since each NAND gate consists of four transistors (two NMOS and two PMOS), the NAND based adder requires 36 transistors. Typically, however, a circuit used as frequently as a full-adder is designed at the transistor level. This only requires 28 components, so is around 20% smaller in area. In principle, this implementation could be a few

percent faster than CMOS if the magnetization reversal is pushed to the limit and the device is reduced to the size limit of 10 nm or so, and consumes 20-30% lower leakage current than one based just on NAND gates. The first attempts to simulate a full-adder using the MEMTJ technology used just two components from the MEMTJ library, the MEMTJ inverter and majority/minority gates [29, 30]. This showed capability, but is not efficient. To make a NAND gate from the MEMTJ majority gate, one of the majority gate inputs must be grounded, and the remaining two inputs then act as either an AND or NAND, depending the magnetization orientation of the fixed ferromagnet (FM) in the on the MEMTJ device (Figure 8). By designing the full-adder, to make optimal use of the MEMTJ device characteristics, this can be reduced to just five components (Figure 8), three majority gates and two inverters [30, 65], reducing the area to about 55% of the NAND-equivalent version, and reducing the input to output delay time by over 40%. In addition, if only the Carry-in to Carry-out is considered, the delay reduces to just 50% of the NAND equivalent circuit.

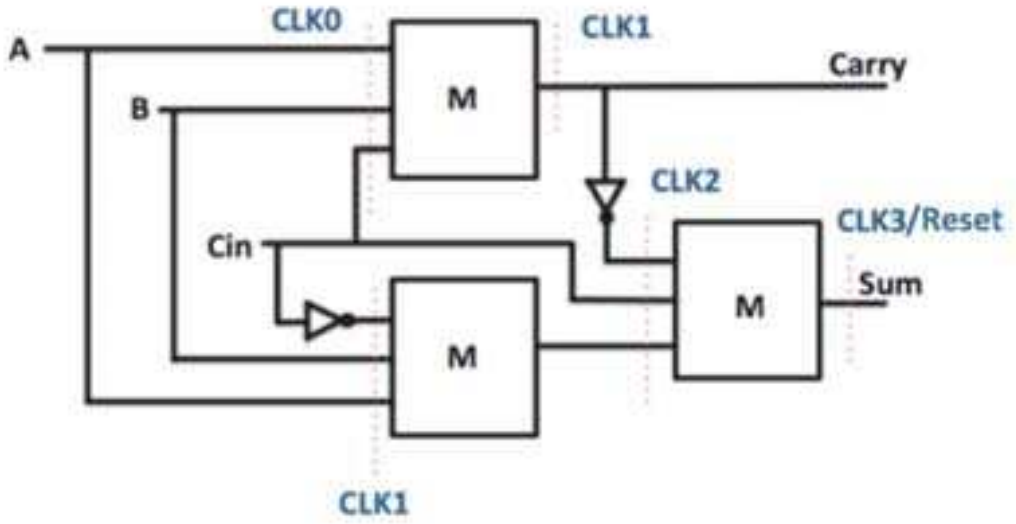


Figure 8. The MEMTJ full-adder using majority gates and inverters. Here, the square, with the letter 'M' within in this circuit schematic, indicates the magnet-electric majority gate tunnel junction devices of Figure 6. Adapted from [30, 31, 65].

The MEMTJ based full-adder described above is improved further when the XNOR version of the MEFET (Figure 7) is introduced into the circuit [65]. The addition of this component enables the very efficient one majority gate and two XNOR devices circuit shown in Figure 9. This further reduces area (the circuit footprint) by an additional 15%, and also leakage is reduced by a similar amount. Carry-in to Carry-out is approximately the same, though there is slightly less interconnect, but the signal path through to the Q or sum output is reduced from 3 gates in the circuit of Figure 8 to just two gates in the circuit of Figure 9.

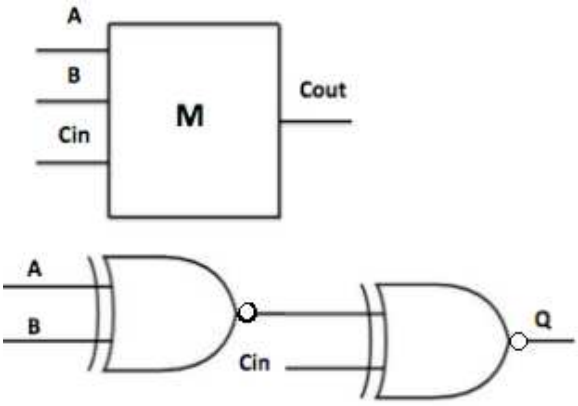


Figure 9. MEMTJ full-adder using majority gates and Exclusive NOR gates.

5. Logic Using MEFET Technology

As noted above, the magneto-electric field effect transistor (MEFET) [19, 30, 32, 37], is in physical appearance, similar to a conventional CMOS device. It is a 4-terminal device with source ("S"), drain ("D"), gate ("G") and back gate ("BG") terminals, but the current flow direction is mediated if spin-orbit coupling is exploited, as in Figure 4. The current is injected into the channel through the source terminal and polarized by the chromia, resulting in a spin polarized current at the drain. The "BG" terminal is grounded and the input voltage is applied across the "G" and "BG" terminals to create a vertical field across the chromia layer and to align its spin vectors either along +x or –x axis, depending on the polarity of voltage applied. The thin channel conductor/semiconductor is polarized either up or down. Both 'up' and 'down' spins can be detected at the drain, but, because of the topological protection of the spin current, two types of transistor operations can be defined depending on the directions of the current flow of Figure 4, as schematically noted in Figure 10. The state of the device is read using a clocked CMOS active pull up device. Clocking of this component reduces leakage dramatically [7, 68].

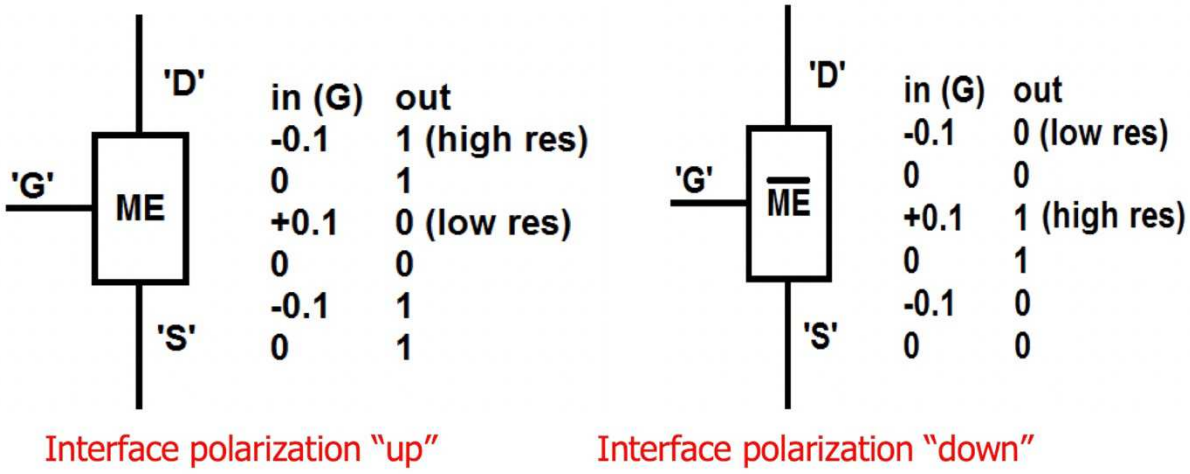


Figure 10. A schematic representation of the two operational states of the anti-ferromagnet spin orbit read (AFSOR) logic device of Figure 4. The notation in this schematic will be used in much of the discussion that follows.

Implementation is readily achieved with some basic driving transistors, to create inverter operation (Figure 11) and minority gate operations (Figure 12).

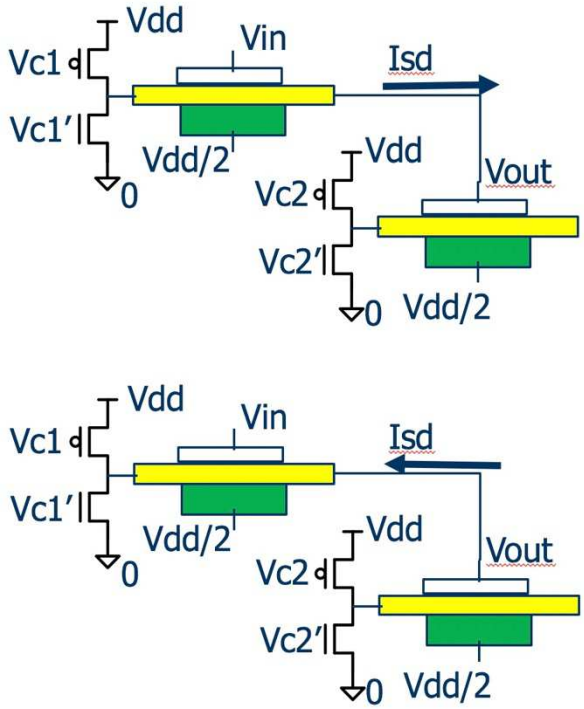


Figure 11. A schematic of basic inverter operations with MEFETs of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4, and driving transistors, as indicated. If Vc1=1, Vc1'=0, the circuit is disabled, while if Vc1=0, Vc1'=1, then the circuit is operating. If Vin=0, Isd>0, Vout rises to Vdd, while if Vin=Vdd, Isd<0, Vout falls to 0.

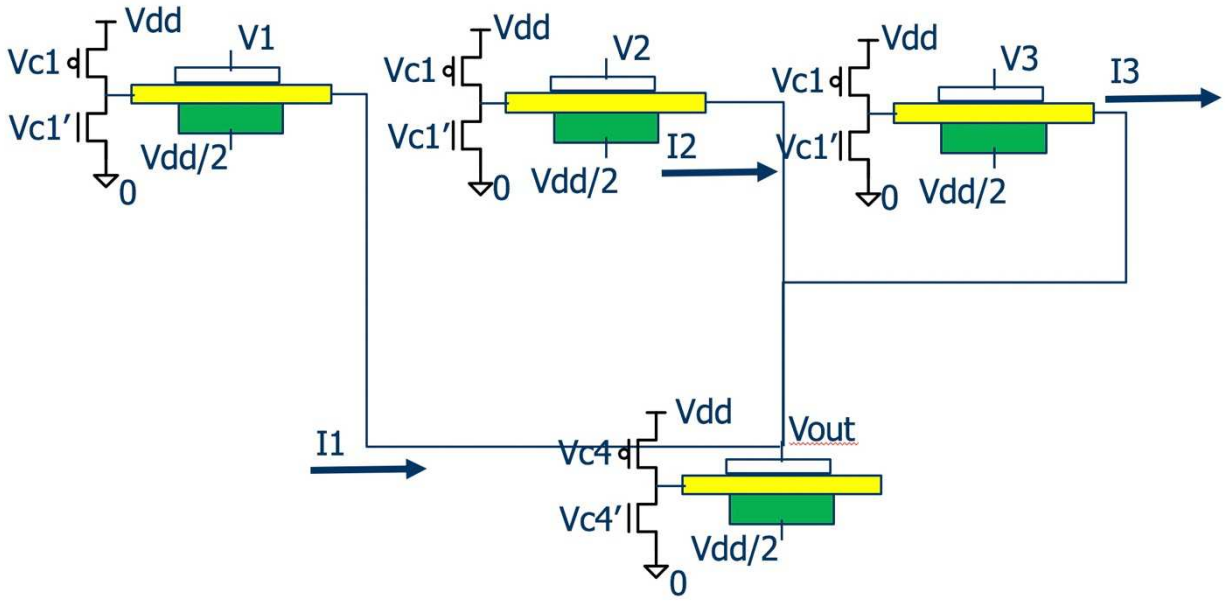


Figure 12. A schematic of basic minority gate operations with MEFETs of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4, and driving transistors, as indicated.

The MEFET of Figure 4 does allow for even more compact gates, however. For example, one might start out with the XNOR gate, as in Figure 13.

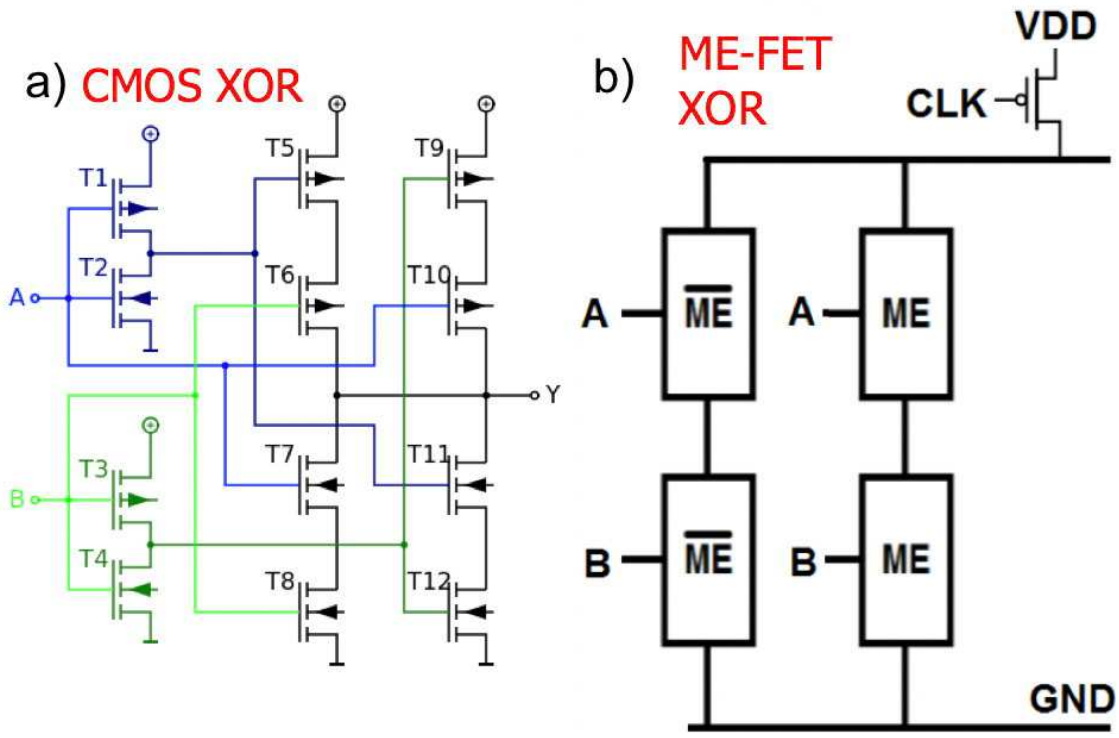


Figure 13. A schematic of basic XNOR gate operations with (a) CMOS and (b) using the MEFETs of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4. The MEFET state, determining current direction, is as in Figure 10.

Yet this simple XNOR gate can be simplified further by creating a MEFET device, of the style of Figure 4, but where the chromia gate can be polarized in series either up or down, as in Figure 14, to make a two input device.

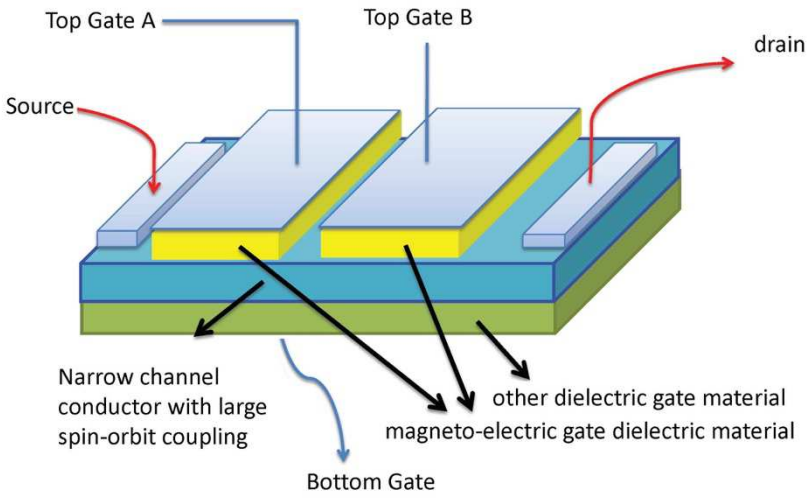


Figure 14. The scheme for a split gate MEFET based on the anti-ferromagnet spin orbit read (AFSOR) of Figure 4, for more compact logic gate circuits.

The configuration of Figure 14, i.e. the split gate MEFET, can be used for the XNOR. This improved device reduces the component count of the XNOR to just two devices, including the pull-up, as seen in Figure 15.

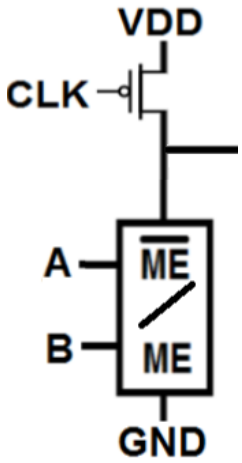


Figure 15. A schematic of basic XNOR gate operations using the MEFETs of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 14. The MEFET state, determining current direction, is as in Figure 10.

The silicon CMOS majority gate typically requires 13 components. The MEFET majority gate, anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4, requires, including clocking, only 6 components, as seen in Figure 16. This represents an area improvement of over 50%, assuming similar size transistors. This is equivalent to greater than one process node.

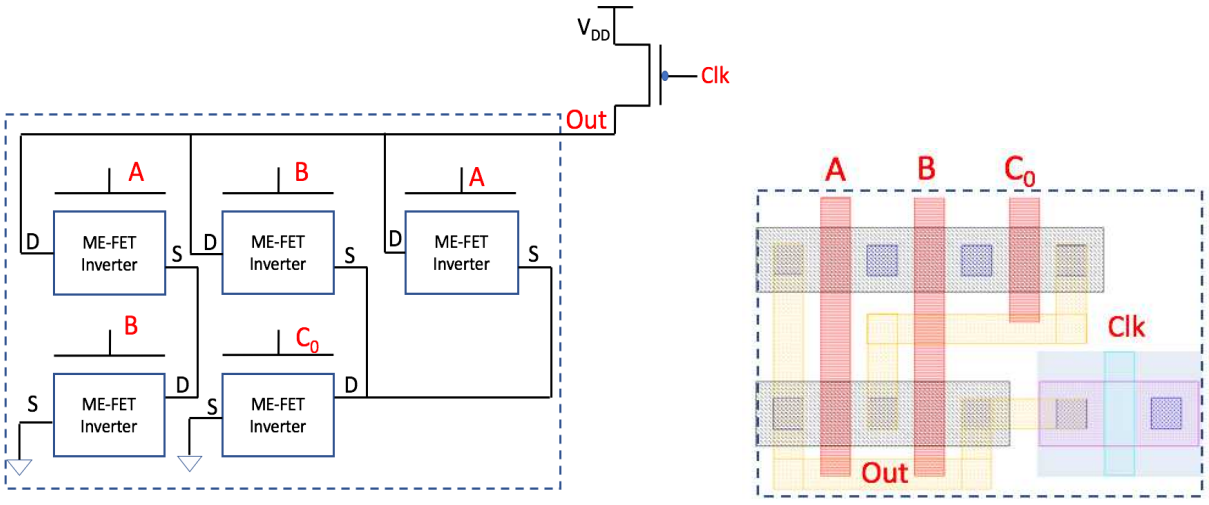
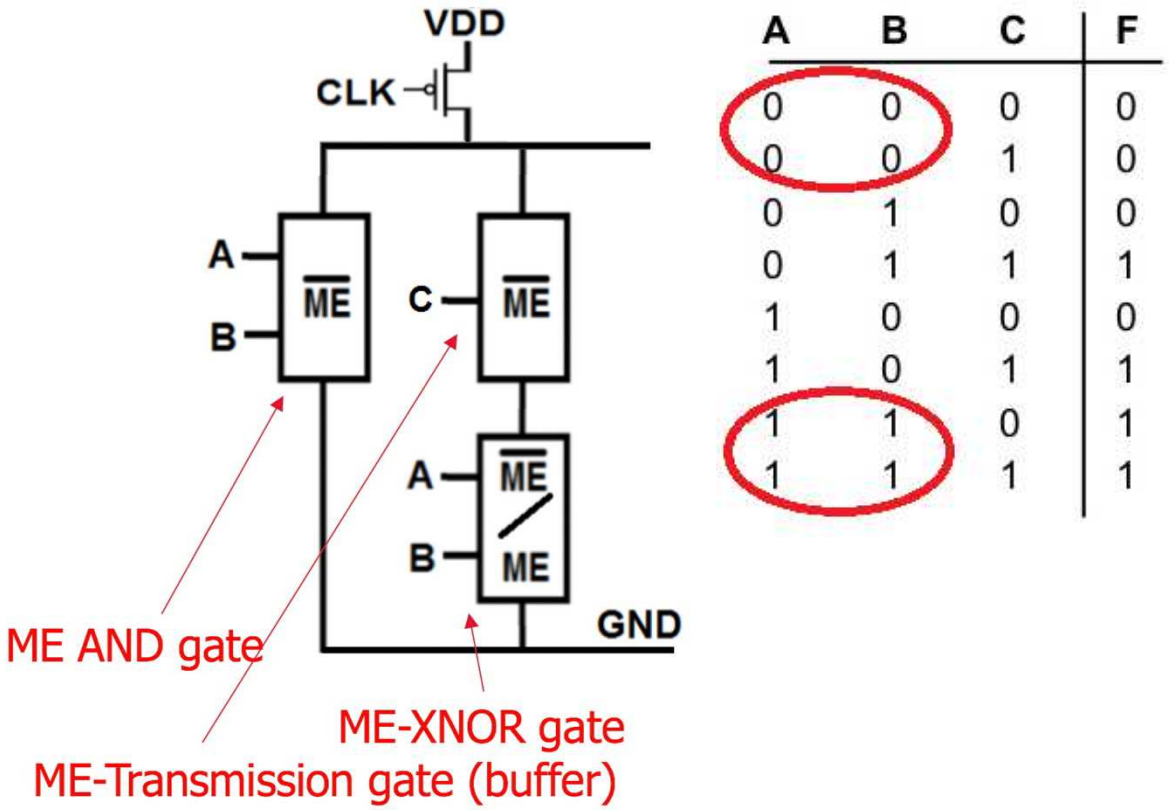


Figure 16. A schematic of basic majority gate operations using the MEFETs of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4. The MEFET state, determining current direction, is as in Figure 10. The layout is indicated to the right. Adapted from [68].

In a similar way, as was applied, for the case of the XOR gate, we can improve on the number of components we use for the majority gate, by using the split gate MEFET of Figure 14. This is laid out in Figure 17.



A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 17. A schematic of the smaller basic majority gate operations using the MEFETs of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 5 and Figure 15. The MEFET state, determining current direction, is as in Figure 10. From the logic truth table, one can see that regardless of the state of the C input, if both A and B are at logic level 1 or at logic level 0, the output of the majority gate is the same as the A and B states. This defines the left hand path, of the majority gate on the left. For the state where A and B are different, the output is the same state as C. We can create this with the right hand path.

Applying the same principles to the creation of a full-adder using the MEFET, we can create a full-adder by substituting MEFET NAND gates into the CMOS equivalent. However, we have several other options available to make the full-adder, based on the MEFET While a majority gate can be constructed in the MEFET technology, the basic gates list for the MEFET does not include the majority gate. This is because the majority gate so constructed is not a single gate, as in [82], but a combination of gates. The full-adder can be made from majority gates, but would look like the circuit of Figure 18, which is less efficient than using NAND gates alone.

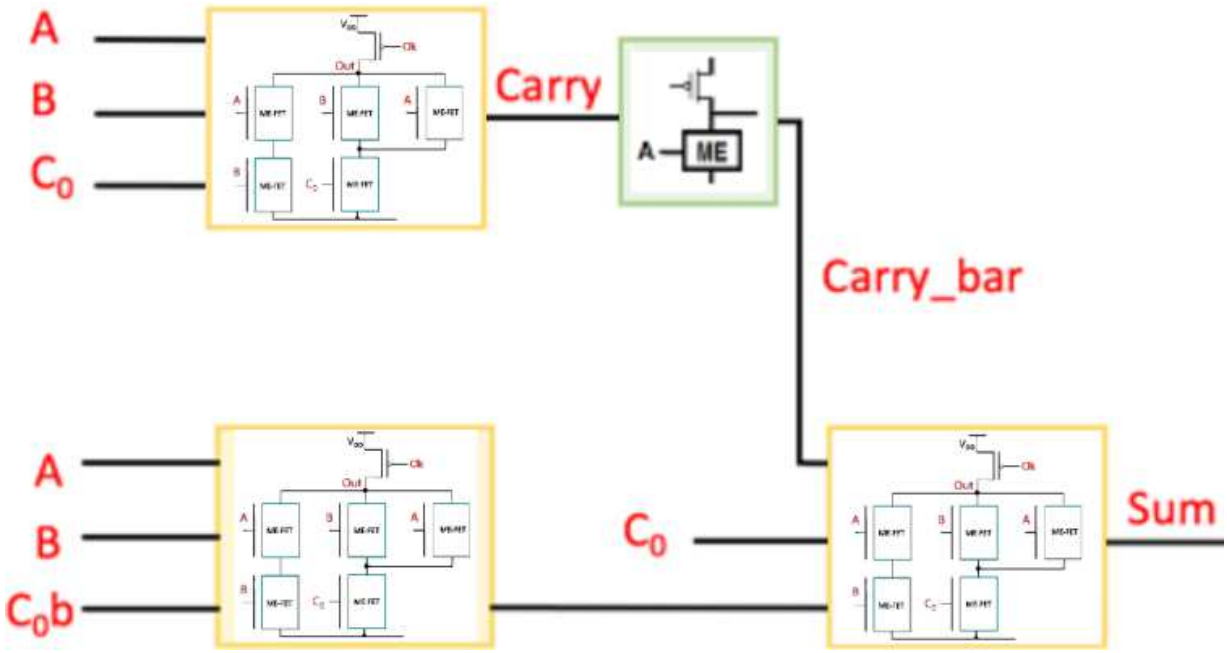


Figure 18. Full-adder concept, using MEFET devices, based on the majority gate template for the circuit of Figure 16. Adapted from [83].

Again, the full-adder is instead efficiently made from a combination of AND, buffer and XOR gates, as shown in Figure 19.

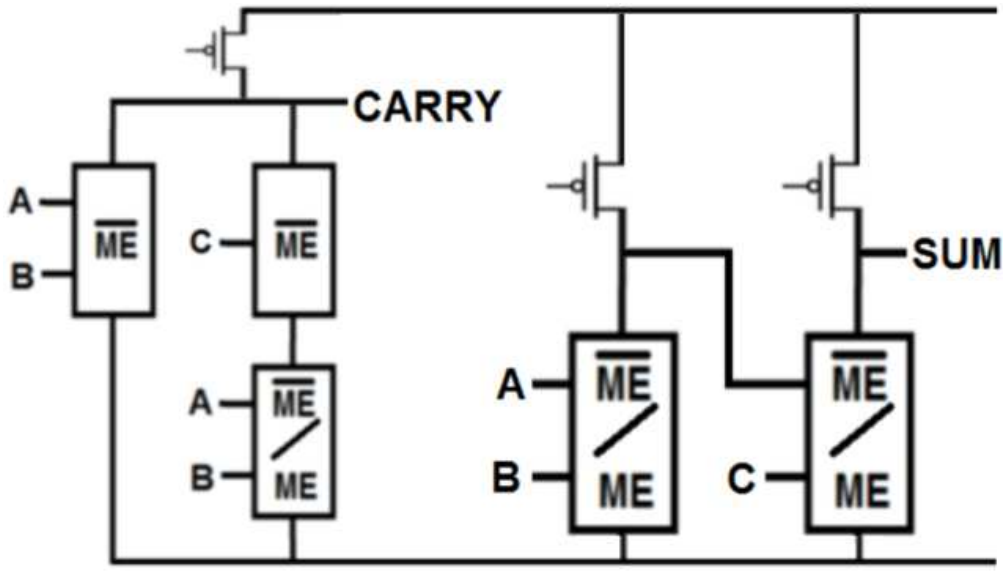


Figure 19. Full-adder using MEFET devices, using a more efficient design of XOR, AND and buffer gates using the MEFETs of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4 and Figure 14. The MEFET state, determining current direction, is as in Figure 10.

For inverter operation, CMOS has better performance than the MEFET. However, for more complex circuits, such as the 1-bit full-adder, MEFET is more competitive. The CMOS full-adder

requires typically 28 components, however, the MEFET based adder has better energy delay performance, as it requires only 23 or 8 components including read and reset circuitry (see above).

Yet the MEFET, of the spin MUXER type, of Figure 5, has very compact basic devices that include: Inverter/Buffer, Nand/And, Mux/Demux, and XOR, and these can be imagined without the driving transistors of Figure 11 and 12, as indicated in Figure 20, based on the implementation of the nonvolatile ME spinFET multiplexer (spin-MUXER) of Figure 5. The nonvolatile ME spinFET multiplexer (spin-MUXER) based full-adder, could be quite compact, as indicated in Figure 21. This large library of basic gates is common to many beyond-CMOS technologies, and opens up an avenue for circuits with reduced component count. However, key is that without the requirement for ferromagnetic domain reversal, the MEFET may provide a route to relatively faster performance circuits than CMOS. In addition, since area is thus also lower than CMOS, interconnect delay is reduced, and logic density is improved.

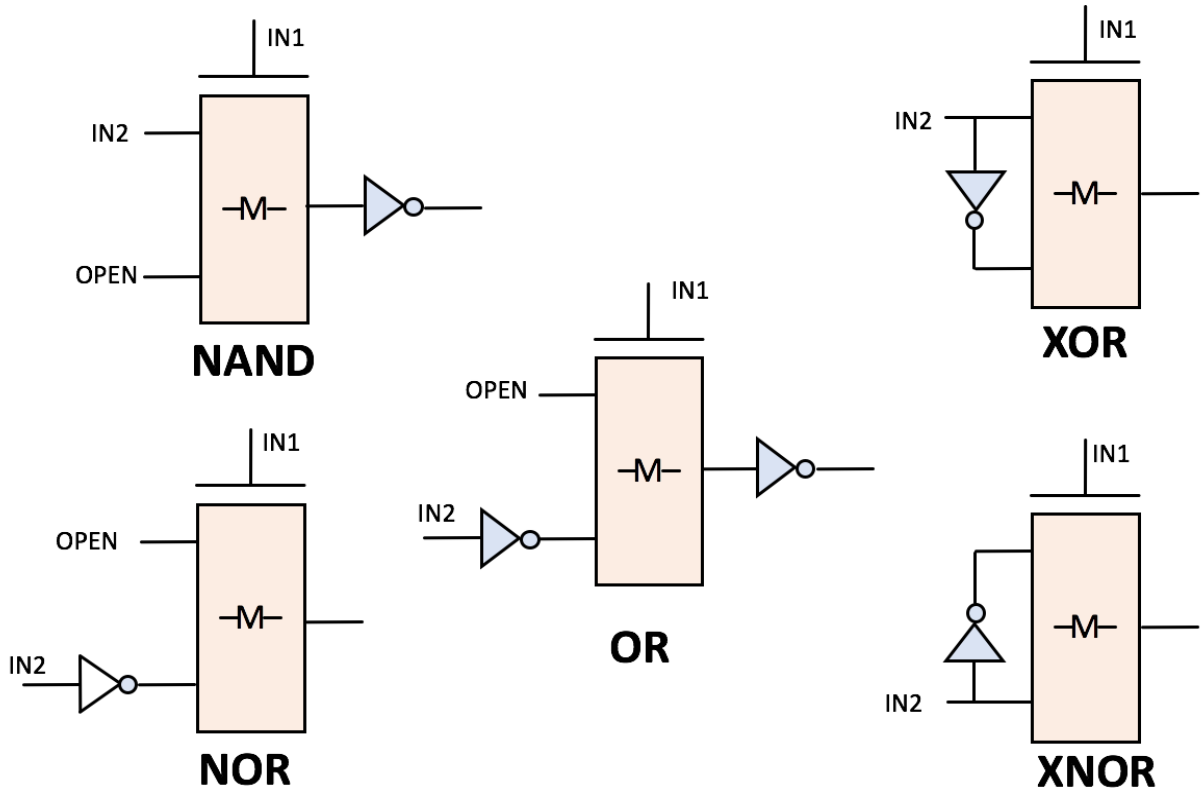


Figure 20. A schematic of basic NAND, NOR, OR, XOR and XNOR gate operations with MEFETs of the MUXER logic device type of Figure 5. The boxes, with an 'M" in the interior represent the spin MUXER device of Figure 5.

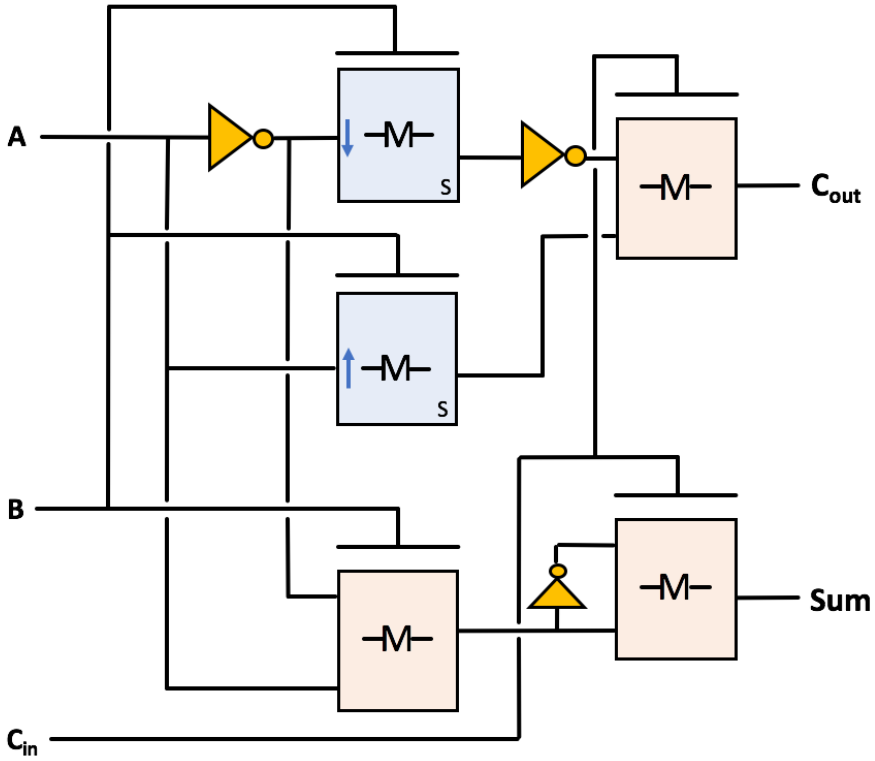


Figure 21. Full-adder using a combination of MEFET devices, of the anti-ferromagnet spin orbit read (AFSOR) logic device type of Figure 4 (blue) and spinMUXER of the type in Figure 5 (red).

6. Comparing Magneto-Electric Technologies: Benchmarking Models and Simulations

In our discussion of the MEMTJ and MEFET concepts, and possible implementation schemes (above, we have alluded to the fact that the MEFET comes across as more competitive, because of the absence of the need for ferromagnetic domain switching. To better show this comparison of these two different magneto-electric device styles, we have also simulated some of the circuits discussed above. This may provide a more objective comparison. While Matlab was widely used in early model development, here we used, for this beyond-CMOS compact models set that were verified using commercial models in Cadence, to integrate VerilogA models with the Spectre simulator, Verilog-A being the industry standard analog modeling language.

6.1 The MEMTJ Model

The energy associated with switching of an MEMTJ, and the total time – or delay – required to induce switching, is determined by analyzing the individual contributions from sections 1 to 3 in Figure 22. These describe the physics of the input stage to the device, the chromia and free ferromagnetic delay and the tunnel component characteristics [66].

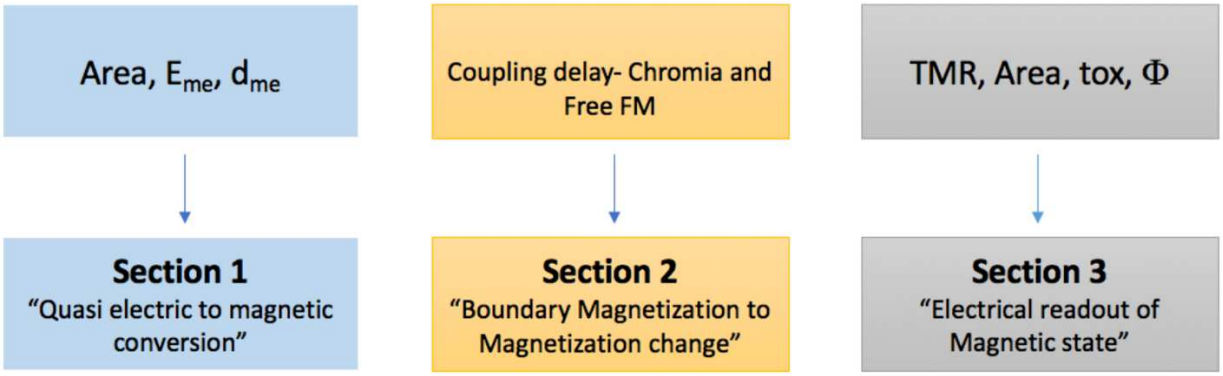


Figure 22. Sections of the MEMTJ model, showing electrical input characteristics, coupling of the magnetics and output characteristics.

As described above, through magneto-electric coupling, the electric field (the applied voltage) induces a change in boundary magnetization of the dielectric magneto-electric (chromia) layer and, in a nonlinear manner, will reverse the polarity at the interface with the free FM. This problem may be described in terms of the charging of an *RC*-capacitor network, in which the relevant capacitance is that of the ME layer ($C_{ME} = \varepsilon_{ME}\varepsilon_0 A/t_{ME}$, where ε_{ME} is the dielectric constant of the ME layer of thickness t_{ME} and A is the cross-sectional area of the device) and the resistance (R_{in}) basically the load of the driving stage on the input side. The *RC*-constant associated with this capacitor ($\tau_{ME} = R_{in}C_{ME}$) defines a transient charging current $I_{ME} = C_{ME}V_g/\tau_{ME}$, where V_g should be in the range of 100 – 200 mV for sufficiently thin films. In this way, the energy cost associated with the electric-to-magnetic conversion step can be computed as:

$$E_{ME} = \frac{1}{2} C_{ME} V_g^2. \quad (1)$$

Pertinent to the model laid out in references [30, 31], the next stage in the switching is denoted by panel (b) of Figure 22 and corresponds to the process in which the induced boundary magnetization at the surface of the ME generates an exchange bias that reverse the magnetization of the free FM. The description of this process of "magnetization transfer" represents the most uncertain aspect of our compact model, in the sense that there is presently little that is known experimentally about the speed and energy cost. In the absence of such knowledge, we are forced to make a reasonable estimate for the time (τ_{xfer}) required for the magnetization-transfer. In the simulations here we take τ_{xfer} = 200 ps, a value that is smaller than the experimental switching speeds (~500 ps) of some spin-transfer-torque magnetic MTJ devices [78], but consistent with the estimate of 178 ps in [23]. This estimate does not, however, consider the influence of Gilbert damping, a process that may add significant viscous drag [84] to the magneto-electric domain-wall motion that governs switching. In considering the influence of this damping [85], it has been proposed that the domain wall velocity should be limited to a maximum value $v_{max} = \gamma H \lambda_o/4$, where γ is the gyromagnetic ratio, γH is the free-electron spin-resonance frequency, and the length parameter λ_o is related to the scale of the domain-wall width. The expression of [84] was used to estimate a velocity v_{max} = 5 nm/ns, implying a switching time of 2 – 3 ns for a device with a critical dimension of 15 nm.

To determine the energy cost (E_{xfer}) associated with the magnetization-transfer process we use:

$$E_{xfer} = \frac{V}{2}\mu_r\mu_0 H_c^2 \,, \quad (2)$$

where μ_r is the relative permeability of the free FM, μ_0 is the permeability of free space, and V is the volume of the free layer. The field strength (H_c) in this relation is the interfacial magnetic field responsible for the magnetization rotation in the free FM and is written as [85]:

$$H_c = 2\frac{\sqrt{A_{\mathrm{AF}}K_{\mathrm{AF}}}}{M_{\mathrm{FM}}t_{\mathrm{FM}}}, \quad (3)$$

where K_{AF} is the magnetocrystalline anisotropy of the antiferromagnetic magneto-electric, and A_{AF}, M_{FM} and t_{FM} are the exchange stiffness, magnetization and thickness, respectively, of the free FM.

The final process of the modeling, as illustrated in Figure 22 (see panel (c)), is one in which we perform electrical readout of the MTJ as a means to detect the relative alignments of the pinned and free FMs in the MTJ. To determine the energy cost associated with this stage of the device we once again treat it as a capacitor-charging problem in which the relevant resistance now involved is dominated by that of the MTJ. For a parameterization of the resistance of the MTJ, we write the resistance (R_{P}) when the magnetization of the two FMs is parallel as [86]:

$$R_{\mathrm{P}} = \frac{t_{Ox}}{FA\varphi^{0.5}}e^{1.025\varphi^{0.5}t_{\mathrm{Ox}}}, \quad (4)$$

where t_{Ox} is the thickness of the MTJ dielectric layer, which in this case we shall take for representative purposes to consist of MgO. φ is the potential-barrier height of the tunnel dielectric, A is the cross sectional area of the device and F is a factor that is calculated from the resistance-area product of the junction. The value of this parameter is material dependent, and in the simulations here we use the value of 332 adopted in [86]. With the resistance for parallel magnetizations defined this way, the resistance (R_{AP}) of the MTJ with antiparallel magnetization of the two FMs is expressed as [55]:

$$R_{\mathrm{AP}} = R_{\mathrm{P}}(1 + \mathrm{TMR}) \,, \quad (5)$$

where TMR is the value of the tunneling magnetoresistance.

Using the resistances defined in Eqs. (4) & (5) we note that the readout current (I_{OUT} in panel (c)) that flow in response to some drive voltage (V_{OUT}) across the two FMs is governed by a time-constant (τ_{OUT}) that can be expressed as $\tau_{\mathrm{OUT}} = R_{\mathrm{Av}}C_{\mathrm{MTJ}}$. Here $R_{\mathrm{Av}} = ½(R_P + R_{AP})$ is the average resistance of the MTJ and $C_{\mathrm{MTJ}} = \varepsilon_{\mathrm{MTJ}}\varepsilon_0 A/t_{\mathrm{MTJ}}$ is its capacitance (with $\varepsilon_{\mathrm{MTJ}}$ dielectric constant of the MTJ insulator). With these various parameters defined, the readout current is easily calculated as $I_{\mathrm{OUT}} = (C_{\mathrm{MTJ}}V_{\mathrm{OUT}})/\tau_{\mathrm{OUT}}$ while the energy cost associated with this process is:

$$E_{\mathrm{OUT}} = C_{\mathrm{MTJ}}I_{\mathrm{OUT}}\tau_{\mathrm{OUT}} \quad (6)$$

While Eqs. (1) – (6) describe the energy cost associated with switching of the MTJ, another factor that must be considered is that of "off-current" leakage. The small size of the TMR (~10) in realistic MTJs means that, even in their high-resistance state, they can still consume significant power. This is very different to CMOS, where one transistor in any inverter pair is typically in a

highly-resistive off state. To account for dissipation in the MTJs we consider a circuit driven at a fairly typical frequency of 1 GHz. Assuming a 4-phase clocking scheme, the leakage energy is calculated based on a 25% duty cycle.

$$E_{\mathrm{Leak}} = \frac{1}{4}\frac{V_{\mathrm{OUT}}^2}{R_{\mathrm{Av}}}T\ , \quad (7)$$

where T = 1 ns is the period of the 1 GHz signal.

Table 1 lists the key parameters of our compact model, along with a description of their basic significance and the values assigned to them in our calculations. These calculations are performed assuming a basic feature size "*F*" of 15 nm, to allow comparison with projections for the 15-nm node of scaled CMOS technology. As a final point we note that, while we have thus far developed our model in terms of the ME-MTJ of Fig. 1, our approach is easily adapted to the analysis of devices such as the majority gate of Figure 6 [30, 31, 65, 66] and the XNOR gate of Figure 7 [30, 65, 66]. For the majority gate, the only difference with the ME-MTJ model lies in the first stage of electric-to-magnetic conversion, where the gate voltage is now applied to three separate electrodes. At the same time, a slightly higher voltage is required for each of these electrodes in order to be able to induce the collective switching of the chromia that provides the majority-gate function. Similarly, for the XNOR/XOR gate, we now have two input stages as a result of replacing the fixed FM with an additional, ME-controlled, free layer. The effect of this additional gate stage is easily incorporated into our calculations, by replicating the stages of electric-to-magnetic conversion and magnetization transfer.

Parameter	Value	Description of Parameter and Units
A	900	Area of ME-MTJ stack, nm^2
A_{AF}	8.4×10^{-12}	Exchange stiffness, J/m [87]
ε_{ME}	12	Dielectric constant of chromia [63]
ε_{MTJ}	10.1	Dielectric constant of MTJ dielectric (magnesium oxide)
φ	0.4	Potential-barrier height of the MTJ tunnel dielectric [86]
K_{AF}	10^{-6}	Magnetocrystalline anisotropy of antiferromagnetic pinning layer, J/m^3 [88]
M_{FM}	0.456×10^6	Perpendicular magnetization of ferromagnetic layers, A/m [86]
$\mu_r\mu_o$	4	Permeability of the free FM [23]
R_{in}	1100	Load resistance from driving stage and interconnects, Ω
T	1	Time period of the 1-GHz clocking signal, ns
t_{FM}	30	Thickness of the free ferromagnetic layer, nm
t_{ME}	10	Thickness of the magnetoelectric layer, nm
t_{MTJ}	2	Thickness of the MTJ dielectric (magnesium oxide), nm

TMR	10	Tunneling magneto-resistance magnitude
V	$A \times t_{FM}$	Volume of the free FM layer
V_g	0.1	Voltage applied across ME layer, V

Table 1. Key parameters used in our compact model of the ME-MTJ. Adapted from [30, 31].

6. 2. The MEFET Model

The modeling for the MEFET device is shown in Figure 23. $R_{channel}$ is the resistance across the two-dimensional (2D) narrow channel and an additional resistance R_{int} is added in series to the $R_{channel}$ to define the boundary conditions for switching. There are two aspects of the model developed here: (a) ME control of the channel spin polarization which is based on the proximity induced polarization in the narrow 2D channel and the (b) spin inject/detect function which is based on the injection into the source and then detection at the drain.

Among the key issues are first the magneto-electric control of the channel spin polarization Here, the gate voltage modulation must be taken into account. The ME layer induces spin polarization in the channel due to the proximity of magnetic atoms or a magnetically ordered substrate [19, 32]. A magnetoelectric like chromia is highly resistive [89] serving as a dielectric gate to the 2D channel. It also has high interface polarization which can be controlled by voltage [19, 32, 36, 53, 90]. When voltage is applied across the "G" and "BG" terminal, this is equivalent to charging of the ME capacitor. The computed delay element is associated with the boundary magnetization between the ME film and the interface of the channel. The switching time of the MEFET device is then limited only by the switching dynamics of the ME.

Also of some importance is the spin detect/inject function. The charge current is injected into the source and the boundary magnetization between chromia and channel gives rise to damped precession of the spins. The spin current is then detected at the drain through a pull up component (Figure 23).

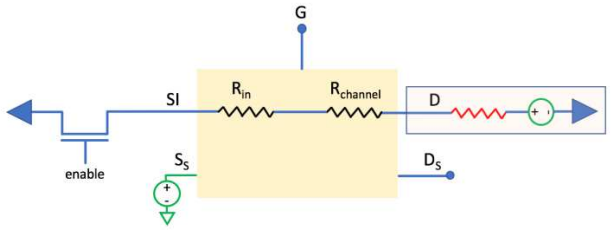


Figure 23. Single source MEFET modeling scheme. Rin and Rchannel represents the internal and channel resistance of the device. Adapted from [68, 83].

For the single source version, additional spin state terminals ("S_S" and "D_S") are added to validate the spin state injected/detected at the source/drain terminals as shown in Figure 23. The 'up' and 'down' spins are represented by constant voltages sources with '+1 V' and '-1 V' respectively at the "S_S" terminal. To model the dual source MEFET (as in Figure 5), three additional terminals should be included to detect the state of spin current injected into the sources i.e. ("S_{1S}" and "S_{2S}") and the corresponding spin current detected at the drain terminal ("D_S"). The model [68, 83] was developed such that, before the simulation is run, the injected spin orientation can be selected, making the model flexible to obtain various logic functions.

In the compact models, the precessional delay across the FM layer was taken into account by a fixed delay assumed to be 200 ps. This assumption is based on the best estimate of the coupling delay [23]. Additional dissipation and moving antiferromagnetic domain wall precession could significantly add to the delay time [84], but is not considered here. The physicals effects are also incorporated [86]. Table 2 lists the parameter values used in the models.

Parameter	Value	Description of Parameter and Units
ε_{ME}	12	Dielectric constant of chromia [63]
ε_{MTJ}	10.1	Dielectric constant of MTJ dielectric (magnesium oxide)
φ	0.4	Potential-barrier height of the MTJ tunnel dielectric [86]
t_{FM}	30	Thickness of the free ferromagnetic layer, nm
t_{ME}	10	Thickness of the magnetoelectric layer, nm
t_{MTJ}	2	Thickness of the MTJ dielectric (magnesium oxide), nm
V_g	0.1	Voltage applied across ME layer, V

Table 2. Compact model parameters of the MEFET, used in the VerilogA model. Adapted from [68, 83].

Using the MEMTJ and MEFET Verilog-A models, and supplementing with CMOS for most clocking needs, accurate simulation using Spectre becomes feasible. In addition to simulations to compare the basic device performances (Inverter and Nand functions), the full-adder was also simulated. These simulations have been performed using at a technology equivalent to the 15-nm node, and compared to CMOS performance at the same process node.

The MEFET full-adder using majority gates (Figure 6) and exclusive NOR gates (Figure 7) was simulated with appropriate clocking, and shown to be functional (Figure 24) [31].

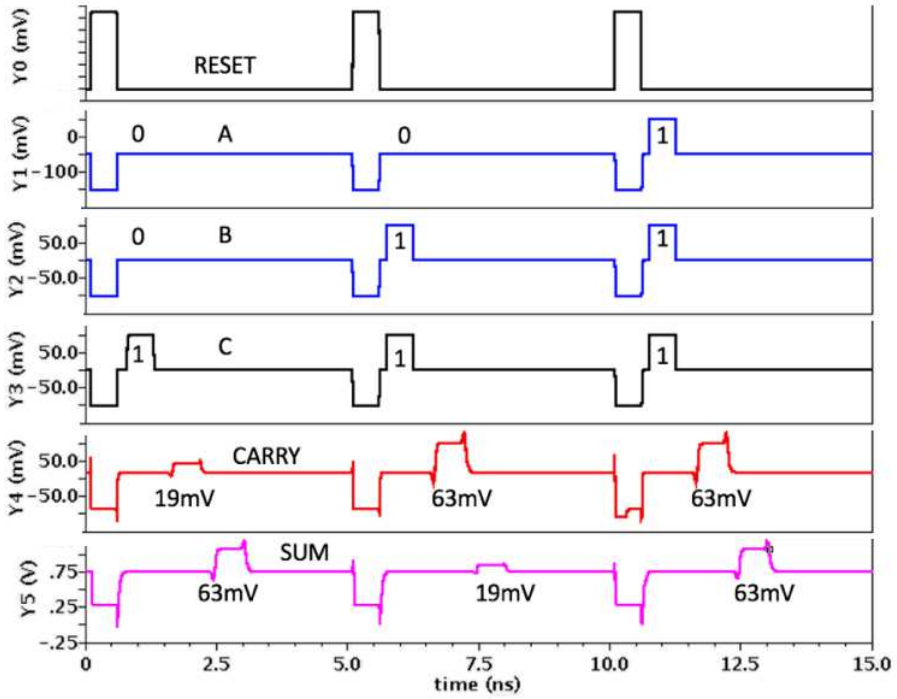


Figure 24. The MEMTJ full-adder Spectre simulation, showing functionality as inputs A, B and C(carry-in) input voltage states scroll through options 0,0,1 and 0,1,1 and finally 1,1,1 the Carry-out and Sum are seen to operate as expected. Adapted from [31].

The full-adder simulation using MEFET devices was made from the circuit of (Figure 19) [83]. For multi-stage circuit design, reset functionality is needed to reset the state of the chromia spin vectors. At the beginning of each cycle, the circuit path is reset. The resulting circuit functionality is shown in Figure 25.

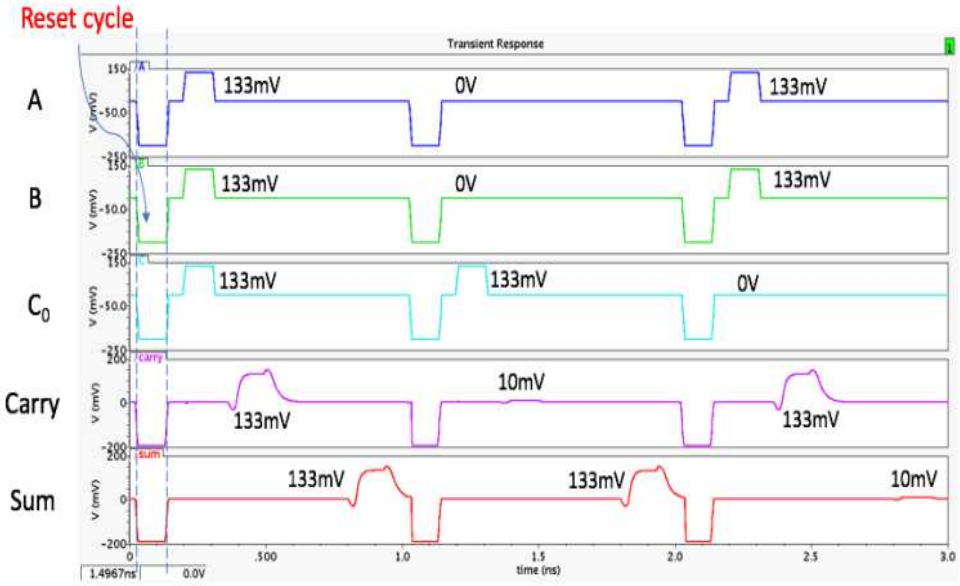


Figure 25. The transient simulation results of the MEFET full-adder circuit, showing functionality as inputs A, B and C(carry-in) input voltage states scroll through options 1,1,1 and 0,0,1 and finally 1,1,0 the Carry-out and Sum are seen to operate as expected. Adapted from [83].

6.3. Comparing the MEMTJ and the MEFET

Once the basic circuit operation has been verified, it became possible to determine performance parameters of switching delay and power, and populate an energy-delay plot, considered to be a significant benchmark of comparison between technologies. As discussed above, designing with 'native' gates (Majority gate for MEMTJ) improves performance, and sometimes energy. Design with enhanced gates (XNOR for MEMTJ) improves things further. The MEMTJ and its derived devices have been presented previously in [31]. The MEMTJ based devices have been benchmarked with respect to CMOS and other device architectures. However, as noted throughout, due to the large exchange coupling delays for switching the FM layer, the MEMTJ has a poor performance. The device modification and enhancements that led to the MEFET, initially also does not look great when applying conventional benchmarking, but when native and enhanced circuit options are used, we find that the resulting circuit/device combination crosses the CMOS benchmark, meaning we achieve a lower power and/or a higher performance. Current MEFET designs are now predicted to about a factor of three better in energy and delay than CMOS. Realistically, we probably need about a factor of 10 for serious consideration of the technology to replace CMOS, but the signs are promising, as indicated by the schematic of Figure 19. Even without considering the more MEFET devices and circuit implementation concepts that are only now emerging, the MEFET performs 10x better than the MEMTJ. The MEFET devices also have significantly better on-off ratios (~10^7) compared to the ME-MTJ with its on-off ratio of just 10x (Figure 26).

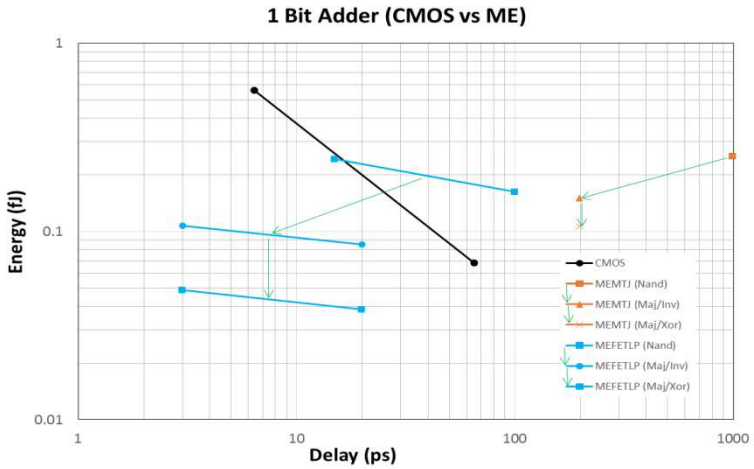


Figure 26. Progression of performance improvement, first of MEMTJ compared to silicon CMOS, then to the MEFET compared to CMOS, showing that not only are the material characteristics important, but so too is device design and also circuit design. The MEFET full-adder, of Figure 17, achieves a better performance than CMOS. Adapted from [83].

One of the four major design benchmarks is chip area (Figure 27). This is a proxy for chip cost, but smaller circuit area has additional benefits: A smaller chip means a smaller package might be used, and that greater logic density is achieved. From a circuit performance point of view, we also get lower capacitance for faster and lower energy chips – If a beyond-CMOS chip is smaller than the CMOS chip it is equivalent to, the electrical currents, active power and delay associated with the chip are lower.

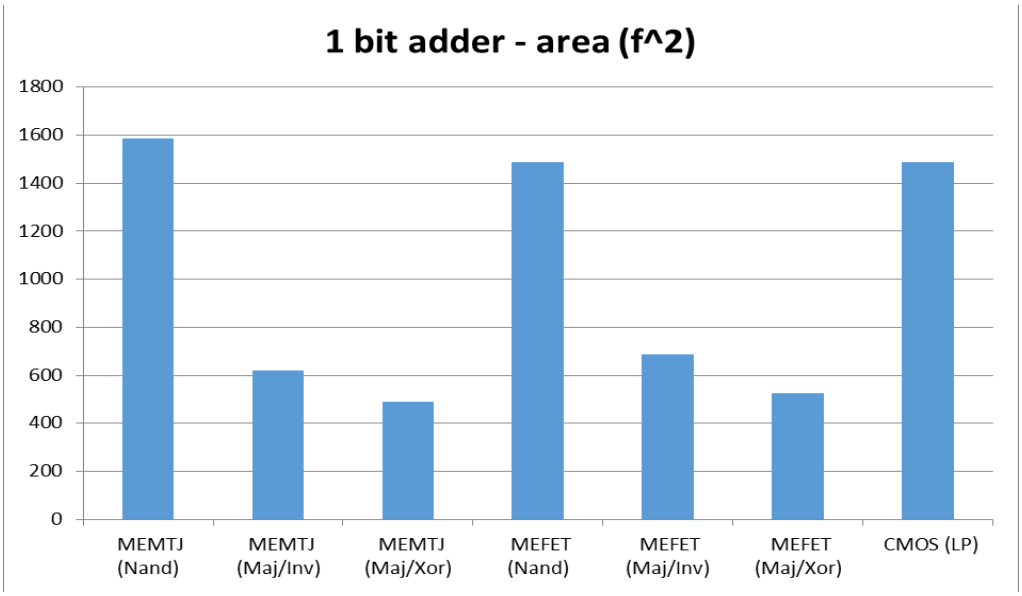


Figure 27. Area improvement, of MEMTJ and MEFET compared to silicon CMOS, for a full-adder circuit.

Comparing Area to energy*delay product, we observe a more significant benefit from MEFET technology compared to CMOS, as seen in Figure 28.

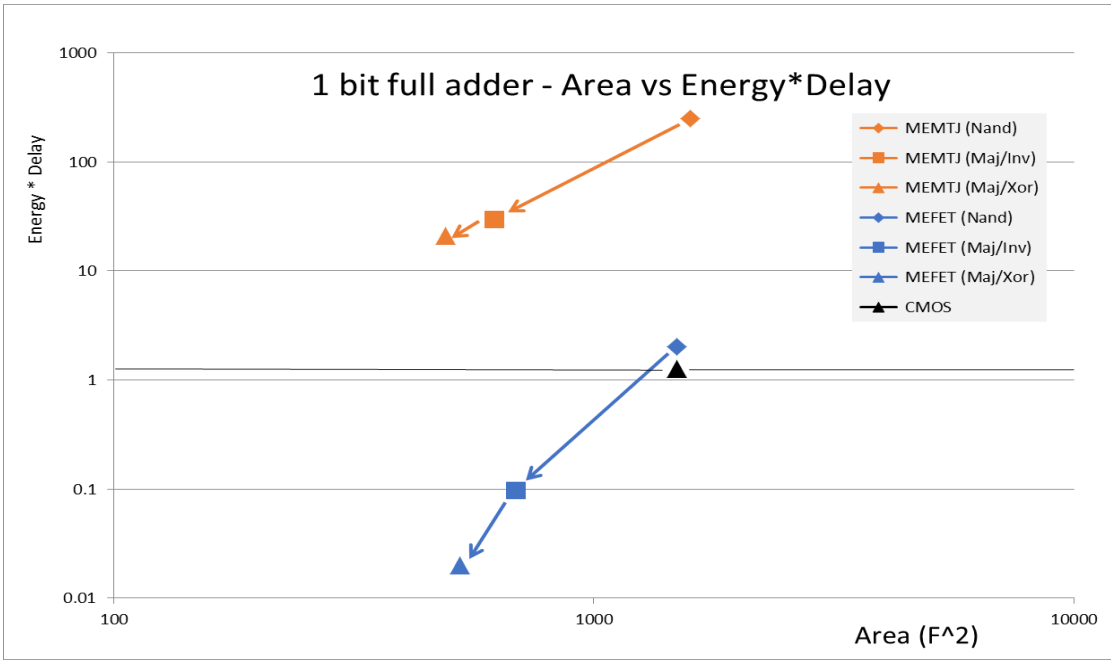


Figure 28. Area vs energy*delay, showing a significant benefit from MEFET technology over CMOS.

7. Summary

Conventional silicon CMOS has been the mainstay of the semiconductor logic industry for fifty years. There is an increasing need to replace or supplement the technology with lower power and faster circuits. As a result, logic that can replace or be used in conjunction with CMOS is being

researched at an ever increasing pace. We have here concentrated on the trends seen over the past five to ten years in magneto-electric based device technologies, showing that as materials, devices and logical concepts have grown together. While at the outset, the technology was not excessively impressive, recent developments suggest that as the device concepts have evolved, and implementation schemes improved, the circuit area is reduced, and performance is significantly better and leakage and power are also reduced compared to silicon CMOS. In addition, magnetoelectrics provide the advantage that each device in the circuit has built in memory, thus power can be removed for a period of time and the logic state is not lost when power is removed. Further improvements in the MEFET benchmarking seem likely given the increasing efforts in improved device and circuit design, and given that only a few of the most promising circuits and device implementations have been benchmarked.

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