Sub-Sampling Direct RF-to-Digital Converter With 1024-APSK Modulation for High Throughput Polar Receiver

Hechen Wang, *Member, IEEE*, Fa Foster Dai, *Fellow, IEEE*, Zhan Su, and Yanjie Wang, *Senior Member, IEEE*

***Abstract*— This article presents a direct RF-to-digital converter (RDC) for polar receivers, in which the amplitude information of the received signal is detected by a reconfigurable analog-to-digital converter (ADC) and its phase is digitized using a time-to-digital converter (TDC). The RDC prototype also includes a multi-phase reference generator and an ADC sampling position adjustment unit realizing the sub-sampling technique. Unlike conventional direct-RF sampling receivers, the proposed RDC samples the input RF signal at the baseband rate. The RDC is capable of digitizing a variety of modulation waveforms, such as quadrature amplitude modulation (QAM), phase shift keying (PSK), and amplitude phase shift keying (APSK). When comparing QAM to APSK, the later has advantages of relaxed system requirements on phase noise and linearity. The proposed direct RF-to-digital polar converter IC achieves a maximum data rate of 1.94 GB/s with a 1024-APSK modulation at a carrier frequency of 6 GHz, while consumes only 3.8 mW power under 1.1 V supply.**

***Index Terms*— Amplitude phase shift keying (APSK), analog-to-digital converter (ADC), blocker tolerance, direct RF sampling, nonlinear distortion, phase noise, polar receiver, quadrature amplitude modulation (QAM), RF-to-digital converter (RDC), sub-sampling, time-to-digital converter (TDC).**

I. Introduction

ALTHOUGH the quadrature up- and down-conversions have been the most popular architecture for conventional transceivers (TRX), communication system designers are seeking alternative approaches to fulfill the requirements of high power efficiency and high reconfigurability in the development of the Internet-of-Things (IoT) networks. Shown in Fig. 1, a direct-RF transceiver directly uploads the baseband data onto the RF carrier frequency through an RF digital-to-analog converter (DAC) and directly sample the RF modulated signal using high-speed analog-to-digital converters (ADCs). This direct RF-sampling approach has attracted increased attention recently due to the improvement of data converters in advanced technology nodes. Compared with conventional TRX, the direct-RF TRX gains advantages in the following key aspects including: (1) the overall topology of the TRX signal chain is greatly simplified; (2) the fast sampling rate enables the usage of wide-bandwidth signals and improves the data throughput; (3) the reconfigurability allows one RF-sampling per radio for multi-band and multi-standard applications. As a result, the direct-RF technique is more suitable for software-defined radios. However, the utopian radio has one bottleneck that prevents it from being broadly adopted by industry that is its need for ultra-high speed, high precision data converters. As shown in Fig. 2, to enable applications, ADCs and DACs running at multiple GS/s rate with 10–12 bits precision are indispensable [1]–[9]. However, a data converter with such high sample-rate typically consumes several hundred mWs or several Watts of power. As a result, the advantages of the direct-RF architecture are eventually neutralized due to those nonrealistic requirements.

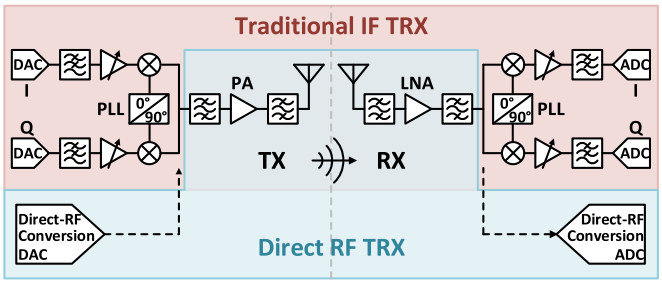

Fig. 1. Direct-RF wireless polar transceiver architecture.

Fortunately, alternative approaches without using ultra-high-speed converters exist to deal with the power efficient problem. In the TX part, as illustrated in Fig. 3, a digital phase-locked loop (DPLL) based polar TX is one possible solution. By utilizing a multi-point injection DPLL [10]–[13] and a digital power amplifier (DPA) [14]–[16], the phase (PHS) and the amplitude (AMP) information are separately uploaded onto the RF carrier frequency in a polar system. The key point that needs to be pointed out is the sampling rate of both the DPLL phase modulator and the DPA amplitude modulator in a polar TX are only several times of the baseband frequency. Although direct-RF polar TX has been invented and studied

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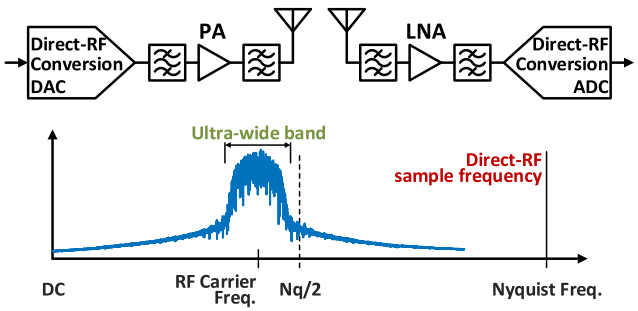


Fig. 2. Ultra-wide band signal direct-RF sampling requirement.

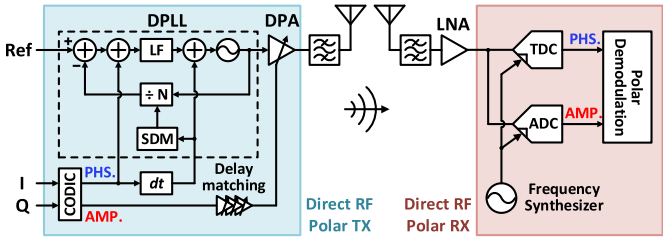


Fig. 3. Polar direct-RF sampling TRX, the DPLL and DPA based direct-RF polar transmitter and the TDC and ADC based direct-RF polar receiver.

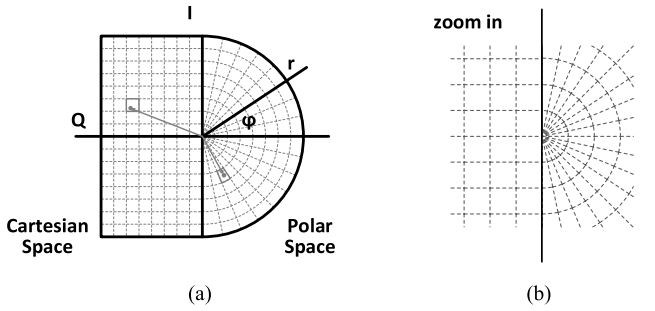


Fig. 4. Denotation of (a) Cartesian and polar quantization cells. (b) zoomed-in area.

intensively for years, the direct-RF polar RX, which detects the phase and amplitude information of the received signal, as shown in Fig. 3, has been barely investigated with very few successful implementations.

Furthermore, compared to conventional Cartesian I/Q TRX, polar transmitters (TXs) are much more power efficient when dealing with large peak-to-average ratio modulations [17]–[19] and polar receivers (RXs) require less data converter number of bits (NoBs) to reconstruct signals with the same signal-to-noise ratio (SNR) [20]–[22]. Meanwhile, the next generation wireless communication systems are expected to support expanded constellation modulation schemes to achieve multi Gb/s data throughput with a reasonable power budget. Complex modulation schemes normally come with high-density constellations, such as 256-quadrature amplitude modulation (QAM) and 1024-QAM, which demand extremely stringent requirements on both the phase noise of the phase-locked loop (PLL) and the linearity of the PA in a conventional Cartesian based I/Q TRX system. In order to meet the requirement, advanced techniques such as sub-sampling PLLs and nonlinear compensated PAs have been introduced, which barely support the high-density modulations and leave limited design margin for the overall system.

The quantization resolution is derived from the SNR requirement set by the modulation types. In an I-Q topology, the quantization step is uniformly distributed in Cartesian space, assuming that half of the step is less than the minimum detectable signal, as shown in Fig. 4. However, the magnitude of quantization step in a polar space varies according to the signal magnitude, namely, it becomes finer when the signal magnitude is smaller, which intrinsically reflects the quantization needs based on SNR requirement. On the other hand, the phase requirement is not normally set by the noise, which requires higher resolution. Instead, the minimum phase step is set by the modulation schemes such as the minimum phase angle between two adjacent constellation symbols. In addition, phase data has better noise and nonlinearity tolerance and can be reconstructed more easily under distortion and compression. As a result, polar converters can achieve higher signal-to-quantization noise ratio (SQNR) than their Cartesian counterparts [20]. Polar TXs [13]–[19] and polar RXs [21] require fewer data converter NoBs to reconstruct signals and have better phase noise and nonlinearity tolerance.

Another major concern for both the direct-RF and polar receiver is the blocker tolerance issue. Theoretically, the blocker tolerance performance of the direct-RF receiver can outperformance conventional architecture according to the article [23]. However, it puts a great burden on the data converters. Without conventional down conversion, the in-band adjacent channel signals become modulated blockers to the receiver and are much difficult to be filtered at RF frequency. Due to the limited blocker tolerance performance, direct-RF architecture is attracted by some unconventional applications, such as high-IF topology, wireless chip-to-chip, and die-to-die communications [5], [24], [25], which have single channel and lower interference level. Especially in mm-Wave and THz range, a much higher path loss leads to a cleaner spectrum with less blockers. Some of the standards such as IEEE Standard for High Data Rate Wireless Multi-Media Network (IEEE Std 802.15.3 [26] and IEEE Std 802.15.3d [27]) have limited number of channels with a loosened channel transmission spectrum mask or only one channel per band, as a result, the requirements of blocker tolerance are relaxed. With the development of the RF channel selection filter [28]–[30] and the aid of blocker detection and blocker canceling techniques [31], [32], direct-RF and polar receiver is capable to support multi-channel, wideband applications as well.

This work presents a prototype of direct-RF sub-sampling conversion system for polar RX. This article is organized as follows. Sections II and III describe the operational principle, the architecture, and the circuit implementation of the proposed converter. The measurement results are summarized in Section IV and the conclusions are drawn in Section V.

II. Polar Based Sub-Sampling Direct RF-to-Digital Conversion

As illustrated in the previous section, the major obstacle for the implementation of a direct-RF receiver is the challenge of

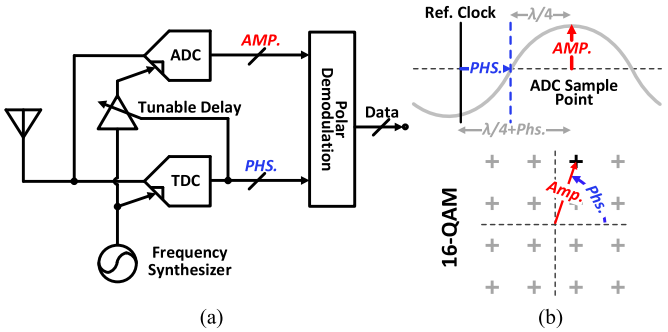


Fig. 5. Illustration of (a) proposed polar receiver concept and (b) conversion principle.

designing a high-performance data converter. In the current direct-RF receiver architecture, an ADC sampling at RF frequency is inevitable, yet it is not power efficient and requires great design effort. Improving ADC's figure of merit (FoM) faces two critical challenges in the advanced CMOS technology: 1) lowered supply voltage reduces ADC dynamic range in the voltage domain and 2) comparator design does not benefit much from the technology scaling. A question then arises: is it possible to shift part of the workload from amplitude domain to time domain, which becomes increasingly effective when feature size shrinks?

The PHS and the AMP are modulated to the carrier frequency signal through two essential blocks in a polar TX, the DPLL and the DPA. In a polar RX, the PHS and AMP information can be extracted by using a time-to-digital converter (TDC) and an ADC, respectively. The burden on the direct-RF sampling ADC is now undertaken by the ADC and TDC together. The received signal is processed in both the time domain and amplitude domain. As a result, the performance requirements for both TDC and ADC are greatly relaxed, leading to less design complexity, reduced sampling rate, and lower power consumption eventually.

The basic polar RX conversion procedure is depicted in Fig. 5(a). For a single carrier modulated signal, the TDC measures the time interval between the reference clock and the zero-crossing point of the received signal. The result of the TDC represents PHS information. The ADC sampling point is then adjusted based on the TDC's output, namely, the PHS information, and is delayed to the position $\lambda/4$ after the zero-crossing point. Fig. 5(b) illustrates the conversion principle: The TDC detects the time interval between the reference clock and zero-crossing point of the received signal indicating the phase of the current symbol. The AMP is represented by the peak point of the received signal in each symbol, which appears $\lambda/4$ after the zero-crossing point. The ADC sampling point is adjusted based on the TDC resolved zero-crossing point. Then with the detected AMP and PHS information, the constellation point can be easily restored in the digital baseband.

The PHS and the AMP can be easily obtained when dealing with the baseband signal in Fig. 5(b). However, the transmitted signal is filtered, and band limited by the maximum physical bandwidth of the circuits such as the PA and the spectral mask restrictions as presented in Fig. 6(a). On the constellation plane, as given in Fig. 6(b), the PHS and the AMP of the points

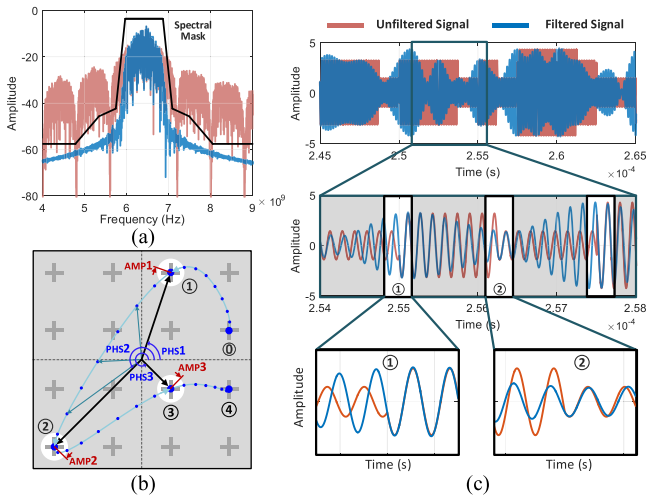


Fig. 6. Once the signal is filtered, (a) spectrum is limited to a narrowband and (b) trajectory between two symbols becomes a smooth curve. (c) Valid sampling positions located in a narrow time window.

on the trajectory in between each symbol, for instance between symbol ① and symbol ②, are equal to neither PHS1 AMP1 nor PHS2 AMP2. Only the areas close to symbol ① and symbol ② have valid PHS and AMP information that can be used for demodulation. So, it is questionable if the previously mentioned polar RX schemes can be used to detect the PHS and AMP of the received signals. Fig. 6(c) presents the signal waveform in the time domain. The red curve is the ideal unlimited bandwidth signal, while the blue curve shows the filtered realistic band limited signal that transmits in the channel. A large discrepancy can be easily observed between the filtered waveform and the original baseband waveform. Instead of having an abrupt change, the phase and amplitude gradually evolve from one symbol to the next. In such a complicated situation, it is hard to identify the zero-crossing point and the corresponding amplitude sample position with filtered signal. Let us take a closer look at the band limited signal in Fig. 6(c), overlapping the unfiltered and filter signals, it is clear that the filtered signal coincides with the unfiltered signal at the edge between two adjacent symbols. In these regions, the PHS and the AMP represent the actual transmitted constellation information. As a result, the valid PHS and AMP for each symbol need to be obtained only within a limited time window located at the edge of two adjacent symbols as the window ① and ② in Fig. 6(c).

III. Polar Based Direct RF-to-Digital Converter

To realize the direct-RF sampling without using ultra-high-speed ADCs, we propose a polar based receiver architecture given in Fig. 7. The core of the receiver is a direct RF-to-digital conversion system, consisting of a 2-bit per cycle SAR ADC with reconfigurable NoBs from 4 to 8 bits and a TDC with tunable resolution from 2 to 5 ps to resolve the AMP and PHS of the modulated input RF signals, respectively. The proposed RF-to-digital converter (RDC) consists of three major parts: (1) TDC based PHS detection path; (2) ADC based AMP detection path; and (3) sub-harmonic injection locked multi-phase reference generation and ADC sampling position adjustment block.

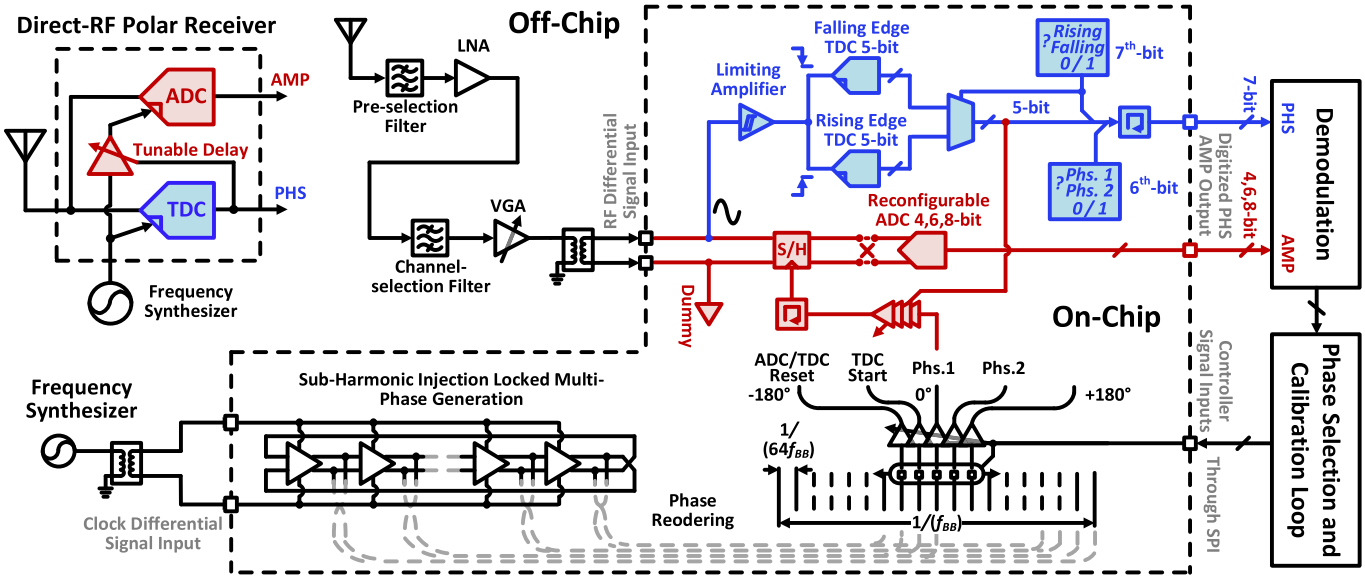


Fig. 7. Proposed polar RX architecture with direct-RF data conversion using a TDC/ADC based RF-to-digital polar data converter.

The PHS detection path contains a limiting amplifier and two TDCs. The limiting amplifier filters out the amplitude information and only feeds the phase information to the TDC to improve the phase detection accuracy. Two 5-bit TDCs measure the time intervals between the rising or falling edge of the signal and the "phs.1" or the "phs.2" phase generated by the multi-phase reference. The sixth bit is determined by which phase ("phs.1" or the "phs.2") of the multi-phase clock is used. The seventh output bit is determined by which edge (rising or falling edge) of the received signal appears first. The residue of the time interval is further digitized by using the 5-bit TDCs.

The AMP information of the received signal is captured by an ADC module. A reconfigurable ADC provides options of 4-, 6-, or 8-bit outputs. The configurability improves power efficiency under different data rates and different modulation types. A successive approximation (SAR) based hybrid ADC architecture is adopted based on the speed and power consumption constraints. The ADC sampling position is adaptively tuned by using tunable delay cells controlled by the detected PHS information.

The period of an RF signal at 6 GHz is around 160 ps. In order to distinguish the phase difference and reconstruct the constellation points from the received RF signal, the TDC resolution needs to be finer than 5 ps. It needs to put great efforts to design a high resolution TDC with large detectable range and good linearity performance [33]–[37]. Therefore, we decide to use multi-phase reference to segment the PHS detection window in order to relax the requirement of the TDC. Sub-harmonic injection locked multi-phase generation technique is utilized [38], [39], which provides a total number of 64 uniformly distributed phases to cover one baseband symbol period. Phase selection calibration loop (off-chip) scans and compares all the 64 phases with the received signal. Then it picks the phase that is closest to the baseband symbol transition point. The selected phase is further aligned with the transition point by adjusting the tunable delay cells controlled by the loop.

A. Direct RF-to-Digital Conversion

Due to the bandwidth limitation and the filtering effects, the PHS and the AMP of a baseband signal modulated on the RF carrier gradually change from one symbol to another over one symbol period as shown in Fig. 6. To ensure an error free detection, the valid sample positions for both TDC and ADC need to be located within one λ ($\pm\lambda/2$) window centered at the baseband transition point, where λ is the carrier period.

To illustrate the sub-sampling direct-RF polar conversion procedure, a 16-QAM modulated RF signal, operating at 6.4-GHz carrier frequency and 400-MS/s baseband symbol rate is used as an example and is presented in Fig. 8 for illustration. A 16× ratio is chosen between baseband and carrier frequency in order to achieve a high data rate throughput. The baseband symbol period ($1/f_{\mathrm{BB}} = 1/400$ and MS/s $= 2.5$ ns) is evenly segmented by 64 uniformly distributed phases generated by the sub-injection locked multi-phase clock generator, among which five adjacent phases are selected by the phase selection calibration loop.

Let us take one of the symbol M as an example and zoom-in to the narrow detection window centered at the boundary between the two adjacent symbol $M - 1$ and M to see how the proposed conversion system works. The first step is the multi-phase clock alignment. One carrier cycle (1/6.4 GHz) is segmented into four pieces by the five adjacent phases from the multi-phase generator. The phase selection calibration loop aligns the center phase (third) to the baseband transition point of the received signal. The first phase is used to reset the ADC and the TDC. The second phase is a start signal for the TDCs. The following two phases (annotated as "phs.1" or "phs.2" in Fig. 8) are used to determine the PHS information of the received signal and to set the sampling point for the AMP detection.

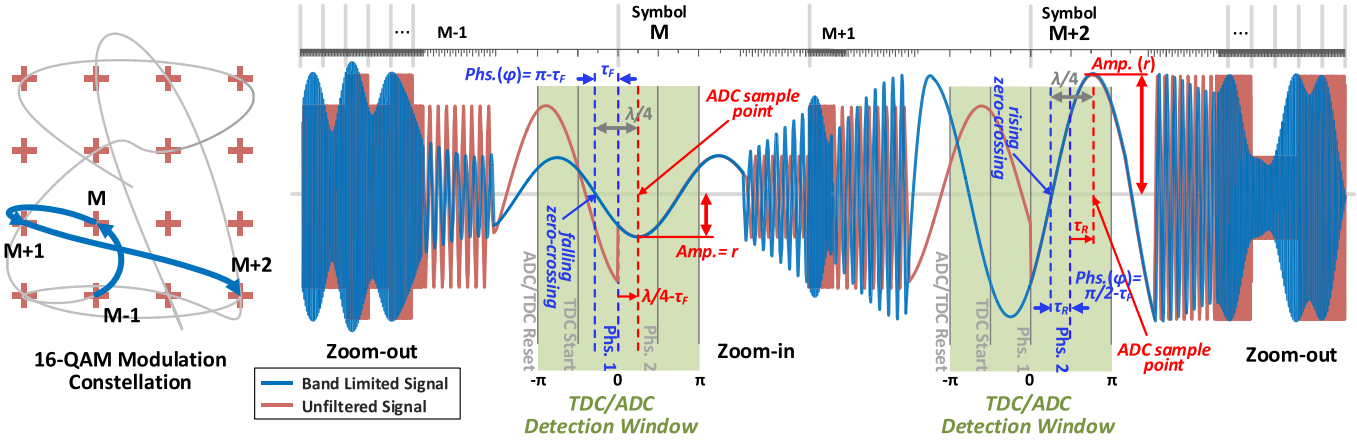


Fig. 8. Illustration of conversion procedure of the proposed direct RF-to-digital sub-sampling converter with 16-QAM modulation signal.

After the reference clock alignment, we split the received signal and feed them into two paths, the PHS path and the AMP path. In the PHS path, after the amplitude limiting amplifier, two identical TDCs are implemented and are triggered by the rising and falling zero-crossing points of the received signal respectively. They measure the time interval between the first zero-crossing point of the received signal inside the detection window and the "phs.1" or the "phs.2" of the multi-phase reference. For symbol M, as shown in Fig. 8, the TDC measured time interval is between the falling zero-crossing point of the received signal and the "phs.1" reference clock noted as "τ_F." Because the zero-crossing point is located ahead of the center of the carrier period, the PHS of symbol M is resolved as "$\pi - \tau_F$." As for symbol M + 2, the first zero-crossing point after the TDC start phase is a rising zero-crossing point. The TDC measured time interval is between the rising zero-crossing point of the received signal and the "phs.2" reference clock noted as "τ_R." Thus, the PHS of symbol M + 2 is resolved as "$\pi/2 - \tau_R$."

The time interval "τ_R" and "τ_F" are measured by the two 5-bit 2-D Vernier TDCs. Their resolution and NoB of the two TDCs are designed to be 2 ps and 5 bits covering a range of 64 ps. The two most significant bits (MSBs) of the PHS correspond to the polarity and phase wrapping of the "τ_R" and "τ_F" and are obtained as follows: the seventh bit is 1 when the rising edge TDC revolves the result "τ_R" first, otherwise, the result is 0; the sixth bit is 1 when the "phs.1" clock is used for comparison, otherwise, the result is 0.

Once the PHS information is resolved, it is time to process the AMP part of the received signal. The AMP of a symbol is represented by the magnitude of the waveform's peak point within one symbol period, which occurs at the time either $\lambda/4$ prior to or after the detected zero-crossing point. The ADC sampling position is then determined by the captured PHS. According to the PHS information, one of the phases "phs.1" or "phs.2" is selected as a reference point. The ADC sampling position is adjusted by the tunable delay cells to $\lambda/4$ later than the measured zero-crossing point. After the AMP information is resolved, the constellation point is reconstructed.

However, when dealing with denser modulation types, for instance, 64-QAM or higher, the PHS/AMP's error tolerance

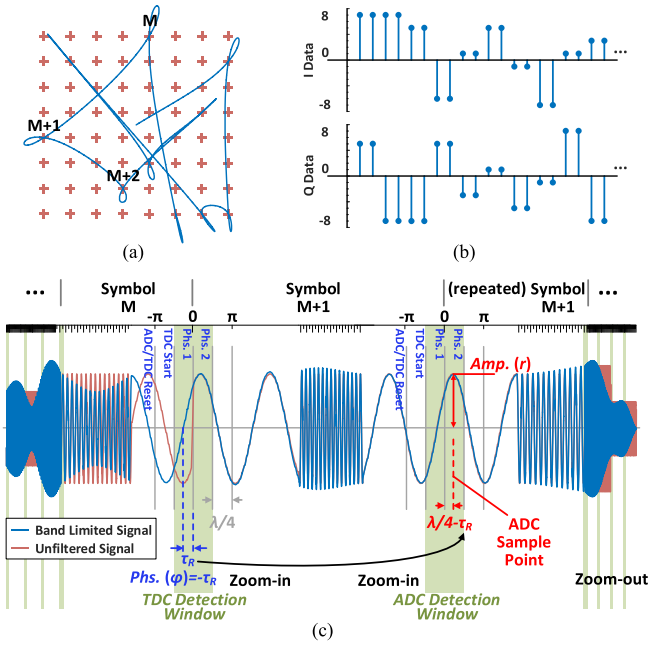


Fig. 9. Redundant signal transmission (twice per symbol) for high data rate dense modulations using the proposed direct RF-to-digital sub-sampling converter. (a) Constellation. (b) Baseband I/Q data. (c) Detection procedure.

requires a narrower detection window of $\pm\lambda/4$. In order to place the sampling points within the $\pm\lambda/4$ detection window, AMP detection may need to happen before the PHS detection is completed. Therefore, one possible solution is to transmit identical symbols twice as shown in Fig. 9. The first cycle is used for PHS detection and the result is used to adjust the sampling point for AMP detection in the second cycle. Note that only one ADC sample is needed per symbol due to the TDC assisted amplitude sample point adjustment. In this design, an equivalent 200-MS/s symbol rate is achieved, which is only limited by the sample rate of the ADC. A sub-sampling process is thus applied to the modulated RF signal to detect the baseband information without the need for down-conversion and anti-aliasing filtering. Without the TDC, RF direct sampling would require an ultra-high-speed ADC sampling at multiple of the carrier frequency.

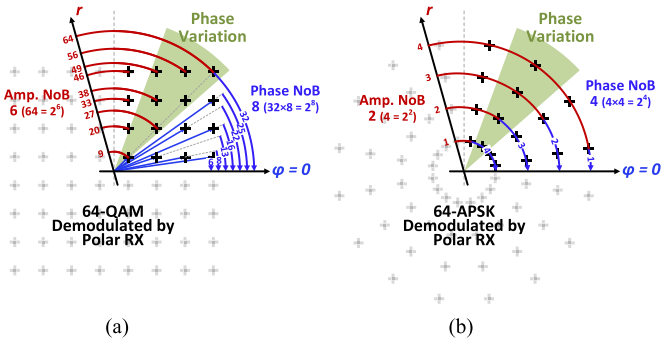


Fig. 10. Comparison between (a) conventional I/Q based QAM modulation and (b) polar based APSK modulation.

B. Amplitude Phase Shift Keying Modulation

The next generation wireless standards call for highly complexed modulations to achieve high data throughput. Complex modulations such as 256-QAM and 1024-QAM put stringent requirements on the phase noise of the local oscillator (LO) and the PLL, the linearity of the power amplifier (PA) and the sample rate, as well as the dynamic range of the ADC. Even with the best effort, the state-of-the-art PLLs [40]–[45] and PAs [46]–[48] can barely support modulations like 1024-QAM, which greatly shrink the margin to tolerate other system impairments such as I/Q imbalance and gain mismatches encountered in conventional Cartesian based TRX. However, these requirements are much relaxed in polar based TRX with constellation arranged in a polar coordinate fashion. Fig. 10 compares the constellations between Cartesian based QAM modulation and polar-based amplitude phase shift keying (APSK) modulation.

The error span due to phase noise and nonlinear distortion is proportional to the distance between the origin and the constellation point. For the QAM modulation, the outer constellation points are much more sensitive to phase variations, as well as nonlinear distortions compared to the inner points. On the other hand, the APSK modulation can tolerate the same amount of phase noise regardless of its amplitude and thus has better power and hardware efficiency, as well as impairment tolerance when implemented in polar systems. The proposed architecture can detect both QAM and APSK modulation signals. However, QAM constellation is designed for classic Cartesian coordinates based on I/Q TRX, while APSK is arranged in polar coordinate, which requires less NoBs in a polar based TRX system. The required minimum NoBs to represent the 64-QAM and 64-APSK are quite different. From Fig. 10, we can clearly find out that 64-QAM needs at least 6 AMP bits and 8 PHS bits, while the 64-APSK needs only 2 AMP bits and 4 PHS bits in the polar based TRX system. Notice that a conventional I/Q TRX system is inefficient to transmit APSK modulation signals. While the polar TX is ready to use, a polar based RX is indispensable if one wants to take advantage of the polar based modulations such as APSK.

C. Circuit Design Details

We discuss in this section the circuit design details for the two critical modules of the proposed RDC system: the TDC

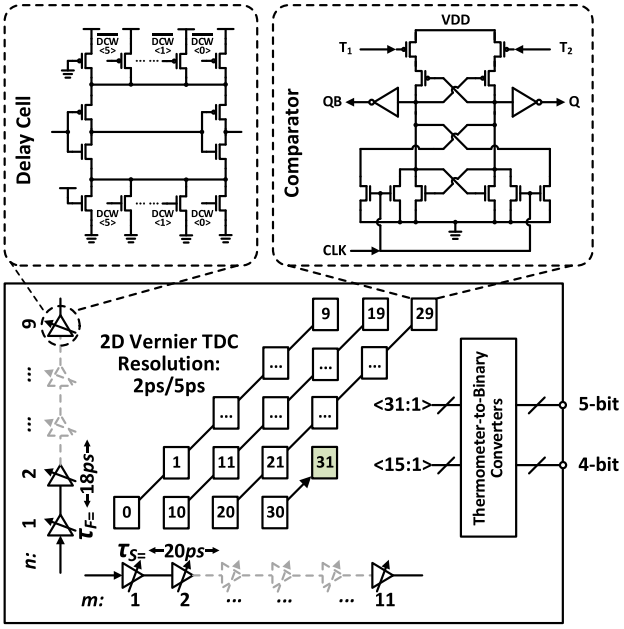


Fig. 11. Block and circuit diagrams of the 2-D Vernier TDC used for phase detection.

used in the PHS detection path and the ADC used in the AMP detection path. Two identical TDCs are implemented for PHS detection. In order to distinguish the phase difference without the down-conversion, the TDC resolution needs to be finer than 5 ps, while the detection range needs to cover at least 1/4 of one carrier frequency cycle λ. To fulfill the high data rate requirement, the maximum conversion rate of the TDC needs to be higher than 400 MS/s.

A wide variety of TDC types have been developed over the years [49]–[52]. Single line TDC, also known as flash TDC, is one of the simplest TDC architecture. It quantizes the input time interval information using a single chain of delay cells and has been adopted by many applications. Although it can be easily implemented and has high conversion speed, its time resolution is limited by the CMOS gate delay, which is sensitive to process–voltage–temperature (PVT) variations. Vernier TDC formed by two delay chains with slightly different delays can achieve sub-gate delay resolution with improved linearity since the first-order mismatches are automatically canceled. However, its detectable range and conversion rate are greatly limited due to the reduced conversion step size. Consequently, a large number of delay stages are needed to cover the detection range, resulting in high power consumption.

Evolving from the Vernier TDC, a 2-D Vernier TDC achieves fine resolution, wide detection range, high conversion speed, and low power consumption simultaneously [53]–[55]. It has the most balanced performance and meets most of the requirements in our proposed polar conversion system. The adopted 2-D Vernier schematic is given in Fig. 11. The resolution is tunable between 2 (5-bit) and 5 ps (4-bit) by adjusting the delay of the delay cells and the arrangement of the comparator array. The schematic of the comparator is also given in Fig. 11. A high-speed dynamic latch topology is adopted to achieve fast response time and accurate

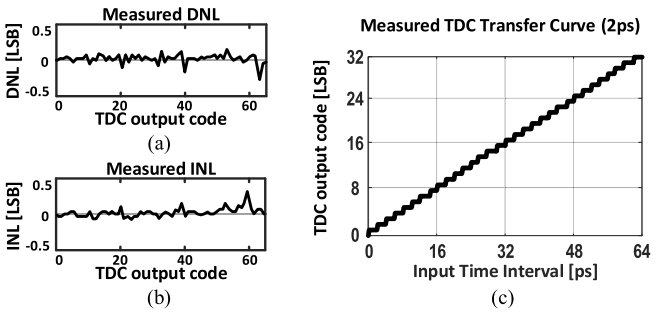


Fig. 12. Measurement results of the 2-D Vernier TDC, including TDC nonlinearity (a) DNL and (b) INL, and (c) TDC transfer curve.

comparison when dealing with time difference in the range of 1 ps [51], [56].

The nonlinearity of the TDC is a critical issue in 2-D Vernier architecture. It mainly comes from the turning points in the comparator array [54]. Minimizing the temporal delay error of the delay units is the prerequisite for its linearity improvement. The unit delay cell in the delay chain comprises a pair of cascaded inverters as shown in the up-left corner of Fig. 11. To reduce the mismatch, both fast and slow delay chains were implemented with identical unit delay cells. In this design, the unit delay cell is tunable with six digitally controlled bits to obtain digital calibration compatibility and also meet tuning requirements against PVT variations. The six delay tuning bits are constructed with six pairs of NMOS and PMOS transistors sized with binary weights. The first and second least significant bits (LSBs) of the tuning bits share the same transistor pair. A pair of keep-life NMOS and PMOS transistors are connected in parallel with delay tuning transistor pairs. The median value of the delay tuning range can be varied during the circuit design by adjusting the size ratio between keep-life transistors and the tuning transistors. The delay calibration mitigates the nonlinearity associated with the turning points in the comparator array. Although additional methods are introduced in [54] to further enhance the linearity, the performance improvement is hard to pay back the increment of design complexity. In order to meet the system requirement with minimum cost, the detection range of the TDC has been reduced to 1/4 of one carrier cycle. A multi-phase reference with total of 64 phases is, therefore, applied to the system to aid the TDCs for phase acquisition.

The TDC standalone performance is measured and summarized in Table I. A 2-ps resolution is achieved with maximum conversion speed of 440-MS/s sample rate. Its nonlinearity plots, including the integral nonlinearity (INL), differential nonlinearity (DNL), and overall transfer curve are given in Fig. 12. With the aid of multi-phase reference, the TDC detection range is reduced, which leads to a better linearity performance. The maximum INL and DNL with 2-ps resolution are 0.31 LSB and 0.28 LSB, respectively.

In the AMP detection path, there are multiple choices when deciding the architecture of the ADC as well [8], [57]–[63]. The RDC requires the ADC with 4–8 bits programmable conversion range and at least 400 MS/s rate with low power consumption. Among all the ADC architecture candidates, SAR based ADCs are chosen to meet the

TABLE I
TDC SPECIFICATIONS AND MEASUREMENT RESULTS

Resolution / NoB	2ps / 5bit	5ps / 4bit
ENoB [bit]	4.61	3.63
INL [LSB]	0.31	0.29
DNL [LSB]	0.28	0.21
Max speed [Msps]	440	350
Power consumption [mW]	0.73	0.47
FoM [pJ / conv-step]	0.05	0.08

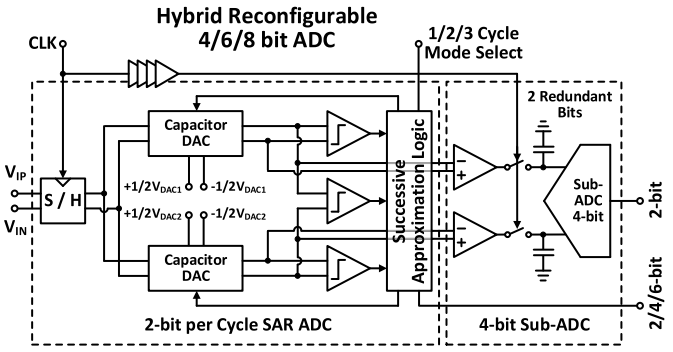


Fig. 13. Block diagram of the hybrid reconfigurable ADC for amplitude detection.

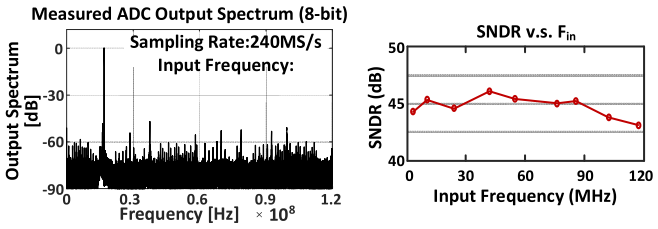
system specifications. The primary advantages of SAR ADCs are high power efficient, high resolution, and good linearity performance. In addition, the SAR ADC can be easily configured to output different NoBs by adjusting the number of conversion cycles.

Although SAR ADCs have many good characteristics, the conversion speed is its major drawback. Compared to flash ADCs or pipeline ADC, which can resolve all the conversion bits within one cycle, the SAR ADC requires multiple cycles to accomplish the conversion. For a single SAR ADC, the number of conversion cycles is proportional to the NoBs, which leads to a relatively low conversion rate. In order to support a higher data rate, we need a faster data converter. In the proposed RDC system, we employ a hybrid scheme given in Fig. 13 that combines a 2-bit per cycle SAR ADC with a 4-bit flash ADC connected in two pipeline stages. Two redundant bits in the flash ADC stage are added for calibration and accuracy improvement. The topology with a 2-bit per cycle SAR-ADC and a pipeline architecture greatly increases the overall conversion speed without introducing complicated techniques. The adopted ADC is also reconfigurable by controlling the number of SAR conversion cycles to produce 4-, 6-, or 8-bit output, respectively. The reconfigurability allows improved power efficiency for the detection of different modulations at various data rates.

The hybrid ADC was tested individually. A maximum sampling rate of 280 MS/s is achieved with the 8-bit configuration. ADC's linearity is also critical to the overall performance. Two commonly used indicators, signal-to-noise distortion ratio (SNDR) and effective NoB (ENoB) are measured and summarized under different output bit configurations in Table II. The ADC's number of output bits is configurable by removing

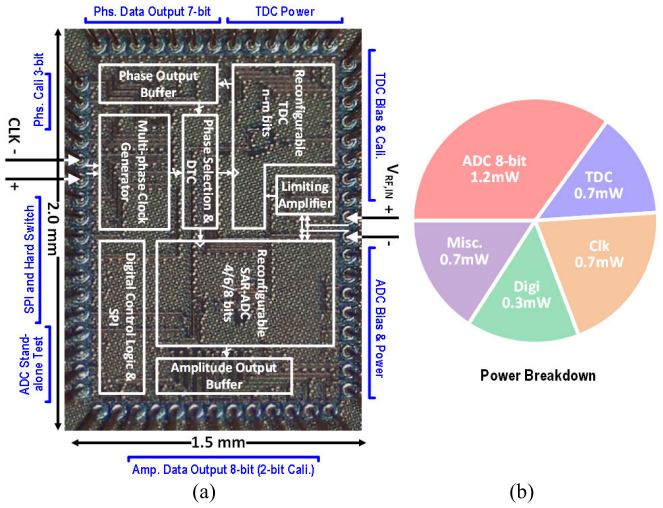
TABLE II
ADC SPECIFICATIONS AND MEASUREMENT RESULTS

NoB [bit]	4	6	8
SNDR (9.7MHz f_{in}) [dB]	22.8	34.5	45.6
SNDR (104.3MHz f_{in}) [dB]	21.6	32.1	43.3
ENoB [bit]	3.50	5.44	7.28
Max Speed [Msps]	440	320	280
Power consumption [mW]	0.78	0.95	1.22
FoM [pJ / conv-step]	137.3	146.8	156.2



(a) (b)

Fig. 14. Measurement results of the hybrid reconfigurable ADC, including (a) output spectrum and (b) SNDR versus input frequency.



(a) (b)

Fig. 15. (a) Die photograph of the proposed RDC RFIC prototype with a detailed module floor plan. (b) Power breakdown of the prototype.

the second pipelined stage and by controlling the number of SAR conversion cycles to produce 4, 6, or 8 digital output bits. A total of 7.28 bits of ENoB is achieved with a maximum sampling rate of 280 MS/s. One of the measured ADC output spectrum plots and SNDR to input frequency plot are presented in Fig. 14, indicating a good linearity performance across the entire Nyquist band.

IV. MEASUREMENT RESULTS

The prototype was implemented in 45-nm CMOS technology with an overall die area of 2×1.5 mm^2. Fig. 15(a) presents the die micrograph of the prototype with the detailed floor plan of the chip. The power breakdown chart is included on the right side of Fig. 15(b) to reveal the contributions of each building block to the overall power consumption. The evaluation board and measurement setup for constellation

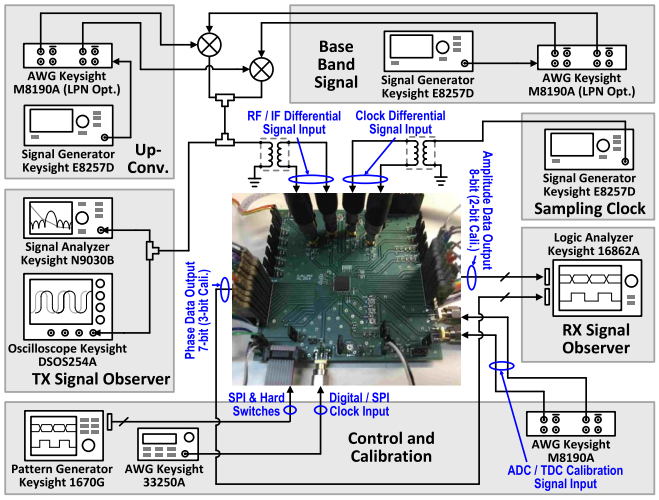


Fig. 16. Measurement setup of the proposed RDC system.

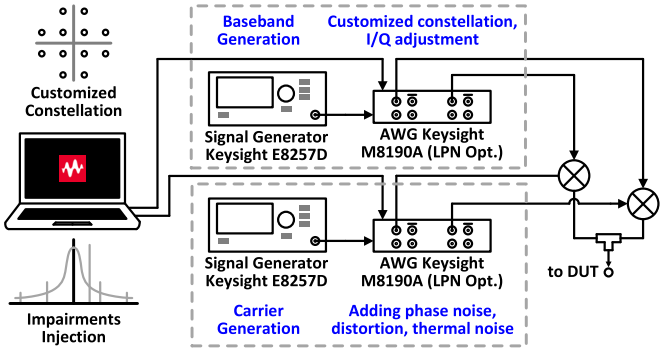


Fig. 17. Customized constellation and impairments (phase noise, nonlinear distortion, thermal noise, and blocker) injection setups.

reconstruction and the receiver bit error rate (BER) test are shown in Fig. 16. Massive measurements were taken to compare the performances between QAM and APSK modulations using the proposed direct-RF sub-sampling polar RDC in the presence of commonly seen impairments: phase noise and nonlinear distortion. A Keysight arbitrary waveform generator (AWG) M8190A was used to generate the modulated baseband signal with customized constellation. External signal source option (low phase noise (LPN) option) on the AWG was enabled to achieve high phase noise purity. An E8257D signal generator (SGN) was used as the external signal source for the M8190A. Another pair of AWG and SGN was used to generate the carrier frequency. Fig. 17 provides a detailed measurement setup. Random phase noise, nonlinear distortion, thermal noise, and blocker were added intentionally onto the modulated signal by using the AWG.

Although the proposed RDC system is capable of detecting both QAM and APSK waveforms, QAM modulation is shown to be more sensitive to practical impairments with denser constellation modulation types. The BER was measured to compare different complex modulations under a default testing condition of 6-GHz carrier frequency, 6-dBm signal power, 375-MHz signal bandwidth, 375-MS/s sample rate, and 0.35 roll-off factor (α). As expected, both the 64- and 1024-APSK outperform the 64- and 1024-QAM modulations

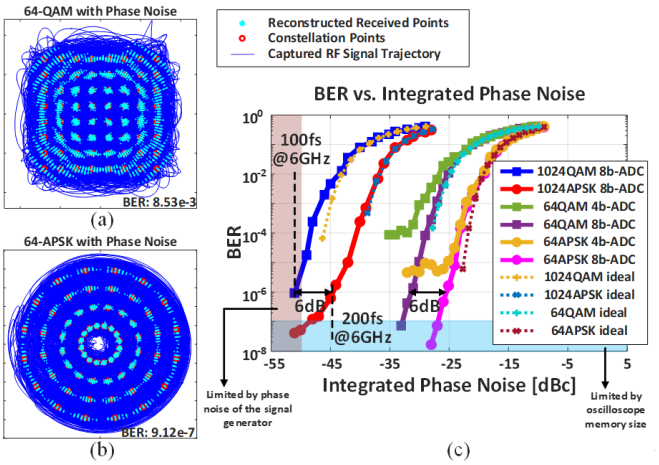


Fig. 18. Comparison of (a) 64-QAM and (b) 64-APSK modulations with phase noise. (c) Measured 64/1024-QAM and 64/1024-APSK BER versus phase noise. Testing condition: carrier frequency 6 GHz, BW 375 MHz, sample rate 375 MS/s, roll-off factor 0.35, and no additional distortion, blocker, and thermal noise applied.

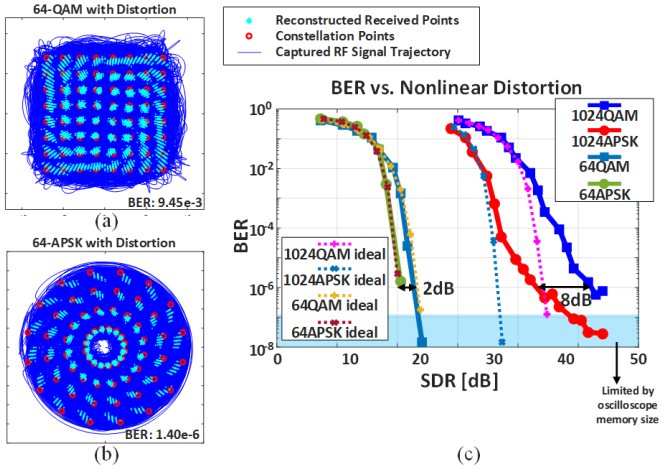


Fig. 19. Comparison of (a) 64-QAM and (b) 64-APSK modulations with distortion. (c) Measured 64/1024-QAM and 64/1024-APSK BER versus nonlinearity distortion (characterized in SDR). Testing condition: carrier frequency 6 GHz, BW 375 MHz, sample rate 375 MS/s, roll-off factor 0.35, and no additional phase noise, blocker, and thermal noise applied.

with the presence of phase noise or nonlinear distortion characterized in signal-to-distortion ratio (SDR). According to the measurement results presented in Figs. 18 and 19, in order to achieve the same BER number, both the 64- and 1024-APSK modulation relaxes the phase noise requirement by 6 dB compared to their 64- and 1024-QAM counterparts, while the nonlinearity requirement was relaxed by 8 and 2 dB for 1024-APSK and 64-APSK modulation schemes, respectively. When converting the integrated phase noise from dBc to rms jitter in femtosecond (fs), the requirement is relaxed from 100 to 200 fs for a carrier frequency signal around 6 GHz, which greatly reduces the phase noise requirement and design complexity of the TRX LO generation units.

Some imperfections of the polar based RDC and the APSK modulation have been revealed during the testing. Compared with QAM modulation, APSK is more sensitive to thermal noise due to its divergent lattice. Fig. 20 reveals the differences

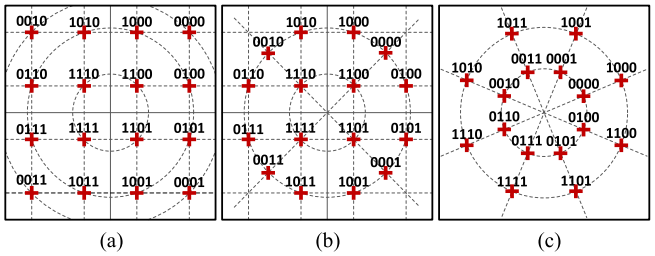


Fig. 20. Constellation arrangement comparison among (a) conventional QAM constellation, (b) APSK constellation Type-I commonly adopted in I/Q TRX systems, (c) APSK constellation Type-II compatible with polar TRX systems.

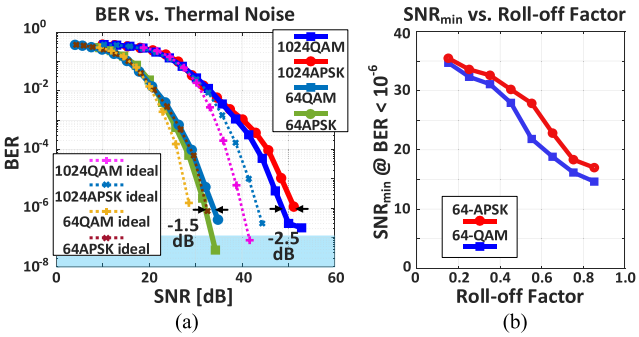


Fig. 21. (a) Relaxation in SDR and phase noise requirements are partially compromised by required higher SNR. Testing condition: carrier frequency 6 GHz, BW 375 MHz, sample rate 375 MS/s, roll-off factor 0.35, and no additional phase noise, blocker, and thermal noise applied. (b) Minimum SNR requirement for BER less than 10^{-6} versus roll-off factor of the raised cosine filter.

among conventional QAM constellation and two types of APSK constellation arrangements. As shown in Fig. 20(a), all the points in QAM constellation are equally distributed with a unified distance between every two points. Fig. 20(b) gives one type of APSK (Type-I), which is commonly adopted in I/Q based TRXs. In this arrangement, most of the points are still on the I/Q lattice, while the rest of the points are forced to the closest amplitude circles, leading to an unevenly distributed phase between each point. Another APSK constellation (Type-II) with an evenly distributed phase is presented in Fig. 20(c), which is suitable for the proposed polar RX. In Type-II, the minimum distance between those points in the inner circle is smaller. Consequently, the Type-II APSK requires higher SNR than QAM to achieve the same BER, especially when larger M-ray is applied. The measurement results are presented in Fig. 21(a). As expected, the relaxation in SDR and phase noise are partially compromised by higher SNR requirement. However, as explained in previous sections, a Cartesian based QAM modulation requires greater NoBs to resolve the information in the polar domain and results in a degraded performance in practice. The minimum SNR level to reach a BER level lower than 10^{-6} from QAM to APSK are increased by 1.5 and 2.5 dB for M-ary 64 and 1024, respectively. The deviation between measurement and theoretical results mainly comes from finite TDC and ADC resolutions, namely quantization noise.

Blocker tolerance is another major challenge for both polar and direct-RF receiver architecture. The performance of the

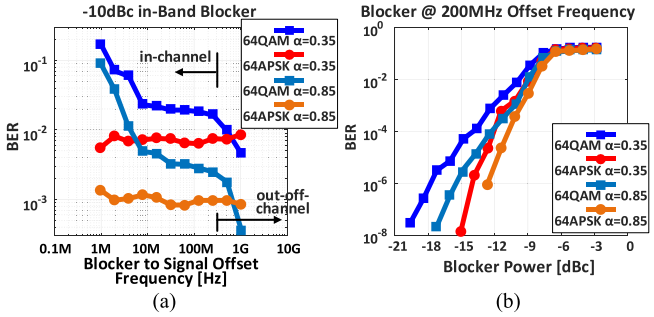


Fig. 22. Comparison of in-band blocker tolerance between APSK and QAM modulations with (a) fixed −10-dBc blocker and (b) fixed 200-MHz offset. Testing condition: carrier frequency 6 GHz, BW 375 MHz, sample rate 375 MS/s, and no additional phase noise, distortion, and thermal noise applied.

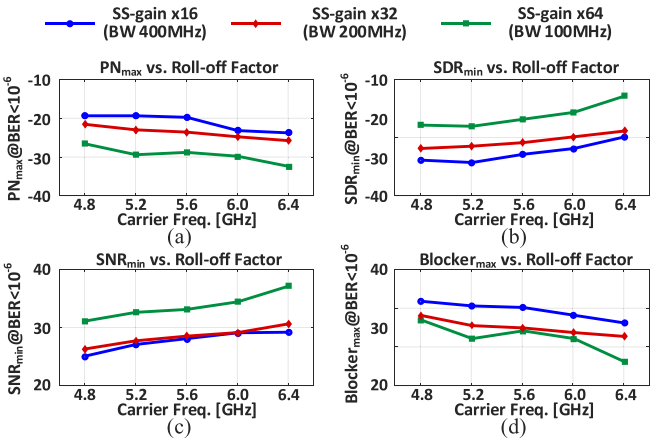


Fig. 23. (a) Phase noise, (b) nonlinearity, (c) thermal noise, and (d) blocker tolerance requirement versus signal bandwidth and carrier frequency with a fixed roll-off factor of 0.35.

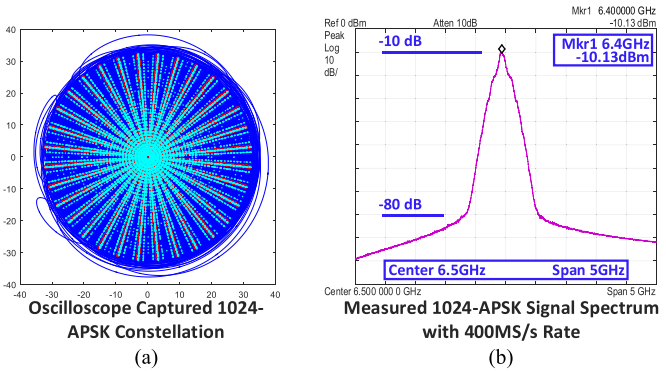


Fig. 24. (a) 6.4-GHz 400-MS/s 1024-APSK modulated waveform with 5 amplitude bits and 5 phase bits. Oscilloscope captured RF modulated signal from the SGN and the recovered data points by the proposed RDC chip and (b) measured RF modulated spectrum.

proposed RDC without any filtering effect is evaluated in this work. According to Fig. 22(a), both APSK and QAM have mediocre blocker tolerance performances when feeding a 6-dBm input signal and a −10-dBc in-band blocker into the RDC. However, it shows that APSK's BER is approximately independent of the blocker's offset frequency and is lower than that of the QAM signal when the blocker is in the channel and overlapped with the wanted signal, which indicates a better out-of-band blocker inter-modulation tolerance. Moreover, the BER versus blocker power measurement with a blocker signal fixed at 200-MHz offset frequency is presented in Fig. 22(b) showing that the decay of the APSK error is much faster than the error of the QAM as the power of the in-band blocker declines. These comparisons legitimate the use of polar modulated data receiving and proposed RF-to-digital conversion scheme in a condition where channel selection filtering techniques are applied or in a single-channel application without any significant interference.

The imperfections mentioned above can be relieved by adjusting the roll-off factor α of the raised cosine filter at the transmitter side. Additional measurement was arranged to analyze the impact of the roll-off factor. A greater roll-off factor helps the receiver to achieve a BER of 10^{-6} with a reduced minimum SNR requirement and a better blocker tolerance performance, as presented in Figs. 21(b) and 22, respectively. A higher roll-off factor also simplifies the hardware in a filter but asks for additional spectrum bandwidth. A tradeoff among performance, hardware, and bandwidth need to be balanced for different applications.

The receiver performance is affected by the signal bandwidth as well. The bandwidth of the proposed RDC is related to sub-sampling gain (SS-gain), which is defined as the ratio of carrier frequency and the baseband rate. Although a large SS-gain can minimize the deviation on phase and amplitude during the sampling, higher carrier frequency or lower signal bandwidth is required. One option leads to extra complexity and power consumption, the other reduces the data rate. Phase noise, nonlinearity, thermal noise, and blocker tolerance are measured with different signal bandwidth and carrier frequency as presented in Fig. 23.

The proposed RDC system supports up to 1024-APSK modulations for high data rate applications. The transmitted 1024-APSK modulated signal was captured by the oscilloscope and is presented with the reconstructed digital data points captured at the output of the RDC chip in Fig. 24(a). Its spectrum plot is given on the right. For the 1024-QAM or APSK modulation, it has a total of ten bits to represent one symbol on the constellation space. In the conventional I/Q based 1024-QAM modulation, 5 bits are placed in the I channel, and another 5 bits are placed in the Q channel. However, for 1024-APSK, different bit partitions can be used to form the constellation space. It is desirable to understand the effect of bit partitions on system BER performance.

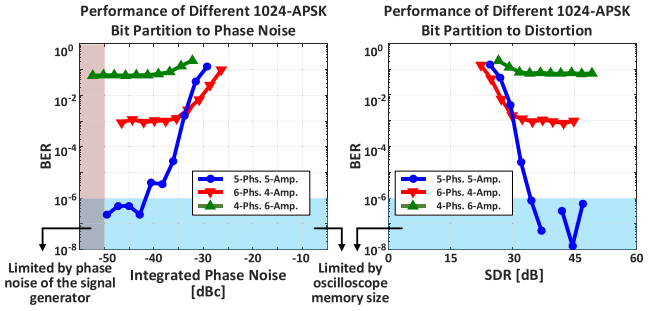
According to the results shown in Fig. 25, for 1024-APSK modulation, the bit partition for PHS and AMP data greatly affects the data link performance. It can be observed that the equal partition of PHS and AMP bits (5-PHS and 5-AMP) has a better performance in general compared to other configurations with the same total NoBs. However, when large phase noise or nonlinear distortion is present, using more bits for the PHS part (e.g., 6-PHS and 4-AMP) achieves better BER performance, indicating phase data has better tolerance on phase noise or nonlinear distortion.

The performance of the proposed RDC direct RF sampling architecture has been summarized and compared with

TABLE III
PERFORMANCE SUMMARY COMPARISON

Parameter	This Work					[2] JSSC 15	[3] JSSC 16	[64] JSSC 14	[65] JSSC 17
Topology	45 nm CMOS					65 nm CMOS	28 nm CMOS	65 nm CMOS	40 nm CMOS
Die size [mm^2]	3.0					2.0 (core)	1.0	5.9	8.6
Supply voltage	1.1 V					1.0 V	1.8 V	1.2 V	3.3 V
Architecture	Polar based RF sub-sampling					RF sampling	RF sampling	RF processing	Super-heterodyne
Support modulation	QAM and APSK					Impulse	QAM	QAM	QAM
Tested modulation	64-QAM	64-APSK	256-QAM	256-APSK	1024-APSK	Impulse	256-QAM	16-QAM	256-QAM
Input freq. [GHz]	6.2(1)	6.8(1)	6.1(1)	6.4(1)	6.2(1)	Up to 12	1	0.5~3	2.4 / 5.0
Sample rate [GS/s]	0.387	0.425	0.38	0.40	0.388	666	2.7	0.1 (ADC)	-
Data rate [Gb/s]	1.16	1.28	1.52	1.60	1.94	-	10	0.008	0.054
ADC ENoB	7.27 bit					7.3 bit	12 bit (NoB)	12 bit (NoB)	-
TDC ERes.(2)	2.62 ps					10.5 ps(3)	-	-	-
Max. in-band blocker power	-4 dBm					-	-	-1 dBm	6.7 dBm
Power [mW]	3.7	4.0	3.6	3.8	3.8	46.7(4)	300(5)	250~600(5)	179(5)

1. Maximum input frequency with BER < 10^{-8}.
2. Effective Resolution (ERes) = resolution×(INL$_{MAX}$+1)
3. Digital-to-Time Converter (DTC) resolution
4. Equivalent parts total power
5. Including PLL power consumption



(a) (b)

Fig. 25. Measured BER performances of different phase and amplitude bit partitions for a 1024-APSK modulated signal with (a) different phase noise and (b) nonlinear distortion. Testing condition: carrier frequency 6 GHz, BW 375 MHz, sample rate 375 MS/s, roll-off factor 0.35, and no additional blocker, and thermal noise applied.

other recently reported state-of-the-art designs in Table III. It demonstrates that our proposed RDC architecture provides a promising candidate for direct RF-sampling receivers.

V. CONCLUSION

A low power direct RDC for wireless polar receivers is presented in this article. The RDC architecture and its operational principle have been discussed. In conjunction with an existing polar transmitter, the proposed polar receiver enables the highly efficient polar signal conversions with APSK modulations. This RDC can not only work for conventional QAM modulations, but also for APSK modulations with even better power efficiency as well as phase noise and nonlinearity tolerance. Comparing with QAM modulations, APSK modulated signal relaxes the requirements of phase noise and linearity in the TRX system by 6 and 8 dB, respectively using the proposed polar converter. This design is competitive with a variety of modulation types (QAM, PSK, APSK, and so on) and achieves a maximum data rate of 1.94 Gb/s with 1024-APSK modulation at a carrier frequency of 6 GHz. Moreover, unlike other direct-RF converters, the proposed conversion system samples the input RF signal at baseband frequency and consumes a maximum power of 3.8 mW only.

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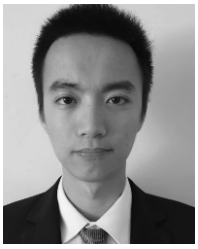

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