



Performance of a Low–Parasitic Frequency–Domain Multiplexing Readout

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Abstract

Frequency-domain multiplexing is a readout technique for transition-edge sensor bolometer arrays used on modern cosmic microwave background experiments, including the SPT-3G receiver. Here, we present design details and performance measurements for a low-parasitic frequency-domain multiplexing readout. Reducing the parasitic impedance of the connections between cryogenic components provides a path to improve both the crosstalk and noise performance of the readout. Reduced crosstalk will in turn allow higher-multiplexing factors. We have demonstrated a factor of two improvement in parasitic resistance compared to SPT-3G hardware. Reduced parasitics also permits operation of lower-resistance bolometers optimized for improved readout noise performance. We demonstrate that a module in the prototype system has comparable readout noise performance to an SPT-3G module when operated with dark TES bolometers in the laboratory.

Keywords Frequency-domain multiplexing · Transition-edge sensors · Cosmic microwave background

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NbTi striplines encapsulated in Kapton and ultrasonically soldered to the LC circuit board on one end and to a breakout circuit board that connects to the SQUID circuit board on the other end [10]. This 60–75-cm-long wiring (shown in thick, red lines in Fig. 1) allows the SQUID chip to operate on the 4 K stage, physically and thermally distant from the LC filters.

A significant source of crosstalk in the cryogenic portion of the readout comes from parasitic impedance in this wiring, which sets up a voltage divider. As the resistance of each bolometer varies according to deposited sky power, the ratio of the voltage divider is modulated, changing the voltage bias across the LC-TES network. This changes the TES resistances across the module that mimic those due to optical power deposition. The level of crosstalk is directly proportional to both the AC bias frequency and the inductance of the wiring [11]. The SPT-3G hardware mitigates this effect by logarithmically increasing the spacing between resonances with increasing bias frequency [12]. Reducing the inductance and suppressing this crosstalk will support future implementations with denser resonant frequency spacing and increased multiplexing factors.

Additionally, stable operation of detectors requires the parasitic impedance to be small relative to the TES resistance [13]. Under these conditions, the applied voltage bias enables negative electrothermal feedback, stabilizing the TES in the superconducting transition. The impedance sourced by the LC-SQUID wiring contributes to this parasitic, setting an effective lower limit to the resistance of the TES. The intrinsic readout noise current in the DfMux system is referred to power fluctuations on the TES (noise equivalent power) via the responsivity, which is inversely proportional to the voltage bias amplitude [11]. Operating bolometers at lower resistances requires lower voltage biases, opening up a larger region of parameter space in which bolometer resistance can be optimized to improve readout noise performance. In the current DfMux system, the optimal bolometer resistance for readout noise performance is typically in the 0.5–1 Ω range, a factor of a few lower than SPT-3G bolometers.

The primary goal of this work is to develop a modified DfMux architecture which minimizes the parasitic impedance of the wiring between the LC filters and the SQUID. This will reduce crosstalk, as well as take a first step toward the operation of lower-resistance bolometers and improved readout noise performance.

3 Design

The wiring between the SQUID and the LC chip should be as short and wide as possible to reduce the parasitic impedance. One straightforward way to achieve this is to move the SQUID from the 4 K stage to the 250 mK stage, onto the same circuit board as the LC chip and to use wide wiring traces. Figure 2 shows photographs of the prototype circuit board (PCB) and hardware, which retains as much of the legacy DfMux design as possible. The objectives of the prototype design are to reduce the parasitic impedance between the LC chip and SQUID, reduce crosstalk, and improve scalability all while inheriting a relatively high level of technological maturity from the existing technology. To that end, the prototype circuit board is identical to the

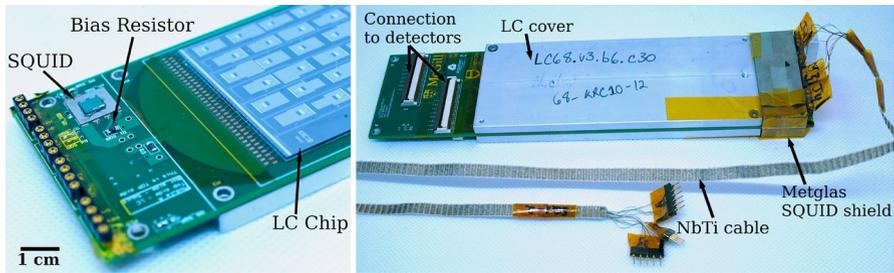


Fig. 2 Left: Partially assembled prototype circuit board showing the SQUID chip, LC chip, bias resistor, and connectors. Right: Fully assembled prototype circuit board showing the Metglas cover for the SQUIDs, aluminum cover for the LC chips, and NbTi twisted-pair ribbon cable which connects the board to a wiring feedthrough at 4 K (Color figure online)

SPT-3G LC board from the input to the LC chip through the connections to the detector wafer. A small extension was added to the input end of the board to accommodate the SQUID chip and its circuitry. This design minimizes the wiring length between the SQUID and LC chips, significantly reducing parasitics from that section of wiring. Additionally, the trace connecting the LC and SQUID has significant width to minimize its inductance. All traces in the circuit board are standard layers of 0.6-mil-thick copper foil. Future implementations of this prototype board could further control the inductance of this trace by controlling layer separation within the circuit board and by tinning the copper layers to enable superconducting traces. A single circuit board houses one LC chip and one SQUID chip on each side. Additionally, the extension to the board is short enough that the prototype hardware fits in every SPT-3G cryogenic testbed (and in principle, in the telescope itself) as a drop-in replacement for the standard SPT-3G DfMux readout hardware. This enables rapid and straightforward testing of the prototype architecture alongside SPT-3G hardware for comparison.

SQUIDs are sensitive magnetometers and require careful magnetic shielding in order to operate optimally as an amplifier [14]. An aluminum box (for mechanical protection) covered with six layers of Metglas [15] (a high-permeability material used for magnetic shielding) covers the SQUIDs (see Fig. 2). Comparison testing has shown that the Metglas box performs as well as an Amuneal [16] box for magnetic shielding in this application [17]. A separate aluminum cover acts as a mechanical shield for the LC chips.

A convenient additional benefit of removing the long wiring between the LC chip and the SQUID chip is that it eliminates a complicated, expensive, and labor-intensive component of the cryogenic wiring. Long wiring is still required to reach from the detector stage to the 4 K stage. However, since the long wiring in the prototype system is between the SQUID output and the warm electronics (instead of between the SQUID and the LC), the impedance of this long wiring does not contribute to crosstalk. Therefore, the technical requirements for this wiring become significantly less restricted. The current prototype uses commercially available niobium–titanium twisted-pair woven loom ribbon cable, hand-connectorized with single inline

package (SIP) socket connectors. Future revisions may use the same ribbon cable with commercially potted connectors for improved scalability.

4 Performance

4.1 SQUID Performance

The prototype system has been tested using SA13 SQUID arrays fabricated at the National Institute of Standards and Technology (NIST). Their performance at sub-Kelvin temperatures is comparable to or slightly better than their performance at more typical operating temperatures of 2 K. Figure 3 (top left) shows a comparison plot of the flux bias versus output voltage for a representative SA13 at three

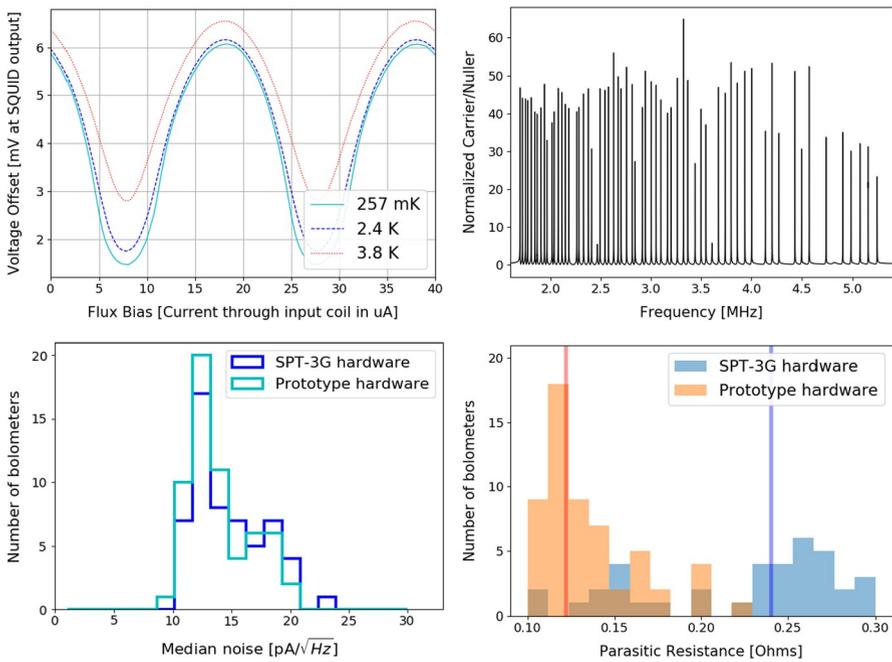


Fig. 3 Top left: Performance of the NIST SA13 SQUIDs is similar across a range of temperatures. Shown here is the flux bias versus the SQUID voltage offset for the same SQUID chip at its optimal (maximal peak-to-peak voltage) current bias. For this SQUID chip, the transimpedance is $Z = 945 \Omega$, $Z = 850 \Omega$, and $Z = 683 \Omega$ at 257 mK, 2.4 K, and 3.8 K, respectively. Top right: Network analysis (carrier signal divided by nuller signal, across the full readout frequency range) of the prototype module showing 63 resonance peaks. Bottom left: A comparison of noise performance for the prototype system and the SPT-3G readout hardware with the detectors. At the prototype system clearly demonstrates comparable performance. Bottom right: Shown here is the parasitic resistance of one module of bolometers on prototype hardware and one module on SPT-3G hardware. The orange and blue vertical lines indicate the medians for the prototype and SPT-3G hardware, respectively. The reduced wiring length between the SQUID chip and LC chip substantially reduces the parasitic resistance in the prototype system compared to standard DfMux readout hardware (Color figure online)

temperatures. The performance of the SQUIDs shows a 38% increase in transimpedance when the operation temperature is lowered from the normal to 257 mK.

Thermal dissipation is also an important consideration when putting SQUIDs on the same thermal stage as detectors. The thermal dissipation of a SQUID can be estimated as the product of the current bias and the voltage offset at the SQUID output. Tuned at a typical operating current—and flux—bias, a single representative SA13 (able to operate one module of bolometers) dissipates about 150 nW of heat onto the detector stage. At this level of thermal dissipation, operating small numbers of SA13s works well, but scaling up to the hundreds of SQUIDs required for operation of a large detector array is not feasible using a typical sorption refrigerator. For example, a Chase Cryogenics [18] gaslight sorption refrigerator provides ~ 1 W of cooling power on the ~ 250 mK stage. For scalability, either a dilution refrigerator or a SQUID with lower thermal dissipation will be required.

4.2 Bolometer Operation and Noise Performance

An SPT-3G detector wafer (retired after observing in 2017) was used for the prototype system characterization and demonstration described in this work [19]. As part of this characterization, both prototype LC/SQUID boards and standard SPT-3G style boards were connected to read out different portions of the detector wafer. Side-by-side measurements with both architectures were performed to enable direct comparisons of the readout system performance. One key performance metric for the stable operation of the TES bolometers is the parasitic resistance in series with them. Resistance is measured by applying small amplitude voltage biases (the carrier) at the resonant LC frequencies. The DAN feedback is enabled and the resistance determined from the ratio of the voltage bias and nulling current amplitude. Measurement of the parasitic resistance is performed holding the detector wafer at a temperature of 250 mK, well below the TES superconducting transition temperature (T_c). Figure 3 (bottom right) compares the parasitic resistance of a prototype and an SPT-3G module. The prototype system clearly demonstrates reduced parasitic resistance (approximately a factor of two). This demonstration of decreased parasitic resistance paves the way to operating lower-resistance bolometers.

Of a possible 66 bolometers connected to this module, 58 should be operable in our current testing configuration. The eight missing bolometers are known flaws on the detector wafer and LC chip, identified by looking for shorts, opens, and missing peaks in the network analysis. A network analysis (carrier signal divided by nuller signal; a tool for identifying working channels and measuring their frequency) showing the LC resonant peaks is shown in Fig. 3. Of the full module of 58 bolometers that can be biased, we have successfully placed 57 into the TES superconducting transition with a operating resistance of $\sim 20\%$ of the normal resistance and held them there with good stability under dark, steady-state conditions. Figure 4 shows resistance versus power curves for a representative selection of bolometers as they are dropped into the superconducting transition. For comparison, under the same conditions, the standard SPT-3G readout hardware was able to operate at no lower than $\sim 30\%$ of the normal resistance before the bolometers became too unstable and the whole module latched

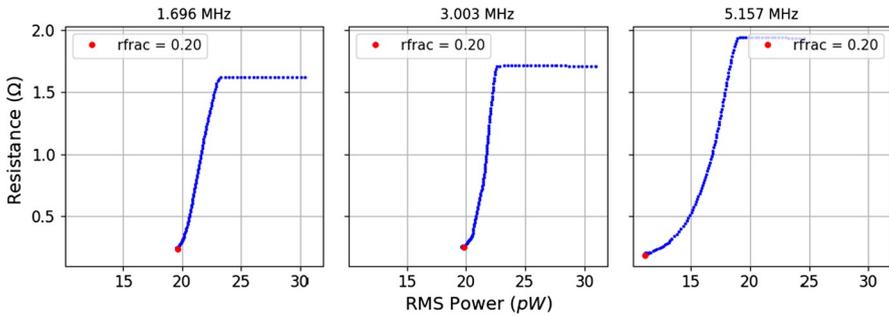


Fig. 4 Operation of a full module of 57 bolometers down to $\sim 20\%$ of the normal resistance has been demonstrated with the prototype. Shown are resistance versus power curves for three representative bolometers as they drop into the superconducting transition. Each bolometer tuning step from maximum bias power down into the superconducting transition is indicated by a small blue dot, and the final tuned point is indicated by a large red dot. These curves have been corrected to remove the parasitic resistance (Color figure online)

superconducting. The improved stability at very low fractional resistances likely results from the decreased parasitic resistance in the prototype system, but more investigation is required to develop a detailed understanding of the performance improvements.

The median noise of the readout system is measured with the detector wafer at a temperature of 650 mK (well above the superconducting transition temperature of the detectors). Additionally, the detector wafer is blanked off with an aluminum cap at the same temperature to minimize optical power and noise. In this configuration the measured noise is dominated by that from the readout system, providing an effective diagnostic of the level of readout noise. The median noise level is measured in the 10–40 Hz band of the resulting amplitude spectral distribution. Figure 3 (bottom left) shows that the noise in the prototype system is comparable to that of the SPT-3G hardware. This is also comparable to the full, fielded readout noise performance of the SPT-3G array [9]. Future studies of the prototype system will characterize the total noise with the detectors operating at various points in the superconducting transition.

While there is not yet a detailed measurement of the parasitic inductance in the prototype system, an estimate based on the geometry of the traces between the SQUID and the LC on the prototype circuit board is 5 nH. From this parasitic inductance value, the effect on crosstalk can be estimated. Reducing the parasitic impedance from that of an SPT-3G-like system (15 nH [10]) to 10 nH, a conservative estimate for the prototype hardware, reduces the wiring impedance crosstalk by a factor of approximately three.

5 Conclusions and Future Work

We have demonstrated operation of a full module of frequency-multiplexed bolometers using a prototype system with parasitic impedance between the LC and SQUID significantly reduced compared to existing systems. Readout noise performance is comparable to that of SPT-3G hardware. NIST SA13 SQUIDs perform well overall at sub-Kelvin temperatures. However, to improve scalability by enabling operation of a large number of SQUIDs on the cold stage, either dilution refrigeration or SQUIDs

with lower thermal dissipation will be required. Finally, we have demonstrated a reduction in parasitic resistance of a factor of two compared to SPT-3G readout hardware. This improvement enables operation of bolometers at lower resistance than SPT-3G, which opens up a larger range of phase space for optimization based on noise performance. Broadly, the prototype architecture shows promise as a more scalable, potentially higher-multiplexing factor, alternative to the standard DfMux system, and more detailed characterization and laboratory testing are warranted to fully mature this technology.

Ongoing testing of this prototype hardware will focus on detailed characterization of the in-transition noise level and crosstalk between bolometers. Additionally, we plan to make a detailed measurement of the thermal dissipation of the SA13 SQUIDs in this configuration and will identify a design requirement for SQUID thermal dissipation. We also plan to test the prototype architecture with lower normal resistance bolometers and scale up to operating a larger number of modules.

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