A Model for R(t) Elements and R(t)-Based Spike Timing-Dependent Plasticity with Basic Circuit Examples

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***Abstract*—Spike timing-dependent plasticity (STDP) is a fundamental synaptic learning rule observed in biology that leads to numerous behavioral and cognitive outcomes. Emulating STDP in electronic spiking neural networks with high-density memristive synapses is therefore of significant interest. While one popular method involves pulse-shaping the spiking neuron output voltages, an alternative approach is outlined in this paper. The proposed STDP implementation uses time-varying dynamic resistance (R(t)) elements to achieve local synaptic learning from spike-pair STDP, spike triplet STDP, and firing rates. The R(t) elements are connected to each neuron circuit thereby maintaining synaptic density and leverage voltage-division as a means of altering synaptic weight (memristor voltage). Example R(t) elements with their corresponding behaviors are demonstrated through simulation. A three-input-two-output network using single-memristor synaptic connections and R(t) elements is also simulated. Network-level effects such as non-specific synaptic plasticity are discussed. Finally, spatiotemporal pattern recognition (STPR) using R(t) elements is demonstrated in simulation.**

***Index Terms*—Memristor, spike-timing-dependent plasticity, spiking neural network, synapse.**

I. Introduction

Human brains are made up of billions of neurons which generate voltage spikes called action potentials in response to stimulus [1]. Those billions of neurons are interconnected through trillions of synapses which effectively serve to scale the magnitude of action potentials that pass through them [2]. The amount of scaling that a synapse performs is referred to as its synaptic efficacy, strength, or weight. The weight of a synapse is not static, and changes over time based on learning rules that depend on pre- and post-synaptic neuron activity. Timing differences between two action potentials occurring in the neurons that the synapse connects is one mechanism that can alter the weight [3]–[5]. This is known as Spike-Timing-Dependent Plasticity (STDP).

Many forms of STDP have been observed in different brain regions across various species. It is known to be responsible for abilities including rapid response to threats and sound source localization [4], [6]–[11]. However, it is also known that biological synapses implement much more complex and diverse learning rules than pair-based STDP [12]. In reality, synapses integrate multiple action potentials asymmetrically and can alter their weight over longer timescales containing multiple pre- and post-synaptic spikes [12]–[17]. Broader consequences of this observation are not well understood, but may enable many advanced cognitive functions.

Electronic spiking neural networks comprised of STDP synapses have been shown to perform complicated learning tasks such as pattern recognition, classification, and feature extraction [18]–[24]. Due to these demonstrated abilities, many researchers have implemented STDP synapses using CMOS circuits [25]–[31]. The circuits generally contain at least a dozen devices and have relatively large footprints [28], [30]–[32]. Both these traits are highly undesirable when the objective is to maximize synaptic density and the overall number of synapses. In other words, although local Hebbian learning rules such as STDP are essential for constructing networks with an extremely large number of elements, the synapse implementations must also be compact.

Memristors are an ideal candidate for electronic synapses because they have only two terminals and can change their resistance based on previously applied bias. They can also be non-volatile with very small cross-sectional area, and densely fabricated in crossbar array structures [33]–[42]. Using single memristors as synapses requires that the neurons somehow control synaptic weight change. A dominant approach for obtaining STDP with memristive synapses is to engineer the shape of the neuron output voltage pulses to achieve the desired weight update function [21], [37], [41], [43]–[50]. In the pulse-shaping method, signals are directed toward both the axonic and dendritic synapses whenever a neuron fires. The potential across the memristor itself is given by the difference between the post- and pre-synaptic voltages. The main drawback of this approach is that it allows only nearest-neighbor pairs of action potentials to contribute to synaptic weight changes, and has no dependence on firing rate [51]–[53]. This paper presents an approach that is similar and complementary to pulse shaping and is compatible with

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single-memristor synapses contained in crossbar arrays. The approach enables the realization of traditional pair-based STDP as well as rules that depend on multiple spikes and long-term firing rates. The key to facilitating these effects is the addition of dynamic resistance, or R(t), elements to the input and output of each hidden layer neuron circuit. In this work, we define R(t) elements as circuits or devices which possess time-varying resistance. This technique is similar to pulse shaping in that a time-varying quantity is driving STDP. However, the distinguishing characteristic of R(t)-based STDP is that the path resistance between neurons changes as a function of the pre- and post-synaptic neuron outputs. Table I compares and contrasts the R(t) and shaped pulse methods of facilitating STDP.

A simple digital pulse is used in the examples presented in this work to activate the R(t) elements which creates the time-varying resistance. This creates a network of time-dynamic voltage dividers, and maximizes the simplicity of the synapses while only slightly increasing the complexity of the neurons. Simple digital pulses are used for mathematical convenience; however, shaped pulses can also be used with R(t) elements for even more complicated learning rules, but this is beyond the scope of this introductory work.

The remainder of this paper is organized as follows: Section II describes perfect STDP using R(t) elements and single memristor synapses and explains the process involved in component value selection. Section III presents examples and simulations of R(t) implementations that result in pair-based and triplet STDP behavior. Section IV contains simulations demonstrating STDP in networks using R(t) elements and single-memristor synapses, and discusses other characteristics of the network. Conclusions are presented in Section V.

II. STDP WITH R(T) ELEMENTS

An R(t) element is a circuit or device which possess a time-varying resistance. To design an R(t) element, one must design a circuit or device such that a controlling quantity varies in time to produce the desired R(t) response. One way to do this is to design a circuit or device which implements an activation function, Q, to bridge the gap between R(t) and the controlling quantity function, ₡. The relationship between the activation function, the time-varying controlling quantity, and the resulting effective resistance is depicted in Fig. 1a. To facilitate

TABLE I
COMPARING AND CONTRASTING THE R(T) AND SHAPED PULSE METHODS OF FACILITATING STDP

	R(t)	Shaped Pulses
Frequency influenced learning rules	Yes	No
Sensitive to component values	Yes[a]	No
Only needs one potential	Yes	No
Sneak paths	Yes[b]	Yes[b]
Frequency influenced nonspecific synaptic plasticity	Yes	No

[a]This depends on the desired behavior. The equations presented in this work represent a rigid case where synaptic weight change is guaranteed not to occur outside of the influence of related spikes. However, if merely facilitating STDP is desired, then component value selection can be relaxed. [b]If the network doesn't use neurons which control the potential at their inputs, then the network will have sneak paths.

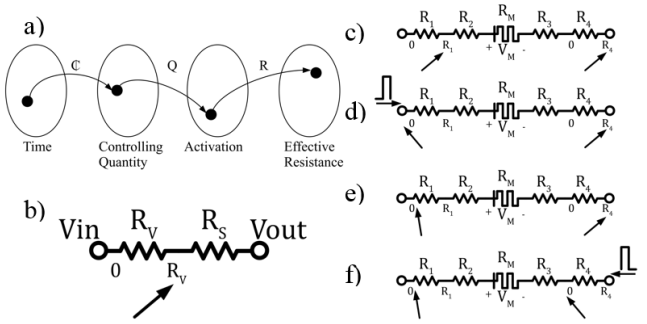

Fig. 1. An R(t) Element model and the four stages of R(t)-based STDP. a) Illustration showing that R(t) is a composition of three functions. b) An R(t) element model represented as a static resistance, R_S, and a variable resistance, R_V, capable of sweeping between 0 and R_V in time. c) An STDP circuit, consisting of two R(t) elements on either side of a memristor, is in its initial state with pre- and post-synaptic R(t) elements at their maximum resistances. d) A digital pre-synaptic pulse arrives, driving its associated R(t) element to its minimum value. e) Some time passes, over which the resistance of the pre-synaptic R(t) element rises. f) A post-synaptic pulse arrives, driving the post-synaptic R(t) element to its minimum value, and placing a potential across the memristor, V_M, greater than its negative threshold V_{TH}^-, causing memristance to decrease.

excitatory STDP behavior, the activation functions should be implemented such that the R(t) element's resistance decreases sharply when exposed to stimulus and increases slowly once the stimulus is removed. In this work we use the term activated to describe a condition where the controlling quantity abruptly and temporarily increases resulting in a temporary state of reduced resistance for the R(t) element. R(t) elements have been modeled using

$$R(t) = R_V Q(₡(t)) + R_S, \quad (1)$$

where R_V is the variable portion of the R(t) element, R_S, is the static portion of the R(t) element which represents its minimum series resistance, Q is an activation function which converts a controlling quantity into a real number in the range [0,1], and ₡ is the controlling quantity function which represents a controlling quantity, such as potential or charge, at a particular time.

From the model one can see that the R(t) element has a minimum resistance of R_S and a maximum resistance of $R_S + R_V$. Using two resistors instead of a single resistor is a mathematical convenience to describe the R(t) element's resistance with a single activation factor between zero and one. Fig. 1b depicts a two-resistor model of an R(t) element. The angle of the arrow going from left to right in the figure is a graphical approximation of the effective resistance of R_V in the range from zero to R_V at a particular moment in time.

A. Synaptic Weight Change

Two R(t) elements combined with a memristor form a circuit which can implement STDP through voltage division. In very general terms, when only one R(t) element is activated, neural spiking is insufficient to cause the voltage across the memristor, V_M, to exceed the memristor's threshold, V_{TH}. However, when both R(t) elements are sufficiently activated, the resistance of the memristor, relative to the rest of the branch, is large enough to cause neural spike voltage to exceed its threshold voltage. More specifically, an increase in synaptic strength through an STDP circuit using digital spiking neurons and R(t) elements with single-memristor synapses can be explained in four stages, as depicted graphically in Fig. 1 c-f. In the first stage, it is

assumed that no spikes have occurred for a long enough time period that both pre- and post-synaptic R(t) elements are in their most resistive states. It is also assumed that the value of the memristor is somewhere between its most resistive (R_{OFF}) and least resistive (R_{ON}) states. The second stage begins when a pre-synaptic spike occurs. The resistance of the pre-synaptic R(t) element is suddenly reduced, and the voltage across the memristor is less than the memristor positive threshold voltage, V_{TH}^{+}, meaning that its value will remain unchanged. In the third stage the pre-synaptic R(t) element's resistance has increased with the passage of time, but is still not at its maximum value. The fourth stage begins with the arrival of a post-synaptic spike. The reduced resistances of the R(t) elements results in a negative voltage, greater in magnitude than the absolute value of the negative memristor threshold voltage, $|V_{TH}^{-}|$, across the memristor. This causes its memristance to decrease. As the memristance is decreased, the total path resistance is reduced. This results in a higher current for a given potential. So, more charge is transferred to the post-synaptic neuron through the synapse for a given spike—the synaptic connection has strengthened. A decrease in synaptic resistance due to a post-pre spike pair is achieved similarly. One final thing to note is that if the memristors used in the simulation are additive in nature, meaning that a change in their memristance is not dependent on their instantaneous memristance value, R(t) element-based STDP causes non-additive behavior to manifest due to the state of the memristor affecting the voltage that it drops in the resistive voltage divider.

B. Component Value Selection for Perfect STDP

In this work we define perfect STDP as a synaptic connection where synaptic change is guaranteed not to occur outside of related spikes. The rest of this section describes how to choose component values that will result in perfect STDP. Before choosing to design STDP circuits which implement perfect STDP, circuit designers should bear in mind that perfect STDP has very strict requirements, results in very small synaptic changes, and as will be demonstrated in Section IV, is not necessary to facilitate spatiotemporal pattern recognition (STPR) with R(t) elements. This section is included to demonstrate that perfect STDP is mathematically possible rather than to be a design guide that one should rigidly follow.

To design a perfect STDP circuit with R(t) elements and a memristor, one must determine the values of R_S and R_V for each R(t) element, decide on an activation function Q, and implement the design. Instead of defining a specific implementation of Q, we will use particular values of Q, denoted as X and Y, to determine values of R which will enable STDP to occur, as implementing a particular activation function is beyond the scope of this work. Our strategy is to focus on selecting particular values of R_V and R_S which will facilitate STDP for all possible values that a particular memristor could have. The shape of a particular STDP curve is due to the composition of $R \circ Q \circ ¢ = R\left(Q\left(¢(t)\right)\right)$, and so to attain a specific desired STDP curve one must carefully design their circuits; however, the point of this work is not to design any particular STDP curve, but rather to show how STDP is possible in the first place and to provide a model which, when properly implemented, guarantees perfect STDP behavior.

With this in mind, to facilitate STDP the memristor voltage, V_M, must be considered with respect to its threshold voltage for two cases: where change is desired ($|V_M| \geq V_{TH}$) and where change is undesired ($|V_M| < V_{TH}$). We assert that the activation of an R(t) element occurs when a bias is applied to its input terminal. In other words, when a voltage spike is applied to Terminal 1 (Terminal 2) in Fig. 1, $R_1(R_4)$ is activated. Its resistance suddenly decreases toward R_S and then slowly rises over time toward $R_V + R_S$.

1) Choosing the R_V values: R_1 and R_4

Resistances R_1 and R_4 are the variable portions of the R(t) elements. They control whether, or not, and by what amount the memristor will be changed in response to spiking stimulus. Consider the STDP circuit model depicted in Fig. 1b. If a potential of V_{PRE} were applied to Terminal 1, and ground were applied to Terminal 2, then the memristor voltage would be

$$V_M = V_{PRE}\frac{R_M}{XR_1 + R_2 + R_M + R_3 + YR_4} \tag{2}$$

where X and Y are real values between zero and one which represent how resistive, at the moment when V_{PRE} is applied, R_1 and R_4 are, respectively. Assume that the R(t) element connected to Terminal 1 is fully activated, and therefore minimally resistive (X=0). Depending on the type of R(t) element it may not be true that a single neural spike would fully activate it. However, this is a safe assumption to make because, for the purpose of determining component values, we are assuming some activation of R_4 and applying a DC bias, and not neural spikes, to Terminal 1. For the case when change is desired, the component values must result in a situation where $V_M \geq V_{TH}$. Substituting into (7) and rearranging gives us

$$R_M\left(\frac{V_{PRE}}{V_{TH}^{+}} - 1\right) \geq R_2 + R_3 + YR_4. \tag{3}$$

This inequality describes all of the factors which determine whether, or not, memristance will change: the current value of R_M, the values chosen for V_{PRE}, R_2, R_3, and R_4, and the resistance of R_4, at the time V_{PRE} is applied.

A similar inequality can be derived for the case when change is undesired ($V_M < V_{TH}$):

$$R_M\left(\frac{V_{PRE}}{V_{TH}^{+}} - 1\right) < R_2 + R_3 + YR_4. \tag{4}$$

Let A denote the resistance of R_4, above which $V_M < V_{TH}$, regardless of R_M, and let B denote the resistance of R_4, below which $V_M > V_{TH}$, regardless of R_M. Choosing A and B is accomplished by examining the fringe cases where change is undesired with the memristor at its highest resistance value ($R_M = R_{OFF}$) and where change is desired with the memristor at its lowest resistance value ($R_M = R_{ON}$), and then selecting from the allowed values. The fringe cases can be expressed as

$$V_{TH}^{+} \leq V_{PRE}\frac{R_{ON}}{R_2 + R_{ON} + R_3 + BR_4} \text{ and} \tag{5}$$

$$V_{TH}^{+} > V_{PRE}\frac{R_{OFF}}{R_2 + R_{OFF} + R_3 + AR_4} \tag{6}$$

which can be combined and rearranged to yield

$$(R_2 + R_3)(R_{OFF} - R_{ON}) < R_4[R_{ON}A - R_{OFF}B]. \tag{7}$$

Since R_2, R_3, and R_4 are greater than zero, and $R_{OFF} > R_{ON}$, then

$$R_{ON}A > R_{OFF}B \tag{8}$$

which can be rearranged into

$$\frac{A}{B} > \frac{R_{OFF}}{R_{ON}}. \tag{9}$$

This inequality is a good rule of thumb for choosing A and B, but insufficient to ensure that the circuit wil produce perfect STDP. Thus, start by choosing A and B which satisfy (9). Next, R_4 is chosen. Re-examining the fringe cases, they can be expressed as

$$R_{OFF}\left(\frac{V_{PRE}}{V_{TH}^{+}} - 1\right) < R_2 + R_3 + AR_4 \text{ and} \tag{10}$$

$$R_{ON}\left(\frac{V_{PRE}}{V_{TH}^{+}} - 1\right) \geq R_2 + R_3 + BR_4. \tag{11}$$

It is clear that if

$$R_4 = \frac{R_{OFF}\left(\frac{V_{PRE}}{V_{TH}^{+}} - 1\right)}{A} \dagger \tag{12}$$

and the value of B is updated such that

$$B \leq \frac{R_{ON}\left(\frac{V_{PRE}}{V_{TH}^{+}} - 1\right) - (R_2 + R_3)}{R_4} \tag{13}$$

then (9), (10), and (11) can all be satisfied. The next step depends on whether symmetrical STDP is desired. If symmetrical STDP is desired, then let R_2=R_3, R_1=R_4, and choose R_2. If asymmetrical STDP is desired, then connect ground to Terminal 1 and V_{POST} to Terminal 2. Assume that the R(t) element connected to Terminal 2 is fully activated, and therefore minimally resistive (Y=0). Thus (2) becomes

$$V_M = V_{POST}\frac{R_M}{XR_1 + R_2 + R_M + R_3}. \tag{14}$$

Let C denote the resistance of R_1, above which $V_M < V_{TH}^{-}$, regardless of R_M, and let D denote the resistance of R_1, below which $V_M > V_{TH}^{-}$, regardless of R_M.

Choosing C and D is accomplished by examining the fringe cases where change is undesired with the memristor at its highest resistance value ($R_M = R_{OFF}$) and where change is desired with the memristor at its lowest resistance value ($R_M = R_{ON}$), and then selecting from the allowed values. The fringe cases can be expressed as

$$V_{TH}^{-} \leq V_{POST}\frac{R_{ON}}{DR_1 + R_2 + R_{ON} + R_3} \tag{15}$$

$$V_{TH}^{-} > V_{POST}\frac{R_{OFF}}{CR_1 + R_2 + R_{OFF} + R_3} \tag{16}$$

which can be combined and rearranged to yield

$$(R_2 + R_3)(R_{OFF} - R_{ON}) < R_1[R_{ON}C - R_{OFF}D]. \tag{17}$$

Since R_1, R_2, and R_3 are greater than zero, and $R_{OFF} > R_{ON}$, then

$$R_{ON}C > R_{OFF}D, \tag{18}$$

which can be rearranged into

$$\frac{C}{D} > \frac{R_{OFF}}{R_{ON}}. \tag{19}$$

This inequality is a good rule of thumb for choosing C and D, but insufficient to ensure that the circuit will produce perfect STDP. Thus, start by choosing C and D which satisfy (19).

Next, R_1 is chosen. Re-examining the fringe cases, they can be expressed as

$$R_{OFF}\left(\frac{V_{POST}}{V_{TH}^{-}} - 1\right) < CR_1 + R_2 + R_3 \text{ and} \tag{20}$$

$$R_{ON}\left(\frac{V_{POST}}{V_{TH}^{-}} - 1\right) \geq DR_1 + R_2 + R_3. \tag{21}$$

It is clear that if

$$R_1 = \frac{R_{OFF}\left(\frac{V_{POST}}{V_{TH}^{-}} - 1\right)}{C} \ddagger \tag{22}$$

and the value of D is updated such that

$$D \leq \frac{R_{ON}\left(\frac{V_{POST}}{V_{TH}^{-}} - 1\right) - (R_2 + R_3)}{R_1} \tag{23}$$

then (19), (20), and (21) can all be satisfied. Finally, choose R_2 and R_3.

2) Choosing the R_S values: R_2 and R_3

The combination of R_2 and R_3 limit the maximum theoretical voltage that can be applied to the memristor and therefore limit the magnitude of change that the memristor can undergo due to the application of a spike. The individual values of R_2 and R_3 will not affect the shape of the STDP curve, only their combined value. To ensure that the memristor will change as desired, choose R_2 and R_3 such that the quantity $R_2 + R_3$ obeys all of the following inequalities:

$$R_2 + R_3 \leq \frac{V_{PRE}}{V_{TH}^{+}}R_{ON} - R_{ON} - BR_4 \tag{24}$$

$$R_2 + R_3 > \frac{V_{PRE}}{V_{TH}^{+}}R_{OFF} - R_{OFF} - AR_4 \tag{25}$$

$$R_2 + R_3 \leq \frac{V_{POST}}{V_{TH}^{-}}R_{ON} - R_{ON} - DR_1 \tag{26}$$

$$R_2 + R_3 > \frac{V_{POST}}{V_{TH}^{-}}R_{OFF} - R_{OFF} - CR_1 \tag{27}$$

III. R(T) ELEMENT IMPLEMENTATION EXAMPLES

Previous work has demonstrated that synapses composed of single memristors driven by short-term memory transistors are capable of STDP. Specifically, thin-film transistors (TFTs) with layers of nanoparticles in the gate dielectric were used to drive memristive synapses. Close correspondence to biological measurements for spike pairs, triplets, and overall frequency measurements [54]–[56]. Simulations also indicated these networks are capable of performing STPR [24]. The nanoparticle TFTs effectively perform the function of an R(t) element, as will be discussed in Section III D.

† Any R_4 such that $R_4 > \frac{R_{OFF}\left(\frac{V_{PRE}}{V_{TH}^{+}} - 1\right)}{A} - (R_2 + R_3)$ will satisfy (10)

‡ Any R_1 such that $R_1 > \frac{R_{OFF}\left(\frac{V_{POST}}{V_{TH}^{-}} - 1\right)}{C} - (R_2 + R_3)$ will satisfy (20).

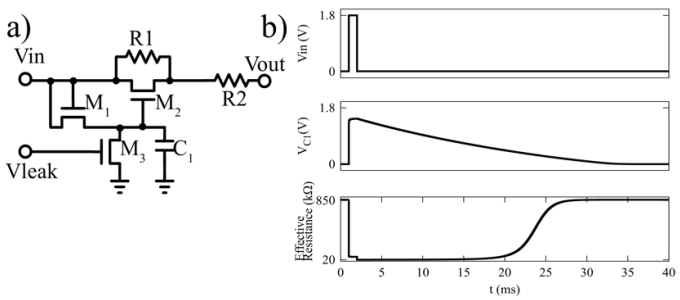

Fig. 2. a) A schematic of a simple R(t) element circuit. b) The simple R(t) element circuit's response to a 1 ms long 1.8 V digital (square) pulse with Vleak = 50 mv, R1=842 kΩ, R2=19 kΩ, C_1 =1 pF, and W/L=10/2 for all MOSFETs. Effective resistance is calculated as the voltage difference between Vin and Vout over the current through R2. A small measuring bias voltage is applied to Vin, but not C1, in the absence of spiking stimulus.

This section provides two additional examples of R(t) elements in the form of CMOS circuits (as opposed to devices). These basic circuits, are designed using the R(t) element model described in Section II, and are meant to emphasize the characteristics of simple and compound R(t) elements rather than perfectly encapsulate simple and compound R(t) element functionality. We demonstrate how to create STDP circuits with these circuits, and provide simulation results conducted using the industry-standard circuit design software Cadence Virtuoso, TSMC 0.18 micron technology MOSFET models, and the NCSU Cadence design kit [57].

The first example is a simple R(t) element circuit, defined to be an R(t) element that achieves its maximum resistance change from a single digital pulse. The second example is a compound R(t) element circuit, defined as an R(t) element that requires multiple digital pulses to achieve their maximum resistance change. Both examples were used in conjunction with an ideal memristor with the following characteristics: α=0.001, R_{ON}=10 kΩ, V_{TH}^{+}=200 mV, V_{TH}^{-}=-200 mV, ΔM described by:

$$f(M, V_M, V_{TH}^{+}, V_{TH}^{-}) = \begin{cases} \alpha \exp(V_M - V_{TH}^{+}) - 1, V_M > V_{TH}^{+} \text{ and } M < R_{OFF} \\ -\alpha \exp(|V_M - V_{TH}^{-}|) - 1, V_M < V_{TH}^{-} \text{ and } M > R_{ON} \\ 0, \text{otherwise,} \end{cases} \quad (28)$$

and memristance, M, described by

$$M = R_{ON}\frac{w}{D} + R_{OFF}\left(1 - \frac{w}{D}\right), \quad (29)$$

where w/D represents physical characteristics of the memristor which for the purposes of a memristor-based synapse can be thought of as the weight with values between zero and one [36], [58]–[60].

A. Simple R(t) Element Circuits

The first implementation of an R(t) element circuit that will be demonstrated is a simple R(t) element circuit. We define a simple R(t) element as an R(t) element that achieves its maximum resistive change from a single digital pulse. The values of R_1 and R_2 were chosen in accordance with the guidance described in the previous section. A and B were chosen to be 0.95 and 0.05 respectively, which resulted in R_1 and $R_2 + R_3$ being 842 kΩ and 38 kΩ respectively. Since symmetrical STDP was desired, and the memristor used had symmetrical characteristics, R_4=R_1. Fig. 2 depicts a schematic of a simple R(t) element circuit and a plot of the response of the simple R(t) element to a 1.8 V digital pulse applied to Vin when w/D=0.5.

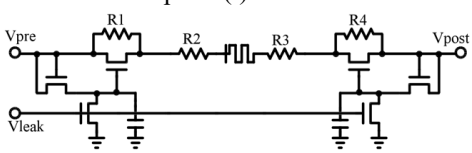

Fig. 3. A schematic of a simple R(t) element-based STDP circuit. It is important to note that the R(t) elements are not part of the synapse, many memristive synapses can be fed by a neuron through a single R(t) element, rather they are an accessory to be added to a neuron. In this figure, the neurons have been substituted with piece-wise linear voltage sources to create simple digital pulses.

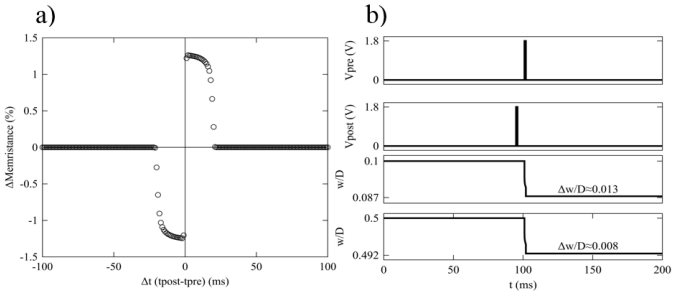

Fig. 4. a) The pair-based STDP plot created by an STDP circuit composed of two simple R(t) element circuits and a memristor. The memristor is initialized to 55 kΩ (w/D=0.5). Applied pre- and post-synaptic pulses are 1.8 V digital pulses with pulse widths of 1 ms and Vleak=40 mV. b) A simulation demonstrating the multiplicative behavior of the additive memristor due to the voltage dividing nature of the R(t) element-based STDP circuit. The same pre- and post-synaptic potentials are applied to two identical simple STDP circuits (Vleak=40 mV) except for the initial condition of the two memristors (0.100 in one and 0.500 in the other). The memristor with the lower initial w/D, and thus a higher initial memristance, experiences a larger $\Delta w/D$ because it drops a larger fraction of the applied potential.

When a digital pulse arrives at Vin, capacitor C_1. Is charged through diode connected MOSFET M1. For the duration of the pulse, V_{GM2} rises towards Vin-V_{DS}, increasing the conduction of M2 and lowering the overall effective resistance of the R(t) element. When the simple digital pulse ends, charge leaks to ground out of C_1 through M3, at a rate determined by Vleak. This causes V_{GM2} to lower over time and the effective resistance of the R(t) element to rise over time. This particular implementation of an R(t) element circuit used in an STDP

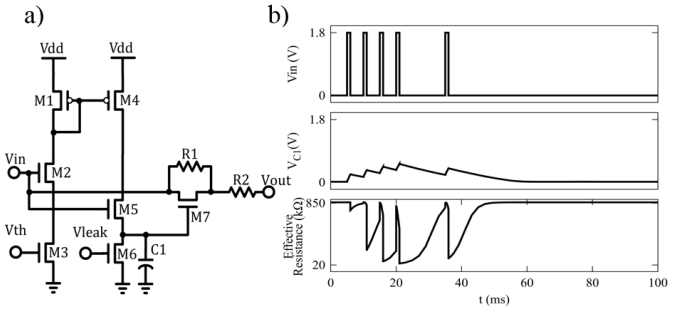

Fig. 5. a) A schematic of a compound R(t) element circuit. b) The compound R(t) element circuit's response to simple 1 ms duration 5 V digital pulses with Vleak= 40mV, Vth=68 mV, R1=842 kΩ, R2=19 kΩ, C1=1 pF, and W/L=10/2 and 20/2 for all NMOS and PMOS respectively. Effective resistance is calculated as the voltage difference between Vin and Vout over the current through R2 with a small measuring bias applied to Vin, but not C1, in the absence of spiking stimulus.

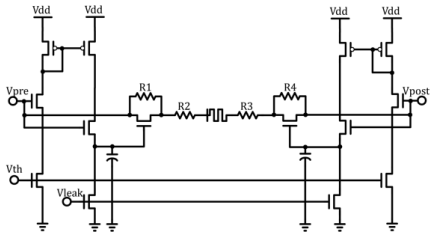

Fig. 6. A schematic of the compound R(t) element-based STDP circuit. It is important to note that the R(t) elements are not part of the synapse, many memristive synapses can be fed by a neuron through a single R(t) element, rather they are an accessory to be added to a neuron. In this figure, the neurons have been substituted with piece-wise linear voltage sources to create simple digital pulses.

circuit as shown in Fig. 3, produces the STDP curve of Fig. 4a. Although the memristor described in (28) is additive, the memristor will change in a non-additive fashion due to the voltage dividing action of the STDP circuit. This property is portrayed in Fig. 4b. It is important to note that the R(t) elements in this single STDP circuit do not belong to the synapse memristor, but instead to the input and output neurons connected through it. In a network configuration, many single-memristor synapses may be connected to a particular neuron's R(t) element. This is explained in more detail in Section IV.

B. Compound R(t) Element Circuits

The second implementation of an R(t) element circuit that will be demonstrated is a compound R(t) element circuit. We define a compound R(t) element as an R(t) element that requires multiple digital pulses to achieve its maximum resistance change. The values of R_1 and R_2 from the previous example circuit are used. Fig. 5 shows a schematic of a compound R(t) element circuit and a plot of the response of the compound R(t) element to five 1.8 V digital pulses applied to Vin.

Fig. 7. Three separate spike trains are applied to the same compound R(t) element-based STDP circuit with the same settings (Vleak=40 mV, Vth=125 mV, memristor initialized to w/D=0.500). The pre- and post-synaptic R(t) element's effective resistances are depicted with thin solid and dotted lines respectively. The memristor's w/D is depicted with a thick line. The times of pre- and post-synaptic spikes are represented with ○ and + respectively. Notice how the magnitude of change varies as the inter-spike-interval and time between triplets varies. a) Three spike triplets are applied to the compound STDP circuit with an inter-spike-interval of 6 ms and 15 ms between triplets. b) Three spike triplets are applied to the compound STDP circuit with an inter-spike-interval of 3 ms and 15 ms between triplets. c) Three spike triplets are applied to the compound STDP circuit with an inter-spike-interval of 6 ms and 10 ms between triplets. Applied pre- and post-synaptic pulses are 1.8 V digital pulses with pulse widths of 1 ms.

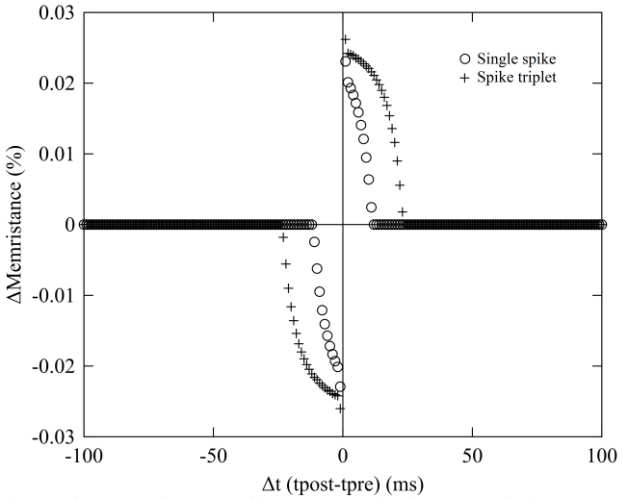

Fig. 8. The STDP plot created by an STDP circuit composed of two compound R(t) element circuits and a memristor under the influence of two different kinds of stimulus—pairs of single spikes and spike triplets. The pairs of single spikes are typical pre-post pairs, whereas the spike triplets are pre-pre-post and post-post-pre triplets where the first two spikes are separated by 5 ms. The memristor is initialized to 55 kΩ (w/D=0.5). Applied pre- and post-synaptic pulses are 1.8 V digital pulses with widths of 1 ms. Vleak=40 mV and Vth=125 mV.

When a simple digital pulse is applied at Vin to the compound R(t) element, current flows through the current-mirror-like arrangement composed of M1, M2, and M3. This induces another current (Vth≠Vleak) in the structure composed of M4, M5, and M6. The induced current is divided between flowing to ground through M6 and charging C1. The charge in C1 raises V_{GM7} which increases the conductivity of M7 and lowers the effective resistance of the R(t) element. When the simple digital pulse at Vin ends the charge stored in C1 leaks to ground through M6 at a rate determined by Vleak. This particular implementation of a compound R(t) element used in an STDP circuit is shown in Fig. 6.

Since compound R(t) elements, by definition, cannot achieve their least resistive state by a single spike, the STDP curve changes for different combinations of spikes. The

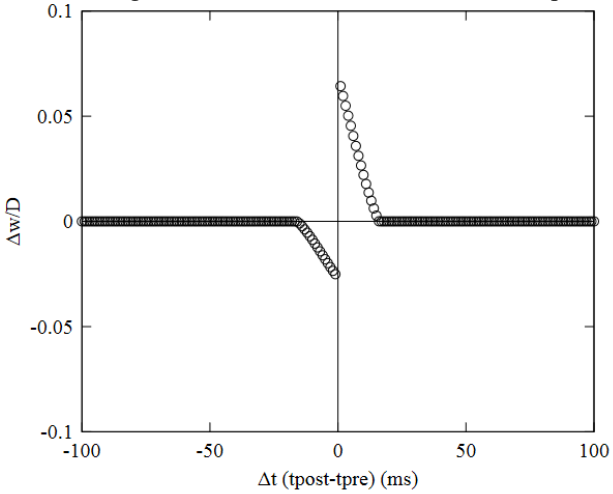

Fig. 9. The STDP plot created by using two simple R(t) elements and a memristor based on the Yakopcic model.

memristance changes resulting from pre-post pairs and pre-pre-post triplets produce different STDP curves because the effective resistance of compound R(t) elements is dependent on the cumulative effect of spike combinations. Thus, combinations of spikes will produce different effects than pairs of single spikes. These higher-order effects, which lead to STDP asymmetry, are examined in Fig. 7. Here, evenly spaced spike-triplets, which would otherwise leave the memristor unchanged, cause a net change in w/D. Two things to note are how the second pair of spikes in the triplet are dominant. A pre-post-pre triplet acts more like a post-pre pair than a pre-post pair. In addition, the repetition frequency clearly affects the change in w/D, as each successive repetition of the triplet causes the magnitude of the change in w/D to increase.

Further, the circuit produces the STDP curves depicted in Fig. 8 when exposed to spike-pair stimulus and spike-triplet stimulus. The triplets are composed of sequences of 1.8 V pre-pre-post ($\Delta t < 0$) and post-post-pre ($\Delta t > 0$) synaptic spikes of 1 ms in duration with 6 ms between the leading edges of the first two spikes in the sequence, and Δt is taken to be the time between the leading edges of the second and third spikes in the sequence. It is important to note that the R(t) elements in this single STDP circuit do not belong to the synapse memristor, but instead to the input and output neurons connected through it. In a network configuration, many single-memristor synapses may be connected to a particular neuron's R(t) element. This is explained in more detail in Section IV.

C. Demonstration with a More Realistic Memristor Model

To demonstrate how R(t) elements can facilitate STDP with a less ideal, and more realistic memristor, an STDP circuit was constructed using two simple R(t) elements and a memristor based on the Yakopcic model [61], [62]. The memristor parameters are as follows: a_1=a_2=0.135, b=0.025, V_p=V_n=0.2, A_p=A_n=4000, x_p=x_n=0.3, α_p=α_n=1, x_0=0.5, and η=1. The R(t) element parameters are R_1=R_2=R_3=R_4=1.5 kΩ. The resulting STDP plot is depicted in Fig. 9.

D. Discussion and Comparison to Other Methods

The use of charge-trapping TFTs mentioned previously is functionally similar to an R(t) approach in that the characteristics of the synaptic path are modified by an accessory element, independent of the neurons, to induce specific synaptic changes. Simulation, fabrication, and experimental validation of these devices have been demonstrated previously and has been shown to enable complex synaptic learning [56], [59], [63]. At first, the simplicity of using a single device as an R(t) element seems elegant and extremely advantageous. However, a great deal of design effort is required to realize device functionality in accordance with the requirements presented in Section II. Threshold voltage must be set to the proper value, and the subthreshold swing must offer the appropriate amount of conductance modulation for the operating voltages. Most importantly, thicknesses of the gate tunneling dielectrics and the charge trapping mechanism (nanoparticles or otherwise) must be precise to achieve the desired time constants. Once the circuit is fabricated, these response parameters cannot be tuned as in the CMOS implementations, dramatically reducing the flexibility of the design.

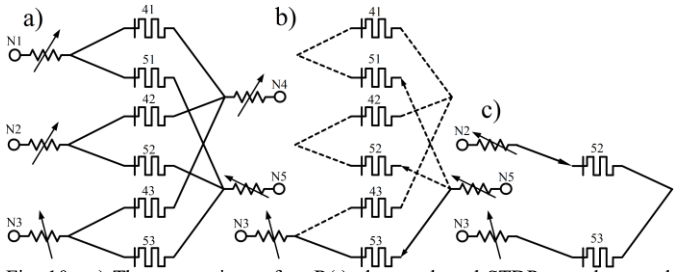

Fig. 10. a) The connections of an R(t) element-based STDP neural network consisting of three input neurons, two output neurons, six single-memristor synapses, and five R(t) elements. The connections to the pre-synaptic neurons are labeled N1-N3 and the connections to the post-synaptic neurons are labeled as N4 and N5. The synapses are labeled according to the neurons they connect using a post-pre naming convention. For example, Synapse 52 connects Neurons 5 and 2. These connections between the R(t) elements give rise to two types of non-specific synaptic plasticity. The first is heterogeneous non-specific plasticity, where the change in weight is due to a low resistance path which begins and ends on different layers. The second is homogeneous non-specific synaptic plasticity, where the change in weight is due to a low resistance path which starts and ends on the same layer. b) This figure depicts an example of the specific and non-specific synaptic paths that arise due to a pre-post pair. The specific path that results from N3 firing followed by N5 firing is illustrated with solid black lines. The non-specific paths, which could result in heterogeneous non-specific synapse weight increase of Synapses 51 and 52 and weight decreases of 41, 42, and 43, are illustrated with dashed black lines. c) This figure depicts an example of the non-specific path that arises due to a pre-pre pair. The non-specific path that results from N3 firing followed by N2 could result in the homogeneous non-specific synaptic weight decrease of Synapse 52 and increase of Synapse 53.

Comparison of power consumption between these two approaches is also important. In the simple and compound R(t) elements presented, the minimum effective resistance of the current path (when the element is activated) is on the order of R2 plus the channel resistance of M2 or M7, resulting in approximately 20 kΩ. This value is on the same order as the lowest possible on-state channel resistance achievable in TFT devices with high-k dielectrics such as HfO_2. Assuming that both the TFT and CMOS implementations would need to exhibit similar changes in resistance between the input and output terminal across similar voltage ranges, the power consumption should be similar in both cases.

One of the biggest drawbacks is that TFTs degrade significantly over time, resulting in an undesirable loss of the expected R(t) properties. It is also far more difficult to integrate these special devices into a typical CMOS fabrication process. Future R(t) element designs could be much more power- and area-efficient than either of the approaches discussed here. However, they would still need to follow similar behavioral rules to achieve the same learning characteristics for any given memristor technology.

IV. Network Examples

Neural networks are typically composed of multiple neurons, each of which connects to other neurons via synapses. The maximum number of R(t) elements, $\mathbb{A}$, required in a layered neural network with R(t) element-based STDP can be determined using

$$\mathbb{A} = I + O + 2\sum_{i=1}^{h} H_i, \tag{30}$$

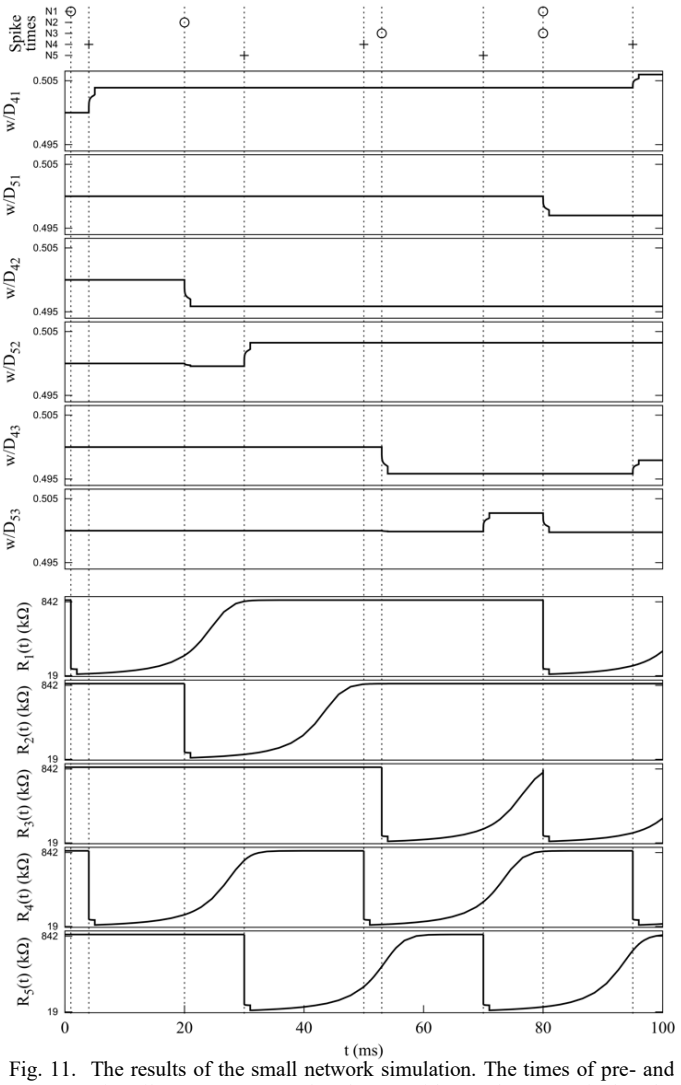

Fig. 11. The results of the small network simulation. The times of pre- and post-synaptic spikes are represented at the top with ○ and + respectively. The weights of the memristive synapses are shown in the middle and change via specific and non-specific plasticity over the course of the simulation. The effective resistances of the R(t) elements are shown at the bottom.

where I is the number of input neurons, O is the number of output neurons, H_i is the number of neurons in the i_{th} hidden layer, and h is the number of hidden layers. In most useful cases ($I > O \geq 2$) this is fewer than the maximum number of synapses, S, in a layered neural network given by

$$S = \sum_{i=1}^{n-1} N_i N_{i+1}, \tag{31}$$

where N_i is the number of neurons in the i_{th} layer and n is the number of layers.

A. Small Network Example

Fig. 10 depicts the connections of a network consisting of three input neurons, two output neurons, six synapses, and five R(t) elements. In Fig. 10, the R(t) elements are symbolically represented as variable resistors and the neurons have been abstracted as voltage signals applied to the connectome.

To demonstrate R(t) element-based STDP in this network, 1.8 V digital spikes of 1 ms duration were applied to the network inputs and outputs in a 100 ms transient simulation. Results of the applied stimulus are shown in Fig. 11. Note the rise in w/D that occurs at 4ms in synapse 41. This corresponds with the pre- and post-synaptic spikes at 1 and 4 ms, respectively. Also, the w/D increase at 30 ms in Synapse 52 is not as large. This is due to the increased amount of time between the pre- and post-synaptic spikes, at 20 and 30 ms, resulting in a larger post-synaptic R(t) element resistance at the time of the post-synaptic spike, and thus a smaller voltage across the memristor resulting in a smaller memristance change. The decreases in w/D that occur at 53 and 80 ms in synapses 43 and 51 respectively can be explained similarly.

At 20 ms into the simulation Synapse 52 decreases in strength, despite the fact that Neuron 5 had not fired yet. This non-specific synaptic plasticity is due to alternative paths through the multiple memristors between the pre- and post-synaptic firing neurons as depicted in Fig. 10. Unlike other methods that induce non-specific synaptic plasticity, which depend on the availability of alternative paths, often referred to as sneak paths, the induced synaptic change was facilitated by activated R(t) elements—meaning that the time between the non-specific spikes altered the resistances of the available paths making some paths temporarily more susceptible to the influence of non-specific synaptic plasticity than others. In simulation non-specific synaptic plasticity has been shown to improve the recognition of sparse patterns under certain conditions [64]. A final set of spikes was added at 80 and 95 ms to demonstrate that, although the memristor is behaving non-additively, the expression of the modified behavior may be very subtle.

Fig 12. The results of the STPR network simulation. The network consists of 25 afferent spiking neurons (N1 through N25), 26 R(t) elements, 25 memristors, and 1 output neuron (Nout). The network was trained using an unsupervised method consisting of the afferent neurons producing random spiking signals with a spike pattern embedded in them at random times. Notice that the spikes produced by the output neuron, Nout, occur after the presentation of the patterns (highlighted with grey bars)—this is STPR. A false positive occurs at 33.624 s and is highlighted with a grey circle.

B. STPR Example

A network consisting of 25 afferent neurons, 25 memristors, 26 R(t) element circuits, and one output neuron was also simulated to demonstrate STPR using R(t) elements. To demonstrate R(t) element-based STPR, 1.8 V digital spikes of 1 ms duration were simulated from the afferent neurons. Training was performed using an unsupervised method wherein the afferent neurons produced random spiking signals mixed with 1666 instances of a 10 ms spatiotemporal pattern over 30 seconds. Fig. 12 depicts a sample of the simulation after training. The STPR performed by this network are the spikes from the output neuron, Nout, which occur after the network is exposed to spatiotemporal patterns in the afferent neurons. The spatiotemporal patterns in Fig. 12 are highlighted with grey bars. A false positive occurs at 33.624 s in the simulation and is highlighted with a grey circle.

V. Conclusions

A model was described for designing dynamic resistance, or R(t) elements that achieve various forms of STDP in memristor-based neural networks. Two examples of R(t) element circuits, a simple R(t) element and a compound R(t) element, were presented. Behavior of these circuits was simulated in a commercially available software package using models provided by the foundry. Simulation results of a three-input, two-output, fully-connected spiking neural network using R(t) element-based STDP, and of STPR in a twenty-five-input, one-output SNN using R(t) circuit elements, were presented. Future work includes examining non-specific synaptic plasticity more closely, and confirming simulation results through circuit implementation and extensive electrical testing.

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