A Chopper Instrumentation Amplifier with Fully Symmetric Negative Capacitance Generation Feedback Loop and Online Digital Calibration for Input Impedance Boosting

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***Abstract* — A symmetric chopper instrumentation amplifier architecture with two identical 8-bit digitally programmable capacitor banks and online digital calibration block are presented. Designed for long-term brain signal monitoring applications, the feedback capacitor banks generate negative capacitance to cancel the input capacitance from electrode cables to boost the input impedance to above 2 GΩ at 10 Hz. These banks are controlled by an automatic digital background calibration unit that includes an oscillation prevention scheme to ensure stable operation. A chopping technique is introduced to enhance the noise performance of the instrumentation amplifier in combination with the capacitive feedback loop that also contains chopping switches. The instrumentation amplifier and online calibration blocks are designed in 0.13-µm BiCMOS technology with a 1.2V supply, consuming 115.9 µW and 176 nW, respectively. Simulations show that the amplifier has a 26.8 dB gain, 8.06 KHz bandwidth, 0.4 µV input-referred noise integrated from 0.1-100Hz, and -49.9 dB THD with 1mV peak-to-peak input. The core layout area of the calibration block is 2100 µm².**

***Keywords* — Chopping, instrumentaion amplifier, online calibration, negative capacitance generation feedback (NCGFB), input impedance boosting.**

I. INTRODUCTION

Chopper instrumentation amplifiers (IAs) are widely used in systems that can monitor physiological signals, such as in electrocardiography (ECG) and electroencephalography (EEG), due to their advantages of low noise, high input impedance and high common-mode rejection ratio (CMRR) [1]-[3]. In general, the chopping techniques are based on modulating the input signal to a higher frequency before it is applied to the amplifier, such that it can be processed with less flicker (1/f) noise. A chopping modulator up-converts the input signal to a chopper frequency, and delivers it to the amplifier. After amplification, the signal is down-converted back to the initial frequency range, while the output flicker noise of the amplifier is modulated only once and shifted to a higher frequency [4]. A low-pass filter (LPF) is typically employed to select only the signal band of interest and to suppress the high-frequency noise. The chopper frequency must be higher than the flicker noise corner frequency and the signal bandwidth to effectively circumvent the flicker noise.

Fig. 1 shows the proposed system consisting of a chopper IA, two negative capacitance feedback (NCGFB) blocks [5], a 2nd-order LPF, and a digital online calibration unit. The online calibration unit consists of two comparators for oscillation detection, a digital calibration block, and a bank (Mux) of eight 2:1 multiplexers. The use of NCGFB blocks for input impedance boosting has been validated with chip measurements in [6], where a variable gain amplifier (VGA) followed the LPF in the analog front-end chain. However, the calibration described in [6]-[7] is a foreground method executed at the startup of the system. On the other hand, the calibration block introduced in this paper is developed to continuously operate in the background. This will allow to compensate in real time for accidental changes of the electrode interface conditions from movements. In addition, the IA design presented in [5] and fabricated in [6] was improved in this work by implementing a chopping technique for 16× noise reduction. Furthermore, the proposed IA topology is fully-symmetric to enable the use of identical NCGFB capacitor banks and to enhance the CMRR. We plan to integrate the proposed IA in an ultra-low power (ULP) system-on-chip (SoC) for EEG monitoring with low-power seizure detection capability by following ULP system-on-a-chip design principles [8].

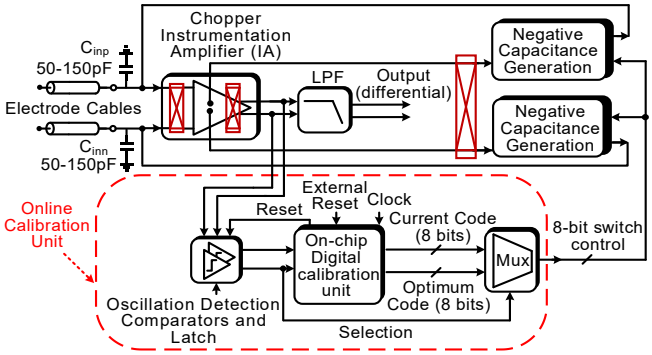

Fig. 1. Proposed chopper instrumentation amplifier with online digital calibration.

This paper is organized as follows. In Section II, the chopper IA design is discussed. The calibration unit is introduced in Section III. Section IV provides the simulation results for the chopper IA with the online digital calibration prior to the conclusion in Section V.

II. PROPOSED CHOPPER INSTRUMENTATION AMPLIFIER

Fig. 2 displays the schematic of the IA with NCGFB loop adapted from [5]-[6]. Compared to prior designs, this version has been enhanced with a chopping scheme, as well as full symmetry in the input stage by replacing a current mirror with two resistors R_{cm} for self-regulated biasing of transistors M_3 and M_4. The two resistors are controlling the gate voltages of M_3 and M_4 instead of the diode-connection of M_3 [5]-[6]. This modification results in a

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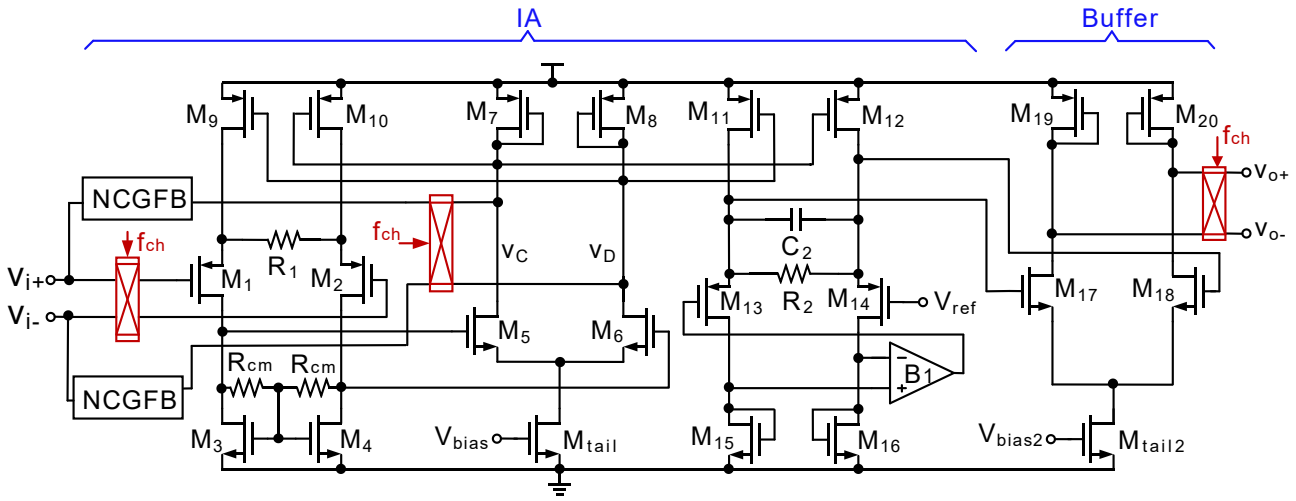


Fig. 2. Fully symmetric chopper IA with negative capacitance feedback (NCGFB).

symmetrical IA with identical gains from the input nodes to the nodes labelled V_C and V_D in Fig. 2. An important benefit of this improvement is that the programmable capacitors' values in the NCGFB blocks can be identical in both branches, avoiding the use of different unit capacitors as with an asymmetric input stage[] . Fig. 3(a) depicts the programmable NCGFB capacitors, which are controlled by the same code here. Furthermore, the symmetrical design also helps the CMRR.

The chopper modulator and demodulator blocks are shown in Fig. 3(b), which were designed based on [4] and [9]. They are implemented by using four transistors that act as switches. NMOS transistors are used in this design due to their higher transconductance relative to PMOS transistors, which improves noise performance. Chains of inverters are used within the chopper modulator blocks to generate complementary 4 KHz clock signals (ϕ and ϕ') with symmetrical delays and rise/fall times.

III. Proposed Online Digital Calibration

To boost the input impedance, the NCGFB generates negative capacitance to cancel the input capacitance of the input port, which is predominantly from the cable capacitance. This effect is achieved by controlling the eight digital switches (S_0-S_7) shown in Fig. 3(a) with a digital calibration block. Over-compensation occurs when excessive negative input capacitance is generated, which causes instability. To avoid oscillation, this instability is detected by monitoring the IA output. In case of an uncontrolled oscillation, the IA's output amplitude increases by at least threefold compared to normal operation. Thus, the reference voltages of the two comparators in Fig. 1 can be set to detect the onset of oscillation by making the range slightly wider than the expected signal swing.

Let us refer to the optimum code as the 8-bit code applied to the NCGFB switches (S_0-S_7) that results in the highest IA input impedance without causing oscillation. Consequently, the next code (referred to as oscillation code here) always results in oscillation. Hence, it can be deduced that the optimum code is lower than the oscillation code by one bit. However, to introduce a stability margin, the optimum code is chosen to be lower than the oscillation code by two bits during the automatic calibration. Therefore, the calibration logic has two main functions: First, it circulates through all the codes to determine the optimum code. Second, when detecting an onset of oscillation, it should avoid the oscillation by returning to the optimum code.

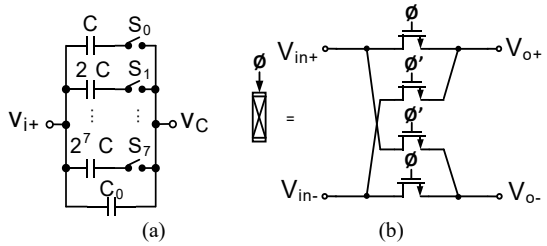


Fig. 3. (a) NCGFB capacitor bank, (b) modulator and demodulator block.

A. Comparator Design

The calibration scheme includes two comparators to prevent oscillation, as depicted in Fig. 4. The comparators are connected directly to the output of the IA to avoid the delay of the LPF in Fig. 1. If the output amplitude of the IA increases above or below certain reference voltages (V_{ref+} and V_{ref-}), one of the comparators will have a high output depending on whether the positive or negative threshold values is exceeded [6]. In this design, the reference voltages are set to 800 mV and 660 mV, allowing a differential signal swing up to 140 mV at the IA output. The schematic of the comparator is the same as in the earlier design [7], but the output logic has been modified as in Fig. 4. The comparators are connected to an OR gate to detect the oscillation onset from any of the two comparators. An SR latch is connected to the output of the OR gate to capture an instantaneous response. The output of this latch is connected the calibration logic, but also directly to the Mux in Fig. 1, where it acts as a selection signal. This signal immediately switches from low to high if there is an onset of oscillation, and it remains high until the reset signal is activated. Thus, the optimum code is recovered and applied instantaneously without waiting for further calibration logic operations. Note that the reset signal of the latch is generated from the digital logic as described in Section III.B. A D flip-flop (DFF) is also connected to the OR gate's output to

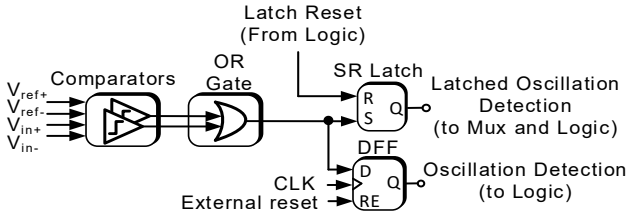


Fig. 4. Comparators and auxiliary digital blocks.

generate an oscillation signal that is synchronized with the positive clock edge for the digital calibration block. The output of this DFF is used as an indicator during the next calibration step.

B. Online Digital Calibration Block

This block delivers two codes to the Mux during each clock cycle, which are the current code and the optimum code. The former is a code under evaluation, and it is connected directly to the NCGFB block in Fig. 1 through the Mux if the Mux's selection signal is zero, which is the normal case. The optimum code is lower than the current code by two bits, and it is connected to the NCGFB block if its selection signal transitions to high when an oscillation onset is detected. The flow chart in Fig. 5 visualizes the digital calibration process. First, an external reset initializes all the signals and registers. Then, the digital calibration block produces a reset signal to reset the latch inside the comparator. If the oscillation signal from the DFF is active, this implies that an oscillation onset was detected, and both of the instantaneous and latched oscillation signals have been triggered. Moreover, the Mux selects the optimum code to be applied to the NCGFB block. During M = 10 clock cycles, the IA should be in a stable state because the optimum code was applied to its NCGFB block. Although the DFF's output is deactivated when the oscillation is prevented, the latched oscillation signal remains high. Consequently, the digital block realizes the past (i.e., during the last cycle) oscillation onset detection from the DFF's output, and it resets the SR latch inside the comparator. Afterwards, the current code continues to count again, starting from the optimum code value until it reaches to the oscillation onset code, repeating the same procedure. In the normal mode, each calibration step spans N = 6 clock cycles to allow the IA output to reach a steady state. M is chosen to be larger than N, as there is no need to count again after reaching to the optimum code. If the optimum code reaches its maximum value, then the current code will start counting from the beginning. With this algorithm, a continuous and automatic calibration is achieved. The clock frequency for the calibration is 60 Hz, hence it converges within 25.6 s, and then the optimum code is applied for M = 10 clock cycles (166 ms). In practice, the wait period of 10 cycles be extended to allow for more time between the repetition of the calibration process.

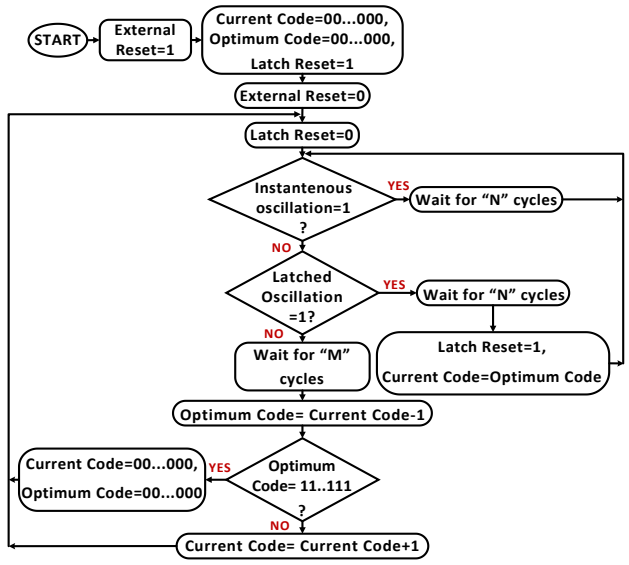


Fig. 5. Flow chart of digital calibration block.

IV. Simulation Results

The IA and the calibration unit were designed in 0.13-µm BiCMOS technology using only MOSFET transistors. The digital logic was written with the Verilog hardware description language, and simulated together with the analog circuits using Cadence's analog-mixed signal (AMS) tool. The IA was simulated separately using the Spectre tool for characterization. The Verilog code was synthesized to gate-level netlists, and to automatically place and route the layouts from the generated gate-level netlists for power and area estimations.

A. Chopper IA Characteristics

The chopping frequency of 4 KHz is higher than the EEG signal bandwidth and the 1/f corner frequency. An ideal 2nd-order passive LPF with a 100 Hz cutoff frequency was utilized in the simulations. Table 1 contains a comparison between the proposed IA characteristics and the earlier one in [5]. It can be observed that the total input-referred noise has been improved significantly, and that the output offset voltage has also decreased thanks to the chopping technique. In addition, the CMRR and PSRR have increased due to the fully-symmetric design. These results were obtained from transient simulations with noise enabled, and with a correlation coefficient of 0.9 between matched devices and of 0.99 for M_3/M_4 in Fig. 2; which implies the use of multiple fingers/subdevices with common-centroid matching for identical pairs of transistors and ratioed passives in the layout [10]. The IA voltage gain without the LPF is shown in Fig. 6, which was simulated using periodic AC (PAC) analysis. Fig. 7 presents the transient waveforms of the IA input signals and the output voltages

TABLE 1. COMPARISON OF SIMULATION RESULTS

Specifications	C. Chang, MWSCAS 2014	This Work
Gain [dB]	32.2	26.8
Bandwidth [KHz]	0.1	8.06
CMRR@10 Hz* [dB]	87.4	98.1
PSRR@10 Hz* [dB]	67.2	79.1
THD@10 Hz [dB] with 1m $V_{pk\text{-}pk}$ input	-51.2	-49.9
Output offset voltage [mV]*	1.8	0.49
Total input referred noise [µV] (noise bandwidth 0.1-100 Hz)	2.72	0.4
Input Impedance @ 10Hz [GΩ] (C_{in} = 50 pF)	5.8	2.4
Power [µW]	93.6	115.9

* Results are the mean from 500 Monte Carlo simulation runs including process and mismatch variations from foundry-supplied device models.

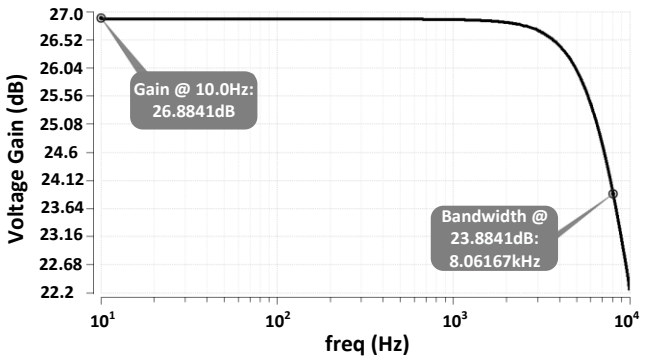


Fig. 6. Simulated voltage gain of the chopper IA without LPF.

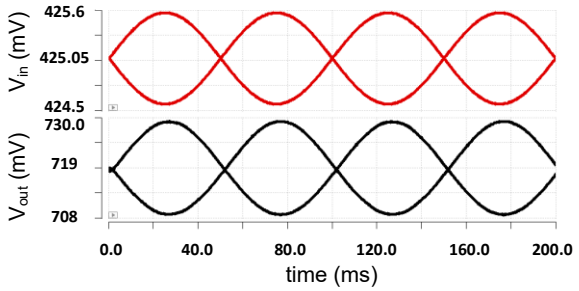


Fig. 7. IA input voltages (top), and output voltages after the LPF (bottom) from transient simulation with a differential input signal of $1mV_{pk\text{-}pk}$.

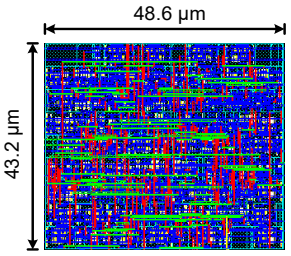
after the LPF from a simulation with a 1 $mV_{pk\text{-}pk}$ differential input.

B. Calibration Block Results

The clock used for calibration is 60 Hz, which is identical to the power supply interference. Therefore, in highly integrated systems-on-a-chip, any unwanted coupling can be suppressed by a notch filter such as in the fully-differential front-end in [6]. The calibration process is illustrated by the results in Fig. 8, which are from a simulation in which the IA was biased properly but no AC input signal was applied. It can be seen that each code is applied for six clock cycles prior to incrementing it. The signals labelled as (S_0, S_1, S_2 and S_3) are the least significant digital bits connected to the NCGFB block, while the rest of the control bits are not shown for simplicity. The switches inside the NCGFB are PMOS transistors, which is why the digital bits Fig. 8 represented the inverted bits of a code. Oscillation onset detection occurs at the code {00001001}. After this instant, the code for the NCGFB is decremented by two bits to {00000111}, which is the optimum code. The layout of the digital calibration block and its specifications are provided in Fig. 9.

V. Conclusions

A chopper-fully symmetric IA with continuous calibration is presented in IBM 0.13-µm BICMOS technology. The chopper technique reduced the total input referred noise by 16 times relative to the same IA but without chopping technique. The calibration process operating continuously in the background to compensate for any real time changes of the input capacitances which results in a high input impedance with a guaranteed stability. The simulation of the transistor level of the IA and the digital calibration block is done using AMS cadence tool. The IA and calibration block consuming 115.9 µW and 176 nW, respectively from 1.2 V supply.



Specification	Value
Number of Gates	140
Area of Standard Cells	1890 µm^2
Core Layout Area	2100 µm^2
Power Consumption	176 nW

Fig. 9. Layout of the digital calibration block and its specifications from synthesis using the foundry-supplied standard digital library.

VI. Acknowledgement

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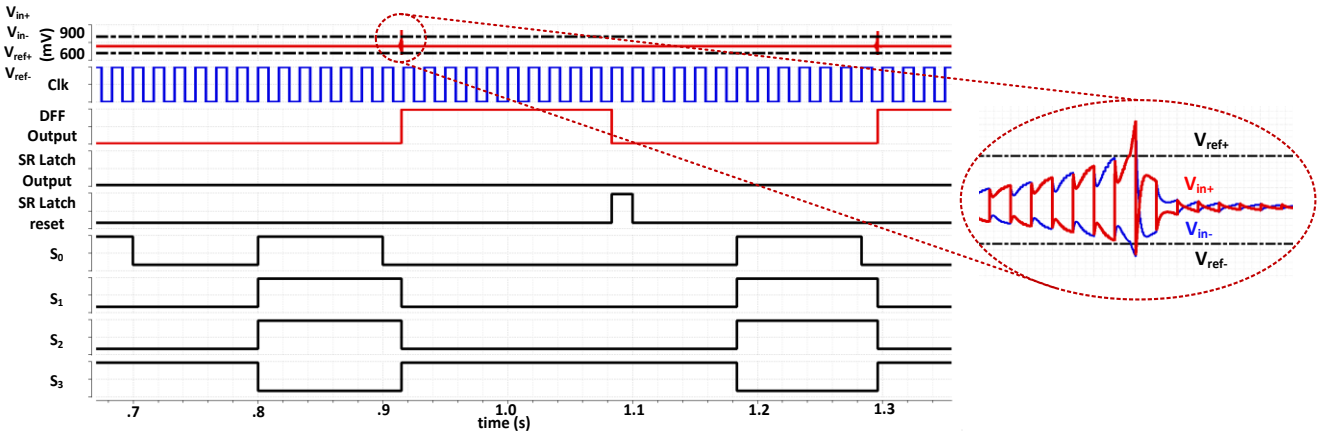

Fig. 8. Simulation of the automatic digital calibration to adjust the NCGFB code for IA input impedance optimization.