

A 9.6 nW, 8-Bit, 100 S/s Envelope-to-Digital Converter for Respiratory Monitoring

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Abstract—The signal's envelope contains important features for a host of applications empowered by machine learning algorithms. Conventionally, the raw analog signal is digitized first, followed by feature extraction in the digital domain. This brief presents an ultra-low-power envelope-to-digital converter (EDC), with respiratory monitoring as one of its applications. The EDC consists of a passive switched-capacitor envelope detector and an inseparable successive-approximation-register analog-to-digital converter (ADC). The two blocks at different sampling rates directly integrate without a buffer between them thanks to a ping-pong operation of their sampling capacitors. An EDC prototype was fabricated in a 180-nm CMOS. It provides 7.1 effective bits of ADC resolution and supports input signal bandwidth up to 5 kHz and an envelope bandwidth up to 50 Hz while consuming 9.6 nW.

Index Terms—Envelope-to-digital converter, ultra-low power, analog circuit for feature extraction.

I. INTRODUCTION

EMBEDDED health and fitness electronics currently dominate the market of commercial Internet-of-Things (IoT) devices. A key challenge is to efficiently extract the biological signal features needed to diagnose a condition or trigger an alert. Traditionally, feature extraction has been done by sampling the audio input in its Nyquist-rate and performing digital signal processing (DSP), as shown in Fig. 1(a). However, this process is not efficient in power and bandwidth because the Nyquist-rate analog-to-digital (A-D) conversion preserves the raw signal but the desired feature usually has a much lower bandwidth than the raw signal. For instance, the bandwidth of the envelope of breathing sound is within 10 Hz but the bandwidth of raw breathing sound extends up to 2 kHz [1], requiring a 4kS/s A-D converter (ADC) which dominates the power budget and limits the lifetime of a small always-on, embedded sensor that constantly monitors the breathing rate; meanwhile, every second, 4k samples are transmitted and processed, a much greater number than necessary.

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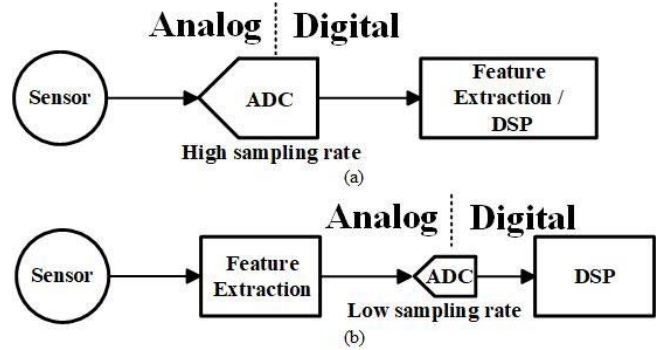


Fig. 1. Conventional Nyquist-rate A-D conversion (a) versus Analog-to-feature conversion (b).

The envelope is a commonly used feature for acoustic signals [2], [3]; for example, in lung auscultation, the patient's breathing rate and breathing conditions can be extracted from the envelope of the auscultation sound [2], [3], [4]. Apart from biomedical applications, envelopes can be used to indicate signal strength [5], [6] and serve as the key feature of a wake-up circuitry that triggers a powerful but high-power consumption system.

The conventional envelope-extraction approach digitizes the original signal in its Nyquist rate and uses DSP such as Hilbert transform [2] to achieve the sound envelope. By performing feature extraction in the analog domain, ADC and DSP could operate under the feature rate rather than Nyquist rate; under the assumption that the feature rate is smaller than the Nyquist rate of the raw signal, the power consumption significantly benefits from the analog-feature-extraction approach [7].

In this brief, we employ an analog-to-feature conversion approach, depicted in Fig. 1(b), to realize an envelope-to-digital converter (EDC) in an efficient manner. The EDC performs envelop extraction and low-rate digitization by inseparable circuits and saves power and bandwidth from the conventional Nyquist-rate signal-acquisition approach [8].

This brief is outlined as follows. Sections II and III present the architecture and circuit implementation of the proposed EDC, respectively. Section IV reports measurement results, followed by conclusions in Section V.

II. PROPOSED EDC ARCHITECTURE

Fig. 2 shows the overall block diagram of the proposed ultra-low-power EDC. The EDC integrates a passive switched-capacitor (SC) envelope detector with an inseparable low-rate successive approximation register (SAR) ADC. Traditional

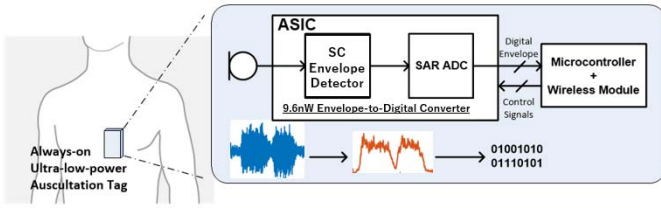


Fig. 2. System block diagram of the proposed EDC.

diode-based rectifiers [9] or class-AB current conveyors [6] could extract the envelope effectively, but they are challenging to integrate due to large capacitors required for low-frequency envelopes. They are also unfit for low-power and low-voltage designs, as they need large bias voltages to turn on their diodes [9] and their large load capacitors are power consuming to drive [6], [13].

The SC envelope detector has a 10kHz sampling rate and supports input signal bandwidth up to 5kHz. Subsequently, the special 100S/s, 8-bit SAR ADC samples the extracted envelope. The SC envelope detector and the SAR ADC operate at different sampling rates but directly integrate without a buffer between them because of a ping-pong scheme detailed in the next Section. The elimination of the buffer saves a significant amount of power.

III. CIRCUIT IMPLEMENTATION

The overall circuit schematic of the proposed EDC appears in Fig. 3, with its critical timing illustrated in Fig. 4.

A. SC Envelope Detector

The SC envelope detector, shown in Fig. 5, contains a polarity detector and a differential first-order low-pass filter, performing rectification and low-pass filtering to the single-ended input signal at a clock frequency above twice the input bandwidth. The polarity detection is achieved by a clocked comparator, which is same to the one in [7]. In ϕ_1 , the polarity detector determines the sign of the signal, which controls the first switch in both paths. Depending on its polarity, the input signal feeds into either the positive or negative path. ϕ_{1a} is a slightly advanced version of ϕ_1 .

This topology rectifies the single-ended input signal and converts it into a differential form. Each path has two capacitors, the sampling capacitor (C_S) and the holding capacitor (C_H). The frequency of ϕ_1 and ϕ_2 is 10kHz to support an input bandwidth up to 5kHz. For the circuit in Fig. 5, we have

$$(C_S + C_H)v_{CH+}[n] = C_S V_{in}[n] \cdot \left(\frac{1}{2} + \frac{1}{2} \text{sgn}(V_{in}[n]) \right) + C_H v_{CH+}[n-1] + C_S v_{CH+}[n-1] \times \left(\frac{1}{2} - \frac{1}{2} \text{sgn}(V_{in}[n]) \right) \quad (1)$$

and

$$(C_S + C_H)v_{CH-}[n] = C_S V_{in}[n] \cdot \left(\frac{1}{2} - \frac{1}{2} \text{sgn}(V_{in}[n]) \right) + C_H v_{CH-}[n-1] + C_S v_{CH-}[n-1] \times \left(\frac{1}{2} + \frac{1}{2} \text{sgn}(V_{in}[n]) \right) \quad (2)$$

If we define the common mode and differential mode component as $v_{out,cm} = (v_{CH+} + v_{CH-})/2$ and $v_{out} = v_{CH+} - v_{CH-}$. By subtracting (2) from (1), we get

$$(C_S + C_H)v_{out}[n] = C_S |V_{in}[n]| + C_H v_{out}[n-1] + C_S \left\{ \frac{1}{2} v_{out}[n-1] - v_{out,cm}[n-1] \cdot \text{sgn}(V_{in}[n]) \right\}. \quad (3)$$

Note that $V_{in}[n] \cdot \text{sgn}(V_{in}[n]) = |V_{in}[n]|$ and V_{in} is referenced to the DC bias voltage V_{CM} in the polarity detection (V_{CM} is the signal ground in the EDC). Assuming $v_{out,cm} \approx 0$, for V_{in} being an amplitude modulated signal, (3) becomes:

$$(C_S + C_H)v_{out}[n] = C_S |V_{in}[n]| + C_H v_{out}[n-1] + C_S \frac{1}{2} v_{out}[n-1] \quad (4)$$

In the z -domain, the transfer function is

$$v_{out}(z) = \frac{1}{1 + \frac{C_H}{C_S} - \left(\frac{C_H}{C_S} + \frac{1}{2} \right) z^{-1}} Z\{|V_{in}|\} \quad (5)$$

where $v_{out}(z)$ and $Z\{|V_{in}|\}$ are the z -transforms of v_{out} and $|V_{in}|$, respectively. The derived z -transfer function reveals that the SC envelope detector rectifies the input and then low-pass filters the rectified signal. Therefore, the overall circuit behaves as an envelope detector.

The C_S is 500fF and the C_H is 12pF in this design. The size and ratio of the capacitors are in which acceptable thermal noise and sufficient low-pass filtering are both achieved. Theoretically, the envelope detector has an envelope conversion gain of 1.2. Off-chip capacitors are supported through the off-chip pads, shown in Fig. 3, if further signal attenuation is needed. The pads also serve as input terminals to test the ADC alone.

B. SAR ADC and the Ping-Pong Scheme

The SAR ADC consists of a capacitive digital-to-analog converter (DAC), a clocked dynamic comparator, an SAR control logic, and sampling capacitors $C_{S,SAR}$. Fig. 6 shows the proposed SAR ADC, which directly interfaces the passive SC envelope detector without needing a buffer between them. The elimination of a buffer is realized by a ping-pong operation. The basic idea is to duplicate the sampling capacitor C_S in the SC envelope detector. The duplicated capacitor $C_{S,SAR}$ has the same value as the C_S .

In Fig. 5, the envelope information is stored in both C_H and C_S during ϕ_2 . While C_H tracks the integration history and its charge must not be altered at any time, C_S is refreshed during ϕ_1 and its stored charge can be used for A-D conversion, provided that there is another C_S to relay the input sampling operation in the envelope-detection circuit. Therefore, we propose to share, in a ping-pong manner, the sampling capacitor in the SAR ADC ($C_{S,SAR}$ in Fig. 6) and in the envelope detector (C_S in Fig. 5). That is, C_S and $C_{S,SAR}$ take turn to serve in envelope detector. After each A-D conversion cycle, C_S will be standby and $C_{S,SAR}$ will sample the envelope.

Instead of the conventional way of sampling the input into the DAC capacitors, the SAR ADC uses a separated sampling capacitor $C_{S,SAR}$ [10], as seen in Fig. 6, for two reasons. First, it accommodates the ping-pong operation of C_S and $C_{S,SAR}$, as described above. Second, by a separated $C_{S,SAR}$, the sizes

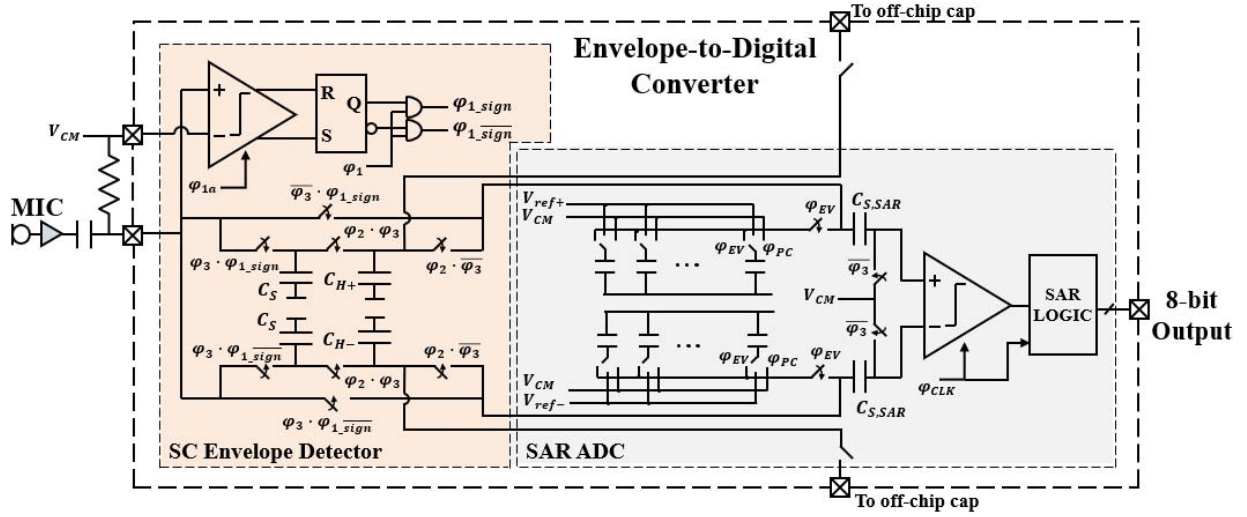


Fig. 3. Circuit implementation of proposed EDC.

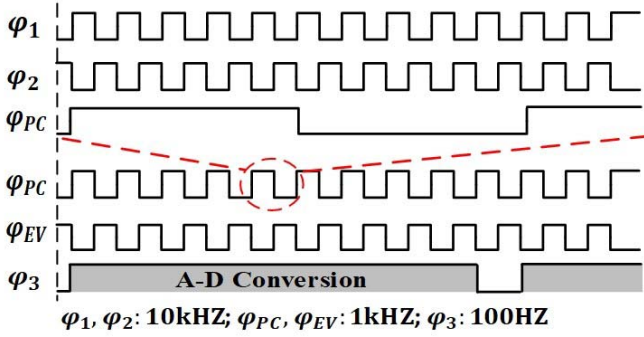


Fig. 4. Critical timing of the proposed EDC.

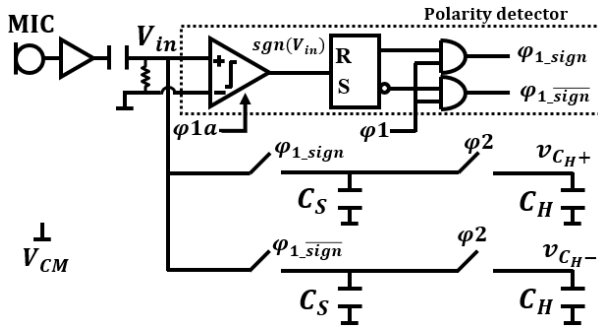


Fig. 5. SC envelope detector.

of the DAC unit capacitor and $C_{S,SAR}$ can be optimized independently for ADC performance and for the EDC's load to the input signal source.

The DAC operates at 100Hz in two phases: the pre-charging phase ϕ_{PC} and evaluation phase ϕ_{EV} . During ϕ_{PC} , the binary-weighted capacitors in DAC are pre-charged to a certain DC voltage controlled by the SAR logic. In ϕ_{EV} , the DAC voltage and the sampled signal are subtracted at the inputs of the comparator, which decides to increase or decrease the SAR register's content. The ADC's comparator has same the topology as the comparator in envelope detector. By slightly delaying ϕ_{EV} , the phase ϕ_{CLK} is used to control the comparator and SAR logic block. Because the voltages in the sampling

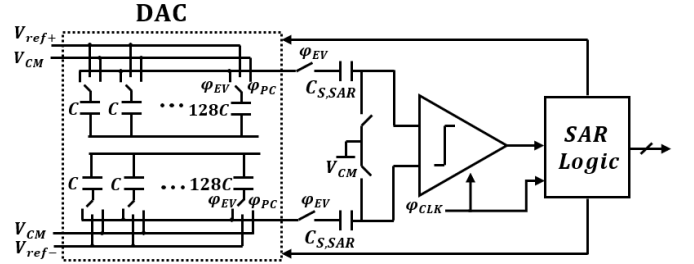
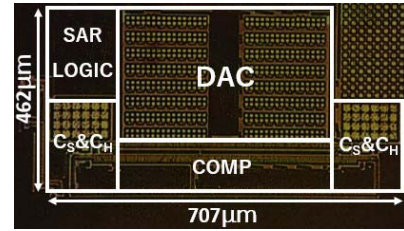
Fig. 6. SAR ADC with shared sampling capacitor C_S . $C_{S,SAR}$ is interchanged with C_S in Fig. 5 in a ping-pong manner to avoid a power-consuming buffer.

Fig. 7. Die photograph.

capacitors are rectified, the DAC only needs a unipolar output and uses an asymmetric reference voltage scheme.

The DAC's unit capacitor is 100fF, which is 4 times larger than the minimum achievable value. A large unit capacitor provides two advantages to this design. First, as the ADC operates under a slow sampling rate, charge leakage can be relieved by a larger unit capacitor. Second, the linearity and gain of the DAC improve because the switch charge injection and the parasitic capacitors of $C_{S,SAR}$ become less significant to a larger DAC.

The ADC operates at 0.6V except for the SAR logic, which runs from 0.4V to optimize power consumption at low operating frequencies. The common-mode voltage V_{CM} for the SC envelope detector and the ADC is 0.3V.

IV. EXPERIMENTAL RESULTS

The EDC prototype was fabricated in a 180nm CMOS process. Fig. 7 shows the die photograph of the chip, which

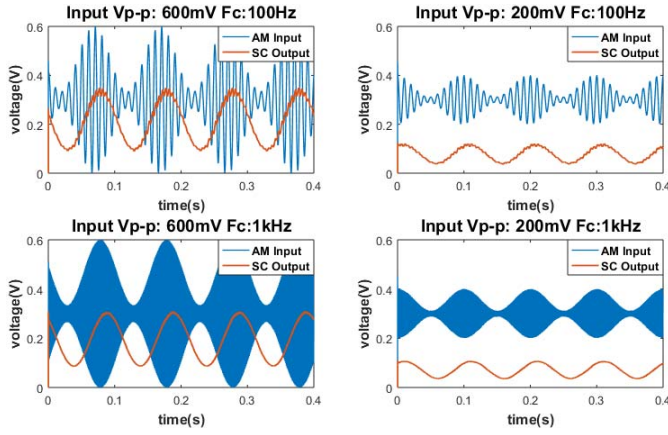


Fig. 8. SC envelope detector outputs for AM signals with different carrier frequencies F_c (100Hz/1kHz) and amplitudes (0.6Vp-p/0.2Vp-p).

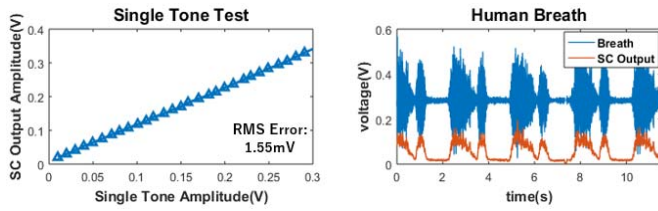


Fig. 9. Single tone test (left) and human breath clips (right).

occupies 0.32 mm² total area. The EDC is designed to support a wide range of applications with various target frequencies; hence, a programmable off-chip microcontroller is employed to generate the clocks. The microcontroller is sufficiently fast to provide the synchronized clock. Simulations show that the clock generation and switch driving circuits consume a few nano-Watts, which will not dominate the power budget if they are implemented on chip.

The SC envelope detector alone is tested with amplitude modulated (AM) signals. As shown in Fig. 8, 100Hz and 1kHz carriers are modulated by a 10Hz signal of varying magnitude. The SC envelope detector tracks the 10Hz sinusoidal envelope and removes the carrier. It exhibits more attenuation to the carrier with higher frequency, which is in agreement with the transfer function described in (5). Single-tone tests are also conducted with a 1kHz pure sinusoidal signal to examine the accuracy of the SC circuit (Fig. 9 left). The SC envelope detector achieves an amplitude RMS error less than 1.55mV, which indicates the circuit is linear. The conversion gain is 1.2, the same as the theoretical value. To demonstrate its capability to detect real biological sounds, human breath sound clips are used; the breath signal and SC output are shown in the right of Fig. 9.

The SAR ADC in this chip can be tested alone by applying an input signal across the output pins (pads labelled “To off-chip cap” in Fig. 3) of the SC envelope detector. The ADC consumes 6nW at 100S/s sampling rate. A 5Hz, 0.59V_{P-P} sinusoidal wave is used to test the dynamic performance of the ADC. The ADC achieves a 44dB signal-to-noise-and-distortion ratio (SNDR), corresponding to a 7.1 effective number of bits (ENOB). As the SC envelope detector is intrinsically nonlinear due to its rectification operation, the linearity of the entire EDC is not characterized.

To illustrate its capability to monitor respiratory rate, we conducted a real-life-scenario experiment that involves human

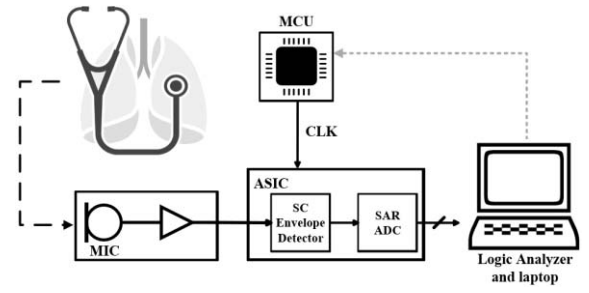


Fig. 10. Experiment setup for respiratory rate monitoring. The control clock is provided by an off-chip micro control unit (MCU).

TABLE I
BREATH RATE ESTIMATION ERROR SUMMARY

True Breath Rate (per min)	Measured Mean and Standard deviation
4	4.016±0.208
8	8.003±0.094
12	11.847±0.130
16	15.791±0.165
20	19.750±0.086
24	23.665±0.099
28	27.623±0.222
32	31.410±0.433

subjects. An off-the-shelf clinic stethoscope was attached to the chest of the participant. To acquire the sound, a microphone is assembled into the rubber tube of the stethoscope. To set a reference to the subjects' breathing rate, beeps with programed frequencies are generated by the speaker of a laptop during the testing [2]. Three participants were instructed to take breaths according to the beep rate; thus their breath rates are considered equal to the preset value in the laptop. The respiratory rate in the experiment ranges from 4 breaths per minute (BPM) to 32 BPM with a step size of 4 BPM. EDC's outputs were collected and analyzed. Fig. 10 illustrates the experiment setup. As reported in [2], breath rate can be rightly estimated by the power spectral density (PSD) of the respiratory signal's envelope. The collected data are analyzed using MATLAB to compute the PSD and find the actual breath rate. An example of the collected envelope and its PSD appears in Fig. 11. The means and standard deviations of estimated breath rates are listed in Table I. Although the raw breath sounds acquired by the stethoscope contain noises like heart beats, which also appear in Fig. 11 (a), the captured envelopes present high accuracy in monitoring breath rates.

The functionality of the EDC is further evaluated by four kinds of physiological respiratory sounds: vesicular sounds, diminished vesicular sounds, bronchial sounds and bronchovesicular sounds. The input to the EDC is from a waveform generator that produces signals from clinic recording data. Fig. 12 shows the successfully extracted envelopes of those four sounds. The EDC's outputs for those four sounds exhibit differently in the shape and amplitude of their envelopes. This enables accurately classifying and monitoring breath sounds in lung auscultation as in [3].

Table II summarizes the performance of the proposed EDC. The entire EDC consumes 9.6nW with 100S/s sampling frequency of the ADC. Its energy efficiency compares

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This work	[5]	[6]	[13]	[8]	[11]	[12]
Application	Respiratory Monitoring	Wake Up Circuit	Bionic Ear Processor	EMG readout	ECG-Monitoring	Signal Acquisition	Biomedical Sensing
Feature	Envelope	Signal energy	Envelope	Envelope	Raw ECG	Raw Signal	Raw ECG
Technology	180nm	90nm	1.5 μ m	180nm	65nm	65nm	350um
Supply	0.6V/0.4V	N/A	2.8V	1.5V	0.6V	0.6V	1V
Bandwidth	5kHz (raw signal) 50Hz (feature)	2kHz	100Hz-10kHz	500Hz	250Hz	500Hz	31Hz-292Hz
ENOB of ADC	7.1-bit	N/A	N/A	9.2-bit	N/A	7.14-bit	10.2-bit
Power	9.6 nW*	700nW	875nW	19 μ W	18.6nW	3nW	445nW-895nW
Power Configuration	Envelope detector, ADC**	Wake up detector	Envelope detector	PreAmp, Envelope detector, ADC	PreAmp, ADC	PreAmp, ADC	PreAmp, ADC

* Clock generation is not included. The DAC, SAR logic, envelop detector consumes 4.8nW, 1.1nW, and 3.6nW, respectively.

** Preamplifier (PreAmp) is not implemented in this design. Estimated from [11], preamplifier power is 9nW

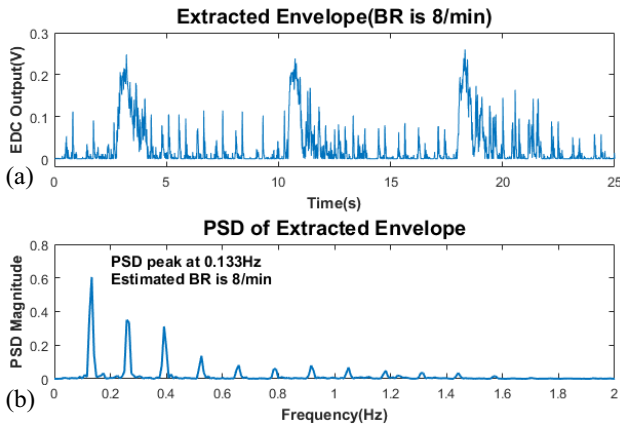


Fig. 11. An example of the respiratory rate estimation: (a) Breath sound's envelope from EDC's output. (b) Computed PSD of the extracted envelope.

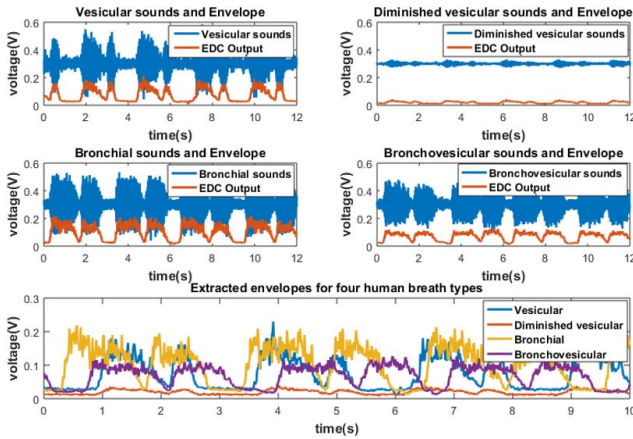


Fig. 12. EDC outputs for various auscultation recordings.

favorably to existing circuits for similar applications, as shown in Table II.

V. CONCLUSION

We presented an EDC for respiratory monitoring that demonstrates the concept of the analog-to-feature conversion by removing redundancy in A-D conversion and data transmission. The EDC consists of a passive SC envelope detector and an inseparable SAR ADC. They operate at

different sampling rates but interface directly without a buffer between them, enabled by a ping-pong operation of their sampling capacitors. The proposed EDC consumes 9.6nW power in a 100S/s output data rate and supports input bandwidth up to 5kHz. Experimental results show that the EDC is able to extract envelopes from various respiratory sounds and the respiratory rate can be successfully computed from the extracted envelopes. This design enables monitoring of respiratory conditions, including counting breath rates in nW power thereby dramatically extending the lifetime of these always-on, energy-conscious IoT devices.

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