Applied Physics Letters

Using single-electron box arrays for voltage sensing applications

Cite as: Appl. Phys. Lett. **116**, 213103 (2020); https://doi.org/10.1063/5.0005425
Submitted: 20 February 2020 . Accepted: 05 May 2020 . Published Online: 26 May 2020

Matthew J. Filmer, Thomas A. Zirkle, Jonathan Chisum, Alexei O. Orlov, and Gregory L. Snider

Applied Physics Letters ARTICLE scitation.org/journal/apl

Using single-electron box arrays for voltage sensing applications

Cite as: Appl. Phys. Lett. **116**, 213103 (2020); doi: 10.1063/5.0005425
Submitted: 20 February 2020 · Accepted: 5 May 2020 ·
Published Online: 26 May 2020

Matthew J. Filmer,[a] Thomas A. Zirkle,[b] Jonathan Chisum, Alexei O. Orlov, and Gregory L. Snider

AFFILIATIONS

University of Notre Dame, Notre Dame, Indiana 46556, USA

[a]**Author to whom correspondence should be addressed:** mfilmer@nd.edu
[b]**Present address:** Northrop Grumman Ogden, Utah 84405, USA.

ABSTRACT

Single-electron tunneling transistors (SETs) and boxes (SEBs) belong to the family of charge-sensitive electronic devices based on the phenomenon of Coulomb blockade. An SEB is a two-terminal device composed of "leaky," C_j, and "non-leaky," C_g, nanoscaled capacitors in series. At low temperatures, the charge at the common node is quantized and can only be changed near energy-population degeneracy points, resulting in periodic oscillations of the SEB admittance as a function of voltage applied to C_g. In comparison to the SETs, SEBs have higher operating temperature, are electrostatic discharge tolerant, and have a much smaller footprint. To monitor the SEB admittance, Radio Frequency reflectometry can be used. To improve the signal-to-noise ratio, limited by the small change in admittance in an SEB, multiple devices sharing the same source and gate electrodes are connected in parallel to form arrays of SEBs. Due to unavoidable random offset charges, the signal boost for an array of N SEBs is expected to be $\sim\sqrt{N}$. We experimentally demonstrate that by carefully choosing the operating point, the response to the voltage on the sensing gate can be enhanced, for small arrays scales, by a factor approaching N and, thus, provides a method by which these devices can be used in practical sensing applications, such as a scanning probe.

Single-electron transistors are very sensitive electrometers that enable charge sensing with unprecedented sensitivities, down to 10^{-6} e/Hz$^{1/2}$.[1] A typical SET is composed of a nanoscale "island" coupled to the outside world by two nanoscale "leaky capacitors" forming tunnel junctions (TJs), with parameters C_j (junction capacitance) and R_j (junction resistance), as well as a non-leaky gate capacitance, C_g. Single-electron boxes (SEBs)[2] are very similar to SETs except they are composed of only one TJ and a gate capacitor [Fig. 1(a)]. At low temperatures ($T \ll E_c/k$, where $E_c = e^2/2C_\Sigma$ and $C_\Sigma = C_j + C_g$, in which e is the electron charge and k is the Boltzman constant), the electron population on the island is quantized due to Coulomb blockade.[3] At low temperature, as gate voltage is swept, the energy added to the system by the gate periodically overcomes Coulomb blockade. The electron population of the island at these energy degeneracy points changes one by one in a stepwise manner.[4] The use of only one junction in SEBs reduces C_Σ and increases the operating temperature, an important feature for scanning probe microscopy applications (see the supplementary material, Fig. S1 for more information). When designing single electron devices to operate at a desired temperature, the primary constraint is the total island capacitance. SEBs can allocate more of the capacitance budget to the gate capacitance, which can further enhance the performance of an SEB compared to an SET. An example of an SEB fabricated by the Dolan bridge (DB) method[5] is shown in Fig. 1(b). For the device shown, the size of the junction is about 900 nm^2, resulting in a charging energy of $E_c \geq 3$ meV and enabling robust operation at temperatures as high as 10 K.

Despite their simplicity, SEBs are not used in practical applications due to the difficulty presented by the lack of a DC path through the device. Early investigations used a separate SET integrated with an SEB to read out the charge state of the SEB, and conventional measurements limited the bandwidth to a few kHz.[6] Recently, it was discovered that radio frequency (RF) reflectometry[6] measurements could be used to directly probe the charge state of the SEB in bandwidths up to tens of MHz[7,8] This technique, called "gate-reflectometry," is also frequently used for low temperature measurements of other devices such as semiconductor qubits.[9,10]

A way to increase the admittance of the sensing single-electron devices while keeping high voltage sensitivity was experimentally studied by Gustavsson *et al.*[11] using an array of 200 parallel connected SETs. However, unavoidable random background charges will shift the thresholds of individual devices, and at moderately low temperatures, $T \sim E_c/3k$, the averaged conductance of the array scales as an

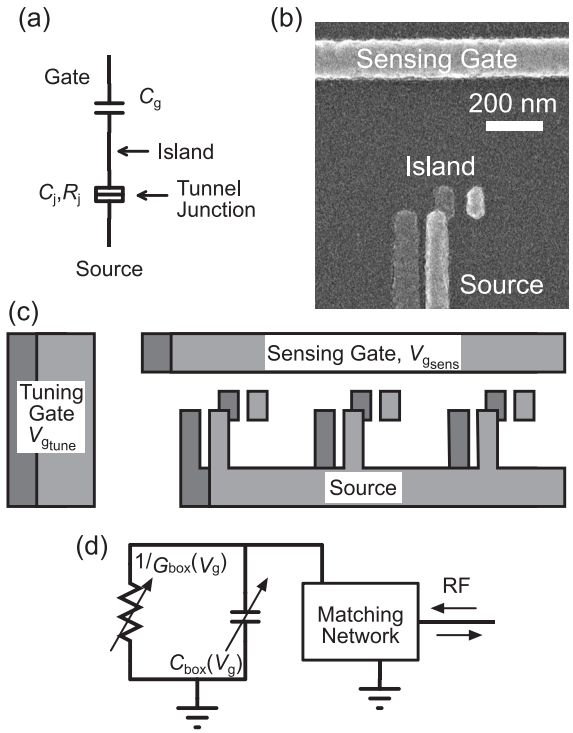

FIG. 1. (a) Electrical circuit of an SEB. (b) An SEM micrograph of SEBs fabricated by the Dolan bridge technique. (c) Representative layout of an array of SEBs fabricated using the Dolan bridge process. (d) Equivalent circuit of SEBs with a matching network.

incoherent sum of sine functions: $N^{1/2}$. Any small variation in coupling results in a beating pattern in the transfer function. By biasing the array in a region with constructive interference, giving higher values of slopes of the transfer function, $d|Y|/dV_g$, it was estimated that the sensitivity can be increased by a factor of 2.[11]

In this work, we study the performance of arrays of SEBs (SEBAs) in parallel for voltage sensing applications such as a scanning probe. The studied device structure makes use of a sensing gate with approximately equal coupling to each island, as well as a tuning gate with varying coupling to each island. A schematic representation of this layout for a 3 box array is shown in Fig. 1(c). Similar to the SET array,[11] the maxima in the admittance of an array composed of N SEBs in parallel are expected to scale in the same manner. However, three important features distinguish SEB arrays from SET arrays. First, while charging energy and, thus, operating temperature of an SET array are dictated by the lowest charging energy device and, thus, even one shorted SET will lead to failure of the whole array, in SEBAs, the lowest charging energy devices will just contribute less (and even SEBs with shorted junctions will only reduce the number of active devices) but not impede the sensitivity of the rest of the array. Second, since no DC currents flow across the junctions, there is no contribution from shot noise.[11] Third, SEBAs are almost completely immune to electrostatic discharge (ESD). While SETs are notoriously prone to ESD and have to be handled with extreme caution, the SEBAs we experimentally studied survived tens of thermal cycles and were connected and disconnected to various experimental setups, and components were added to the devices already connected, etc., without any degradation of performance.

From the standpoint of circuit design, the SEB represents a two-terminal voltage-controlled variable admittance (Y). When Coulomb blockade prohibits electron transfer through the junction, its admittance approaches that of two capacitors C_j and C_g in series, while when the Coulomb blockade is lifted, the magnitude of its admittance is maximized. Near charge degeneracy points, two mechanisms associated with the underlying physics of single electron charge transfer must be taken into account for evaluation of admittance changes in the SEB. One is the so-called Sisyphus resistance[7]—excess dissipation at frequencies $\omega \geq \Gamma$—which for a given temperature T is approximately $\Gamma = 2kT/e^2R_j$ at the degeneracy point, where ω is the RF excitation frequency and R_j is the junction resistance. The second effect is the enhancement of capacitance due to the ability of an electron to travel through the junction—the dynamic input capacitance.[12] These two components of total admittance change as the device goes in and out of blockade, resulting in phase and magnitude variations in the reflected signal and yielding an equivalent circuit of a parallel combination of (G_{box}) and (C_{box})[13] shown in Fig. 1(d),

$$\begin{aligned} Y &= G_{box} + j\omega C_{box}, \\ G_{box} &= \frac{e^2\alpha^2\gamma}{4kT}\left(\frac{\gamma^2}{\omega^2}+1\right)^{-1}\cosh^{-2}\left(\frac{-e\alpha\Delta V_g}{2kT}\right), \\ C_{box} &= \frac{e^2\alpha^2}{4kT}\left(\frac{\omega^2}{\gamma^2}+1\right)^{-1}\cosh^{-2}\left(\frac{-e\alpha\Delta V_g}{2kT}\right). \end{aligned} \tag{1}$$

Here, $\alpha = C_g/(C_g + C_j)$ is the lever arm factor of the gate, ΔV_g is the gate voltage relative to an SEB population degeneracy point, and γ is the net tunnel rate. The magnitude of oscillation of both components of admittance for one SEB shown in Fig. 1(b) is much smaller than the respective magnitude of conductance oscillations in the SET with the same parameters C_j, C_g, and R_j.

To simulate the response of an array of boxes, the summation is taken of the admittance of N individual boxes assuming no interaction between them. It is difficult to directly measure the junction parameters of an SEB, and so the arrays simulated for this work were composed of boxes with parameters based on a typical SET of similar structure:[14] $R_j = 49\ \text{k}\Omega$, $C_j = 20$ aF, $T = 2.4$ K, and $\omega = 2\pi \times 300$ MHz. Two sets of arrays were simulated using different C_g values. For the first, $C_g = 2.9$ aF, which corresponds to SEBs with the same structure as the SET but without the drain side TJ. The second, $C_g = 22.9$ aF, corresponds to SEBs with the same capacitance budget (42.9 aF) as the SET, with the extra 20 aF capacitance allocated to the gate. To simulate expected lithographic variation between individual boxes, the gate capacitances were randomized according to a Gaussian distribution using the previous values as the mean and a standard deviation of 10% of that mean, and the junction capacitances and conductances were likewise randomized with a standard deviation of 15% of the mean, which is typical of the devices fabricated for this work. Finally, to account for unpredictable background charge, each box is given a uniformly random phase shift across its period. These arrays are simulated across a V_g range of both 100 mV and 10 V. The maximum slope of the response curve corresponds to the maximum sensitivity. Therefore, for each simulated array, the maximum derivative of $|Y|$ in the simulated V_g range is extracted. Each array is simulated 100 times, with new randomized values each time and the mean value extracted.

The result of these simulations is shown in Fig. 2. It is apparent that a higher gate capacitance results in a large increase in sensitivity. This occurs for two reasons. First, the peak values of both components of Y are proportional to α^2, and second, as C_g increases, the Coulomb blockade oscillations are compressed in V_g, increasing the derivative and, therefore, increasing the sensitivity. In the plot, dashed lines indicate scaling proportional to $N^{1/2}$, the predicted scaling from a similar analysis conducted for an array of SETs by Gustavsson *et al.*,[11] and N, the maximum possible scaling, which occurs when all N boxes are in perfect alignment. The mean value across each repetition is given by the solid curves. From these, it is clear that in both cases, the peak sensitivity scales proportional to $N^{1/2}$. However, searching across a wider V_g range gives more of an opportunity to find a high sensitivity region, resulting in a higher sensitivity for all array sizes. For the smallest arrays, those less than around 5 SEBs, the scaling is proportional to N when measuring a wide V_g range. This indicates that for small arrays, it is likely to find a region where all N boxes converge in the V_g ranges investigated.

To compare a SEBA with a SET with the same 42.9 aF total capacitance budget ($C_j = 20$ aF, C_g=2.9 aF), the sensitivity of the SET is included in Fig. 2 as a horizontal dashed line. From this, we conclude that SEBAs can compete with SETs for $N > 8$.

Devices for this work are fabricated on fused-silica substrates using high resolution e-beam lithography and the Niemeyer–Dolan shadow evaporation technique to define Al/AlO_x tunnel junctions (see the study by Zirkle *et al.*[14] for more fabrication details, and see Fig. S1 in the supplementary material for images of fabricated devices). Experiments are performed in the temperature range of 0.3–10 K. To suppress the superconductivity of Al, the samples were glued to the surface of small permanent magnets with a field strength of about 0.4 T at the surface. To evaluate junction resistance, SETs with the same design parameters are fabricated in close proximity to SEBAs. We consistently fabricate SETs with $E_c > 1$ meV.[14]

To characterize the response of the SEBA, we perform a standard single-port reflectometry measurement using a UHF lock-in amplifier by Zurich Instruments [for setup information, see the supplementary material, Fig. S2(a)]. The device or array to be measured is connected to a π matching network [supplementary material, Figs. S2(b) and S2(c)]. The matching network is designed to maximize changes in the reflected signal caused by variations of admittance in the SEBA in response to the change in gate voltage. Proper design of the matching network for an SEBA is a subject of a different publication. A quantitative analysis, which enables the accurate back calculation of device admittance from acquired reflectometry data, is only possible if a properly calibrated system is used. Since our system is not calibrated, we will present qualitative results that are sufficient for the determination of trends and comparison between several arrays measured under the same experimental conditions.

Voltage gain for an SET is determined by the ratio $\alpha_{set} = C_g/C_j$; likewise, this ratio determines the voltage sensitivity of an SEB. For array applications to obtain better sensitivity, it is best to design the sensing gate to maximize this ratio within the available capacitance budget. In practice, a second tuning gate with capacitance $C_{g_{tune}}$ can be used to set the operating point of an array to the steepest slopes of constructive interference peaks within the reachable span of the tuning gate voltage, $V_{g_{tune}}$. An example of the reflectometry signal obtained from array "A" composed of three SEBs and coupled to two gates is presented in Fig. 3 [see supplementary material Fig. S1(a) for the micrograph of the device]. The 2D map in coordinates $V_{g_{sense}}$ and $V_{g_{tune}}$ shows the magnitude of reflection coefficient Γ for array "A." Each SEB generates a set of lines with a distinct slope $\partial V_{g_{tune}}/\partial V_{g_{sense}} = -C_{g_{sense}}/C_{g_{tune}}$. Interference peaks

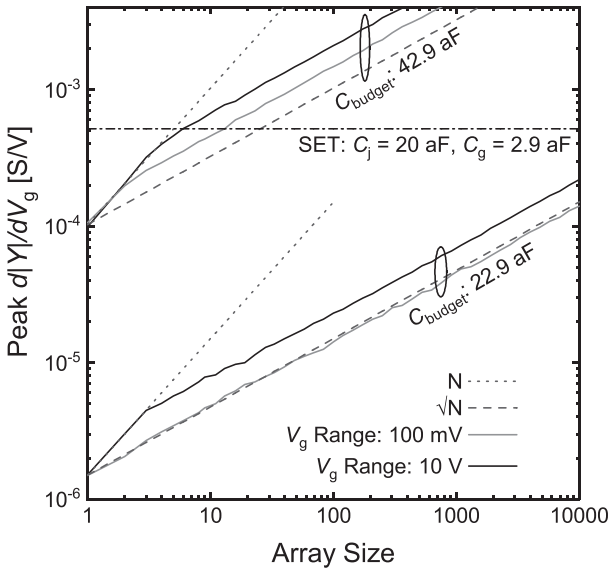

FIG. 2. Plot of the maximum slope of the magnitude of admittance for single electron box arrays of varying sizes. Each data point is the average of 100 simulations of the same array conditions with randomization to account for process variation.

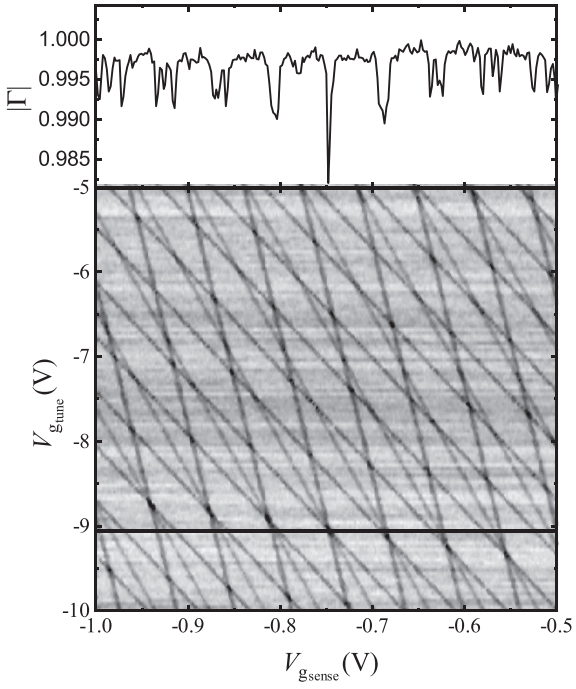

FIG. 3. Plot of the magnitude of reflection coefficient $|\Gamma|$ for array "A" as a function of sensing ($V_{g_{sens}}$) and tuning ($V_{g_{tune}}$) voltages. $T = 0.32$ K; $f = 461$ MHz. A cross section shows a large peak with the steepest slopes.

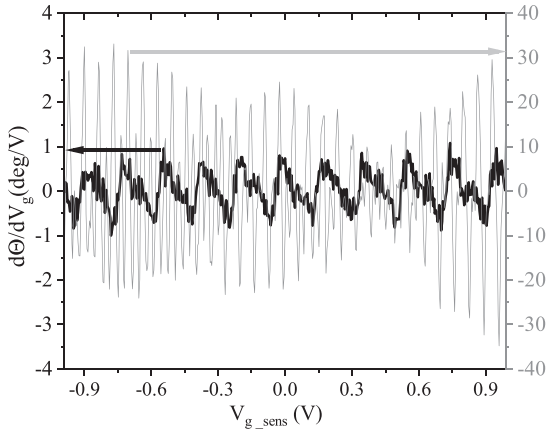

FIG. 4. Relative sensitivities ($d\Theta/dV_g$) of two devices: single SEB (black) and array of 50 SEB (gray) vs sensing gate bias.

appear at the points of line crossings. Note that the spacing between lines in each SEB along the $V_{g_{sense}}$ axis is almost the same, while along the $V_{g_{tune}}$ axis, it is distinctly different, indicating dissimilar capacitance $C_{g_{tune}}$ for each SEB. This combination ensures the appearance of line crossings within an easily accessible span of $V_{g_{tune}}$. Clearly, the use of two gates makes it easier to reach such a high-sensitivity crossing point where the signals add up since to find such a point with a single gate would require a much broader span of $V_{g_{sense}}$. This effect could be expanded, by including additional gates, up to a limit of one gate per SEB. However, it is infeasible to control more than a few gates at a time. The slice at the top of Fig. 3 shows how the signal is greatly increased where the boxes all align, resulting in a stronger signal and a more sensitive sensor (with a steeper slope of the resulting peak). Since all the boxes contribute, the sensitivity to the applied gate voltage, $d\Gamma/dV_g$, increases by $\sim N$ in good correlation with Fig. 2. An estimation of the sensitivity for array "A" at 320 mK was made by comparing the sidebands created by a low frequency modulation of the gate electrode with the level of the noise floor.[1,15] From this measurement, a voltage sensitivity per SEB of $\sim 12\ \mu V/Hz^{1/2}$ was found and is expected to scale proportional to $N^{-1/2}$ (see the supplementary material, Fig. S5 for more information).

To validate trends predicted by simulations for arrays with a large number of SEBs, sensitivity measurements were made of a single SEB and a fabricated array with $N = 50$. To eliminate differences caused by dissimilar matching networks, the same matching network was used for each measurement [see supplementary material Fig. S3(c) for the details of the experimental setup]. The sensitivity in magnitude of the single SEB and array with respect to $V_{g_{sense}}$ is plotted in Fig. 4. An analysis of the expected run-to-run variation for these two devices is given in the supplementary material, Fig. S6. This example also illustrates the premise that devices with smaller E_c (including shorted junctions) simply contribute less to the response of the entire array but do not degrade the performance as in the case of parallel connection of SETs.

To conclude, we demonstrate that the use of arrays of single-electron boxes for sensing applications has some advantages compared to SETs due to higher fabrication density and the elimination of DC currents as a source of shot noise. Single-electron charging of the SEB results in periodic oscillations in its admittance due to excess power dissipation (Sisyphus resistance effect) and deviations from static gate capacitance (dynamic capacitance effect). To boost the measurable signal, SEBs can be connected in parallel. We calculate the expected sensitivity of SEBAs as a function of N for a given set of device parameters in the presence of random background charge and evaluate potential routes to improve sensitivity and tunability of the arrays. By comparing arrays with different numbers of SEBs, we demonstrate that (a) the general trend in scaling of signal response is $\sim N^{1/2}$ and (b) while the performance of a single SEB may vary greatly due to parameter distribution, the performance of the array in contrast to SET arrays will be dictated by the devices with the largest and not smallest charging energy. From these results, we conclude that SEB arrays provide attractive solutions for nanoscale voltage sensing applications, such as scanning probes and on-chip voltage measurements.

See the supplementary material for additional details of fabrication, test, and sensitivity.

This work was supported by National Science Foundation Grant Nos. ECCS-1509087 and DMR-1904610. The authors are grateful to Xavier Jehl and Mark Sanquer for useful discussions and suggestions.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]H. Brenning, S. Kafanov, T. Duty, S. Kubatkin, and P. Delsing, J. Appl. Phys. **100**, 114321 (2006).
[2]P. Lafarge, H. Pothier, E. R. Williams, D. Esteve, C. Urbina, and M. H. Devoret, Z. Phys. B **85**, 327–332 (1991).
[3]K. K. Likharev, Proc. IEEE **87**, 606–632 (1999).
[4]P. Lafarge, P. Joyez, H. Pothier, A. Cleland, T. Holst, D. Esteve, C. Urbina, and M. H. Devoret, C. R. Acad. Sci., Ser. II **314**(9), 883–888 (1992).
[5]T. A. Fulton and G. J. Dolan, Phys. Rev. Lett. **59**, 109–112 (1987).
[6]R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, Science **280**(5367), 1238–1242 (1998).
[7]F. Persson, C. M. Wilson, M. Sandberg, G. Johansson, and P. Delsing, Nano Lett. **10**, 953–957 (2010).
[8]J. I. Colless, A. C. Mahoney, J. M. Hornibrook, A. C. Doherty, H. Lu, A. C. Gossard, and D. J. Reilly, Phys. Rev. Lett. **110**(4), 046805 (2013).
[9]X. G. Croot, S. J. Pauka, M. C. Jarratt, H. Lu, A. C. Gossard, J. D. Watson, G. C. Gardner, S. Fallahi, M. J. Manfra, and D. J. Reilly, Phys. Rev. Appl. **11**(6), 064027 (2019).
[10]A. Crippa, R. Ezzouch, A. Aprá, A. Amisse, R. Laviéville, L. Hutin, B. Bertrand, M. Vinet, M. Urdampilleta, T. Meunier, M. Sanquer, X. Jehl, R. Maurand, and S. De Franceschi, Nat. Commun. **10**(1), 2776 (2019).
[11]S. Gustavsson, D. Gunnarsson, and P. Delsing, Appl. Phys. Lett. **88**(15), 153505 (2006).
[12]N. M. Zimmerman and M. W. Keller, J. Appl. Phys. **87**(12), 8570–8574 (2000).
[13]J. C. Frake, S. Kano, C. Ciccarelli, J. Griffiths, M. Sakamoto, T. Teranishi, Y. Majima, C. G. Smith, and M. R. Buitelaar, Sci. Rep. **5**, 10858 (2015).
[14]T. A. Zirkle, R. A. Bonek, G. L. Snider, and A. O. Orlov, J. Low Temp. Phys. **195**(5), 419–428 (2019).
[15]A. Aassime, D. Gunnarsson, K. Bladh, P. Delsing, and R. Schoelkopf, Appl. Phys. Lett. **79**(24), 4031–4033 (2001).