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Controlling Polarity of $MoTe_2$ Transistors for Monolithic Complementary Logic *via* Schottky Contact Engineering

Xia Liu, Arnob Islam, Jing Guo, and Philip X.-L. Feng*

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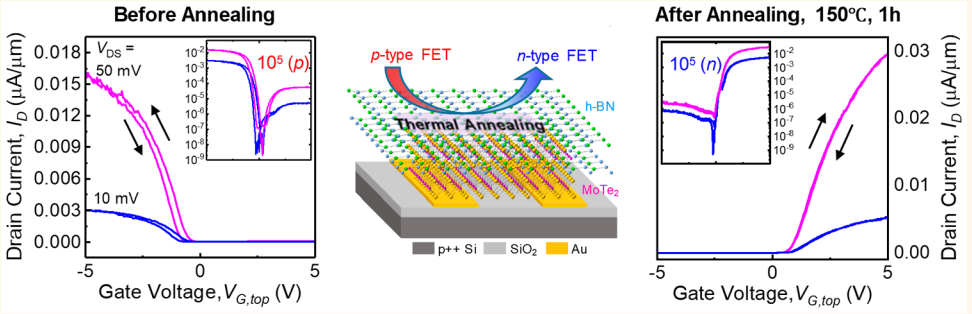

ABSTRACT: **Two-dimensional (2D) layered molybdenum ditelluride ($MoTe_2$) crystals, featuring a low energy barrier in the crystalline phase transition and a sizable band gap close to that of silicon, are rapidly emerging with substantial potential and promise for future nanoelectronics. It has been challenging, however, to realize n-type $MoTe_2$ field-effect transistors (FETs), thus complementary logic, because $MoTe_2$ FETs mainly exhibit p-type behavior. Here, we report a dopant-free method for controlling polarity of $MoTe_2$ FETs by modifying Schottky barriers at their $MoTe_2$−metal contacts *via* thermal annealing. Upon annealing, $MoTe_2$ FETs encapsulated by hexagonal boron nitride (h-BN) are consistently changed from hole to electron conduction, displaying an on/off current ratio of 10^5 or higher. When the $MoTe_2$ channel is sandwiched between top and bottom h-BN thin layers (h-BN/$MoTe_2$/h-BN FETs), higher field-effect mobility is attained, up to 48.1 $cm^2 V^{-1} s^{-1}$ (hole) and 52.4 $cm^2 V^{-1} s^{-1}$ (electron) before and after thermal annealing, respectively. The thermally controlled FET polarity change further enables high-performance $MoTe_2$ monolithic complementary inverters with gain as high as 36, suggesting this simple and effectual approach may lead to compelling possibilities of rationally controlling transport polarity, on demand, in atomically thin transistors with metal contacts and their 2D integrated circuits.**

KEYWORDS: *2D materials, molybdenum ditelluride ($MoTe_2$), transistor polarity, Schottky barrier, semiconductor−metal contact, monolithic inverter, thermal annealing*

Two-dimensional (2D) atomic or molecule sheets of layered semiconductors are natively endowed with ultimate thinness, broad spectra of outstanding electronic and optoelectronic properties, as well as their compelling dependency on discrete, integer numbers of layers, thus having strong potential for enabling devices with unconventional features and performance.[1−3] Group VI transition metal dichalcogenides (TMDCs) have tunable band gaps (from 0.88 to 2 eV) and are especially suitable for atomically thin transistors by virtue of their band gaps being comparable with those of conventional semiconductors (*e.g.*, Ge, Si, GaAs). Moreover, these semiconducting TMDCs show reliable transition from indirect to direct band gap when scaled down to the single-layer limit.[4,5] They also offer different crystal structures and phases so that they can be accessed and configured to achieve programmable functions. For example, the electrodes (*i.e.*, source and drain) and the channel of a field-effect transistor (FET) can be built in a single material with configurable metallic and semiconducting phases.[6−9] TMDCs may also possess dangling-bond-free surfaces and can be assembled together through van der Waals interactions to

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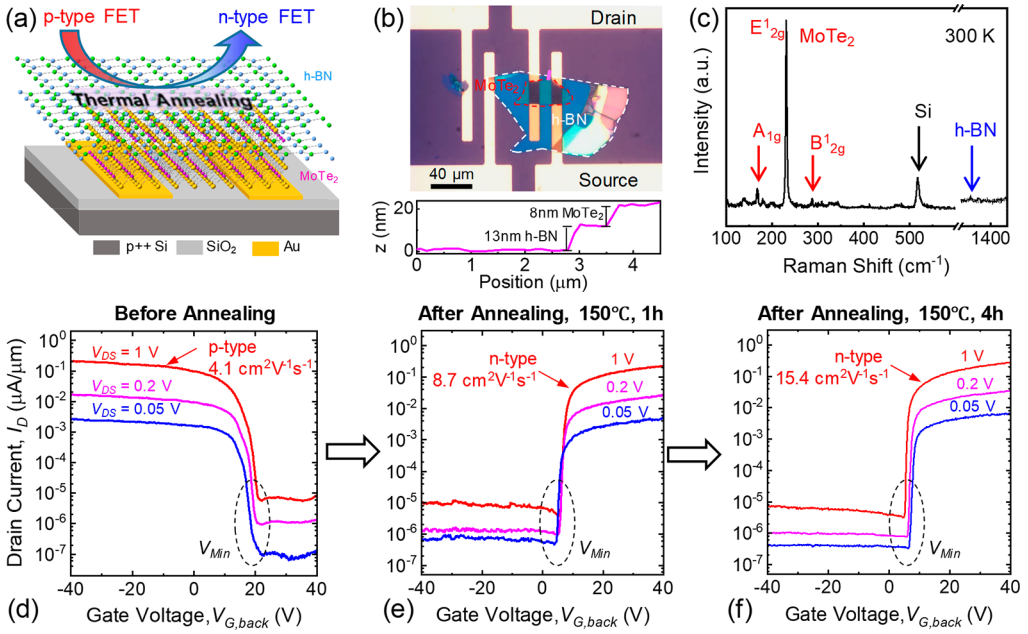

Figure 1. Device structure and electronic characteristics of back-gate h-BN/$MoTe_2$ FET measured before and after thermal annealing. (a) 3D atomic-view schematic of the device and its heterostructure. (b) Optical microscopy image of the representative device and thickness profile of stacking nanosheets. (c) Raman spectroscopy measurement and verification of signatory Raman peaks of the constituting crystals in the device stack. (d) Drain current, I_D, as a function of the back-gate voltage, $V_{G,back}$, of the as-fabricated FET at varying drain-to-source bias voltages, V_{DS}. (e) Transfer characteristics of the same device after thermal annealing in N_2 flow for 1 h. (f) Transfer characteristics of the device after the second thermal annealing in N_2 flow for 4 h.

create novel heterostructures with great versatility. To date, 2D TMDCs have been adopted in many electronic and optoelectronic devices, ranging from FETs, tunneling FETs, memories, to logic circuits and photodetectors.[10−12] Carrier transport in the channels and across the metal−semiconductor contacts is at the heart of electronics and optoelectronics. One basic and essential characteristic of a 2D FET is its dominant polarity of carrier transport, that is, electron (n-type) or hole (p-type) conduction in the channel. However, often due to strong Fermi level pinning at the metal−2D semiconductor interface, the Schottky barrier (SB) height does not change considerably irrespective of the choice of metal contact, which results in 2D molybdenum disulfide (MoS_2) FETs mainly exhibiting n-type conduction[13] and 2D tungsten diselenide (WSe_2) FETs being accessible to both electron and hole conduction.[14]

Recently, molybdenum ditelluride ($MoTe_2$), a newer member of the TMDC family, is receiving increasing attention due to its rich crystalline phases and its unusual semiconducting, metallic, and superconducting properties.[15−18] The hexagonally structured $MoTe_2$ has a band gap comparably narrower than those of other semiconducting TMDCs.[5,19] Single-layer (1L) $MoTe_2$ is theoretically predicted and experimentally verified to have a band gap of E_g = 1.1 eV, which very well matches the band gap of silicon (Si). The acoustic phonon-limited mobility of $MoTe_2$ is greater than 2500 $cm^2\ V^{-1}\ s^{-1}$ theoretically.[20] In contrast to MoS_2, $MoTe_2$ mainly shows p-type (or p-dominated ambipolar) when prepared by using a flux of tellurium (Te).[15] Nevertheless, traditional doping methods, including ion implantation and dopant diffusion, are not yet practically applicable to 2D materials.[21,22] The technological challenge of chemical doping is manipulating doping concentration in atomically thin semiconductors. Recently, unconventional doping strategies, such as molecular doping,[23,24] electron doping,[25,26] and optoelectronic activation,[27] have been explored. Such methods mainly involve surface dopant species, including H-doping from parasitic H_2O accompanying Al_2O_3 atomic layer deposition (ALD),[24] MgO film deposited by electron-beam evaporation,[26] or O_2/H_2O ad/desorption-induced doping mediated by electrothermal self-heating.[28] These approaches are invasive to the host 2D materials and often require special gases or complex fabrication processes. Meanwhile, another issue in most TMDCs is that surface stability and susceptibility can often be affected by the presence of ionic impurities when exposed to an ambient environment or at the interface with the substrate.[29−31] $MoTe_2$ thin FETs are also sensitive to oxygen and water vapor due to intrinsic Te defects, thereby altering the device performance.[32] Therefore, reliable and controllable creation of n-type transport of $MoTe_2$ FETs remains an open challenge and demands careful investigation toward realizing $MoTe_2$ monolithic logic functions and fulfilling the promises and potential of this excellent 2D material.

In this study, we introduce a dopant-free method for rationally controlling the polarity of $MoTe_2$ transistors from p- to n-type. To prevent environmental susceptibility and ensure stability of the transistor performance, we employ a thin hexagonal boron nitride (h-BN) layer on top of $MoTe_2$ to encapsulate the devices, thus evading direct exposure of the chemically active Te atoms on the device surface. The pristine h-BN-encapsulated $MoTe_2$ (h-BN/$MoTe_2$) FETs are p-type. Interestingly, after simple thermal annealing at ∼100 to 350 °C in inert gases, the polarity of the h-BN/$MoTe_2$ transistors is switched from p-type to n-type with excellent performance enhancement. The efficacy and simplicity of this approach to controlling transistor polarity manifests in several aspects. First, the method does not involve any chemical dopants, electrical field, or any complex process. Second, very moderate annealing

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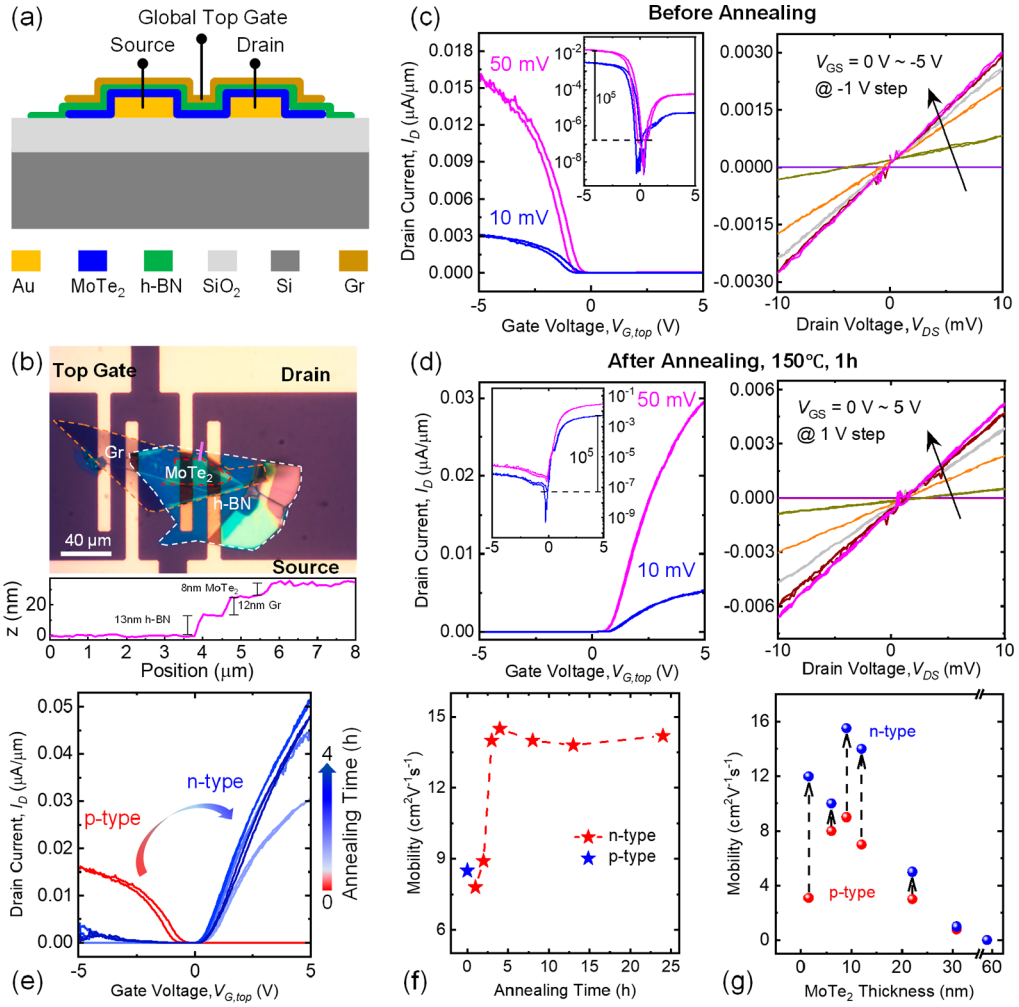

Figure 2. Transfer characteristics of the Gr top-gate h-BN/$MoTe_2$ FET measured before and after thermal annealing. (a) Cross-sectional illustration of the top-gate $MoTe_2$ FET. (b) Optical microscopy image of the device and thickness profile of stacking nanosheets. (c) Left: Drain current, I_D, as a function of the top-gate voltage, $V_{G,top}$, with drain-to-source excitation voltage V_{DS} of 50 and 10 mV in linear and logarithmic scale, respectively. Right: I_D as a function of V_{DS} for the device before thermal annealing as $V_{G,top}$ decreases from 0 to −5 V with a step of −1 V. (d) Left: I_D as a function of $V_{G,top}$ for the same device after 1 h thermal annealing at 150 °C in linear and logarithmic scale, respectively, which shows unipolar n-type. Right: I_D as a function of V_{DS} for the annealed device with $V_{G,top}$ increasing from 0 to 5 V with a step of 1 V. (e) Annealing time dependence of I_D−$V_{G,top}$ curves at the same V_{DS} = 50 mV. (f) Measured mobility with varying annealing time. (g) Summary of the switch from hole to electron conduction, measured from multiple top-gate h-BN/$MoTe_2$ FETs with varying $MoTe_2$ thickness, all through 4 h annealing.

temperature (~100 °C) can trigger p- to n-transport in $MoTe_2$ FETs with Au contact electrodes. Third, h-BN encapsulation renders excellent passivation and highly stable transistors. Importantly, this simple technique has enabled $MoTe_2$ transistors with very high electron mobility of μ_n = 52.4 cm^2 V^{-1} s^{-1} and on/off current ratio of I_{on}/I_{off} ~ 10^5. This controllable realization of n-type $MoTe_2$ transistors is conscientiously elucidated by $MoTe_2$−metal Schottky contact modulation due to thermal annealing, along with an extensive set of clear and deterministic control experiments. This method is further utilized to build all-$MoTe_2$ monolithic complementary logic functions, thus validating a viable and agile approach to controlling transport polarity and enhancing performance of 2D Schottky contact FET-enabled electronic and optoelectronic devices.

RESULTS AND DISCUSSION

p- to n-Type Polarity Change in Back-Gate $MoTe_2$ FETs by Thermal Annealing. We first describe the device structure and measure the transfer characteristics of a global back-gate $MoTe_2$ FET with top h-BN encapsulation. Figure 1a presents a three-dimensional (3D) illustration of the h-BN-encapsulated $MoTe_2$ (h-BN/$MoTe_2$) FET on 290 nm thick silicon oxide (SiO_2) with doped Si as the global back gate. Specifically, the $MoTe_2$ crystal is fully encapsulated by a thin h-BN layer. A top-view optical micrograph of the as-fabricated h-BN/$MoTe_2$ FET (Figure 1b) displays the distinctive colors of different stacking layers of the heterostructure. Gold (Au) is selected as the electrode material due to its moderate work function (ϕ_m = 4.7−4.9 eV)[33,34] compared to that of other metals (such as Pt, Ni, and Ti), so that the Fermi level is around the midgap of the $MoTe_2$ semiconductor.[35] The line profile measured by atomic force microscopy (AFM) shows that the thicknesses of h-BN and $MoTe_2$ layers are 13 and 8 nm, respectively. The device fabrication process is described in detail in the Experimental Section. Raman spectroscopy probing (λ = 532 nm) on the h-BN/$MoTe_2$ stack of the back-gate FET (Figure 1c) exhibits the overall information on

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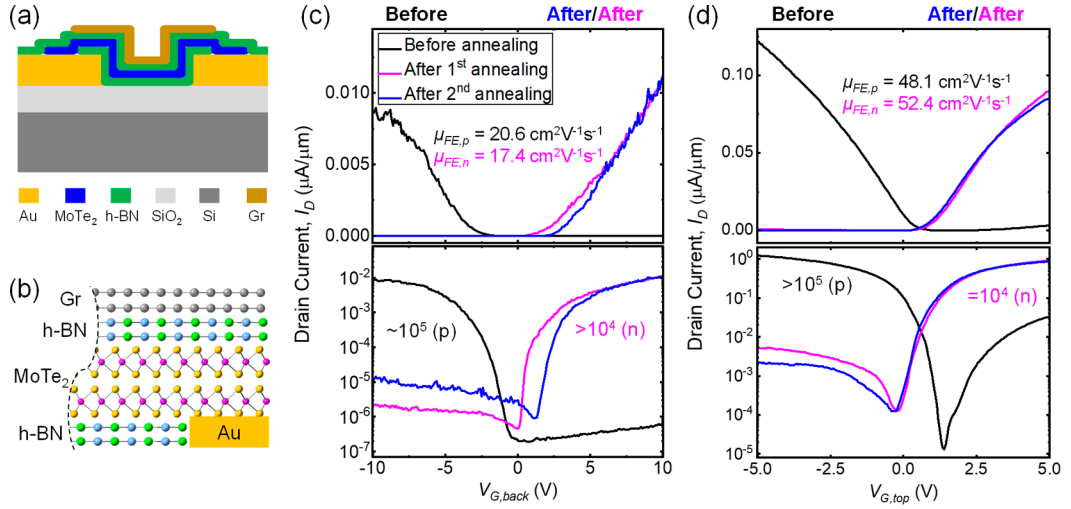

Figure 3. Transfer characteristics of double-encapsulated, dual-gate h-BN/$MoTe_2$/h-BN FET measured before and after thermal annealing. (a) Cross-sectional illustration of the h-BN/$MoTe_2$/h-BN FET. (b) 3D atomic-view schematic of the S−M contact region. (c) I_D−$V_{G,back}$ curves measured in the back-gate configuration, before thermal annealing, after the first and the second thermal annealing, in linear (top plot) and logarithmic (bottom plot) scales, all at V_{DS} = 50 mV. (d) I_D−$V_{G,top}$ curves measured in the top-gate configuration, before thermal annealing, after the first and second thermal annealing, all at V_{DS} = 50 mV.

the identities of the constitutive crystals in this heterostructure.[36]

Transfer characteristics of the back-gate FET is investigated under simple thermal annealing. Figure 1d shows the drain current (I_D) as a function of the back-gate voltage ($V_{G,back}$) and at various drain voltages (V_{DS}) before thermal annealing. As shown, the as-fabricated pristine back-gate h-BN/$MoTe_2$ FET exhibits hole conduction behavior (p-type transport), although the ambipolar $MoTe_2$ transistor has been previously reported due to Fermi level pinning at contacts.[37] The hole field-effect mobility is $\mu_{FE,p} = \frac{L}{W}\frac{d}{\varepsilon_0\varepsilon_r}\frac{1}{V_{DS}}\frac{dI_{DS}}{dV_G} \approx 4.1$ cm^2 V^{-1} s^{-1}, where L and W are the length and width of the channel, respectively, and d and ε_r are the thickness and dielectric constant of the corresponding dielectric layer, respectively. The dielectric constants of SiO_2 and h-BN are 3.2 and 3.5, respectively. The subthreshold swing (SS) is calculated to be $SS = \left(\frac{d\log_{10}I_{DS}}{dV_G}\right)^{-1} = 250$ mV/dec. As seen in Figure 1d, the gate voltage sweeping remains stable, and thus the environment has little effect on the measured data.

It is worth mentioning that the gate voltage (V_{Min}) at which the current becomes minimal is positive, indicating that the Fermi level of the as-exfoliated $MoTe_2$ is closer to the valence band. Specifically, in terms of crystal structure, the initial atom ratio of Te and Mo is 2.3, higher than the stoichiometric number of 2.0 (Supplementary Figure S1), verified by energy-dispersive X-ray spectroscopy (EDS). The excess Te is suggested to be atomic Te dopants that have been consistently observed in CVD-grown $MoTe_2$.[38,39] It was recently reported that the intrinsic defects of natural $MoTe_2$ are in the forms of interstitial/intercalated Te atoms and Mo vacancies observed through scanning transmission electron microscopy (STEM) and scanning tunneling microscopy (STM).[40] Therefore, presumably, the freshly exfoliated $MoTe_2$ flakes are p-type doped by excess Te. Interestingly, after thermal annealing at 150 °C in N_2 flow for 1 h, the polarity of the same device immediately turns into unipolar n-type (Figure 1e). In addition, the electron field-effect mobility increases to $\mu_{FE,n}$ = 8.7 cm^2 V^{-1} s^{-1}. Moreover, the hysteresis (quantified in voltage swing) decreases by ∼4 times after thermal annealing (Supplementary Figure S2). The intrinsic origin of hysteresis in $MoTe_2$ transistors could probably be attributed to charge trap states at the interface between $MoTe_2$ and the dielectric due to adsorption/desorption of water molecules or other contaminants. Thermal annealing essentially removes such contaminants and reduces the hysteresis. The positive value of V_{Min} in Figure 1e indicates that the $MoTe_2$ channel with n-type conduction is still p-type doped, which indicates that the transport behavior in the annealed $MoTe_2$ FET is not due to the electron doping effect. Subsequently, after a second thermal annealing for 4 h, the FET maintains n-type conduction and its performance is further boosted, with electron mobility boosted up to $\mu_{FE,n}$ = 15.4 cm^2 V^{-1} s^{-1} and an improved subthreshold swing of SS = 208 mV/dec (Figure 1f). It shall be emphasized that the positive values of V_{Min} in Figure 1e,f are approximately unchanged, which suggests that thermal annealing has a negligible effect on shifting the Fermi level of the p-type $MoTe_2$ channel material. It is worth mentioning that in Figure 1d,f, I_{off} increases with the increase of drain voltage (V_{DS}) due to the increase of thermionic emission contributed carrier transport at higher V_{DS}.

p- to n-Type Polarity Change in Top-Gate $MoTe_2$ FETs by Thermal Annealing. The transistor polarity change from p- to n-type has also been observed in top-gate h-BN/$MoTe_2$ FETs, as shown in Figure 2. A thin graphite (Gr) layer is additively transferred on top of an h-BN-encapsulated $MoTe_2$ FET to serve as the global top gate, as shown in Figure 2a,b. Figure 2c shows measured I_D as a function of $V_{G,top}$ for the top-gate FET before thermal annealing. The transistor behaves as a unipolar p-type with hole mobility of $\mu_{FE,p}$ = 7.8 cm^2 V^{-1} s^{-1} and an on/off current ratio of $I_{on}/I_{off} \sim 10^5$. I_D as a function of V_{DS} (I_D−V_{DS}) increases with increasing top-gate negative voltage $V_{G,top}$, indicating p-type conduction in the transistor. The linear I_D−V_{DS} characteristic indicates low SB at the source/drain (S/D) contacts, and holes can tunnel through. After thermal annealing under the same condition, 150 °C for 1 h (Figure 2d), the transistor polarity is also changed from p-

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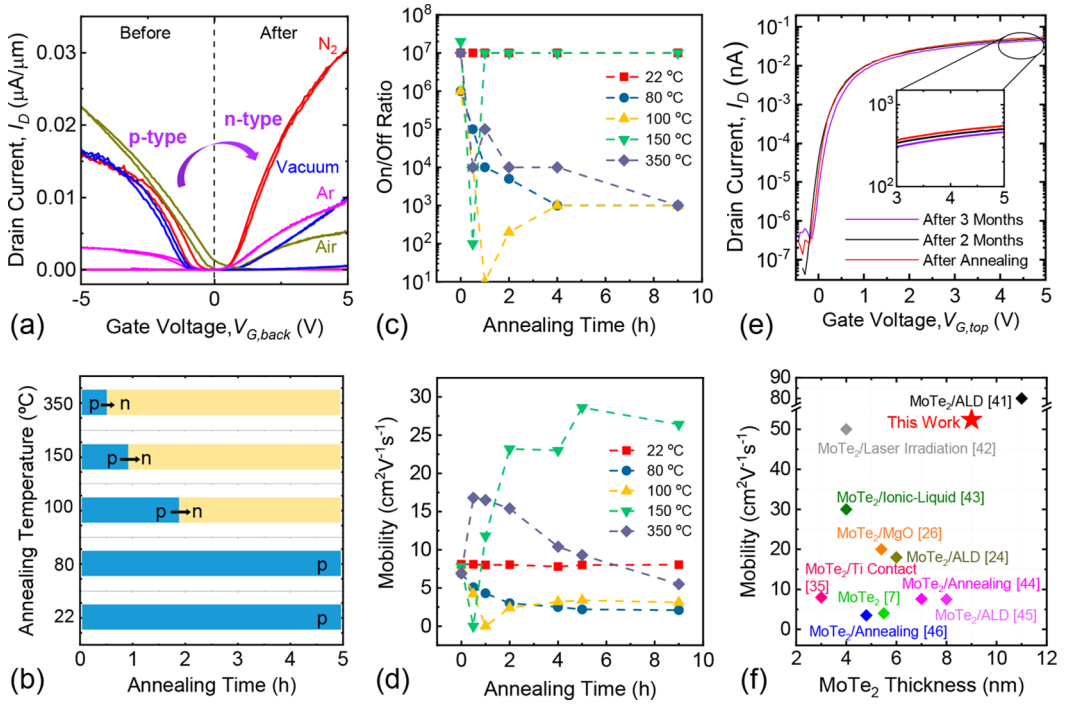

Figure 4. Summary on polarity change, annealing conditions, and performance of h-BN-encapsulated $MoTe_2$ FETs. (a) Transfer characteristics of top-gate h-BN/$MoTe_2$ FETs before and after thermal annealing in different carrying gases or vacuum. (b) Transistor polarity switch occurs at >100 °C and needs shorter time at higher annealing temperature. (c) Evolution of mobility with varying annealing temperature. (d) On/off ratio varies with annealing temperature and time. (e) Transfer characteristics of the same device after thermal annealing and after several months. (f) Comparison with other best n-type $MoTe_2$ FETs reported in the literature.

to n-type, and the hysteresis voltage swing decreases dramatically. The I_D-V_{DS} characteristic is also linear, and the drain current increases with increasing positive $V_{G,top}$. Figure 2e summarizes that the transistor polarity has been changed from p- to n-type and subsequently maintains n-type during continued thermal annealing. The mobility of the top-gate device increases with continued thermal annealing and reaches a high value after 4 h, stabilizes, and persists for >24 h of annealing (Figure 2f). In addition, the transistors show reliable current levels and high stability of threshold voltage (V_T) during thermal annealing, confirming the h-BN-encapsulated $MoTe_2$ structures are robust and electrically stable.

We have measured tens of top-gate h-BN/$MoTe_2$ transistors with various $MoTe_2$ thicknesses, and all of them (as summarized in Figure 2g) exhibit polarity change from p-type (of the as-fabricated pristine devices) to n-type after 4 h thermal annealing at 150 °C in a N_2 flow. In addition, the gate leakage currents in all of the measured transistors are negligible at several picoamperes (pA) (Supplementary Figure S2). The freshly exfoliated $MoTe_2$ flakes used in this study cover a wide range of thicknesses, from 1.5 nm (bilayer, 2L) to 57.6 nm (82L). A thicker channel enhances the carrier mobility through reduced Coulomb scattering due to physical separation from the SiO_2 dielectric. Meanwhile, the transistor performance declines when the $MoTe_2$ thickness is greater than 10 nm. Given the highly consistent observations in both back-gate and top-gate devices described above, the data have shown that the type of dominant injected carriers in the h-BN-encapsulated $MoTe_2$ FETs have been switched from p- to n-type through the 150 °C thermal annealing.

p- to n-Type Polarity Change in Dual-Gate $MoTe_2$ FETs by Thermal Annealing. Considering SiO_2 used in the above devices might interact with $MoTe_2$ at the interface, we conduct a careful control experiment using h-BN as the bottom dielectric of the transistor. h-BN makes outstanding ultrathin dielectric layers for 2D electronics due to atomically smooth surface and high immunity to surface states. Figure 3a illustrates the h-BN double-encapsulated device with both top gate (Gr) and back gate (Si), with thicknesses of the top h-BN, $MoTe_2$, and bottom h-BN being 25, 9, and 30 nm, respectively. Figure 3c shows that the polarity of the back-gate branch is p-type with a hole mobility of $\mu_{FE,p}$ = 20.6 $cm^2\ V^{-1}\ s^{-1}$. After thermal annealing under the same condition, the transistor polarity is changed from p- to n-type. Similarly, the top-gate h-BN/$MoTe_2$/h-BN transistor shows the same phenomenon (Figure 3d). Before thermal annealing, the hole mobility is $\mu_{FE,p}$ = 48.1 $cm^2\ V^{-1}\ s^{-1}$, which is the highest value ever attained by back-gate $MoTe_2$ transistors at room temperature. After thermal annealing, the transistor exhibits electron conduction (n-type) with an even higher mobility of $\mu_{FE,n}$ = 52.4 $cm^2\ V^{-1}\ s^{-1}$.

Control Experiments, Persistence of Polarity Change, and Its Temperature Dependency. We systematically investigate the p- to n-type polarity change phenomena and further conduct more control experiments to meticulously explore effects possibly contributing to the transistor polarity change. One first set of control experiments is on direct comparison between devices with and without h-BN encapsulation, cofabricated on the same $MoTe_2$ flake (Supplementary Figure S3). Upon the same thermal annealing (at 150 °C in N_2 flow for 1 h or longer), the h-BN-encapsulated FET shows a p- to n-type polarity switch, whereas the uncovered one does not transform to n-type but exhibits considerable degradation of its p-type behavior. As detailed in Supporting Information, spectroscopic studies (EDS, Raman) indicate that the annealing has no noticeable

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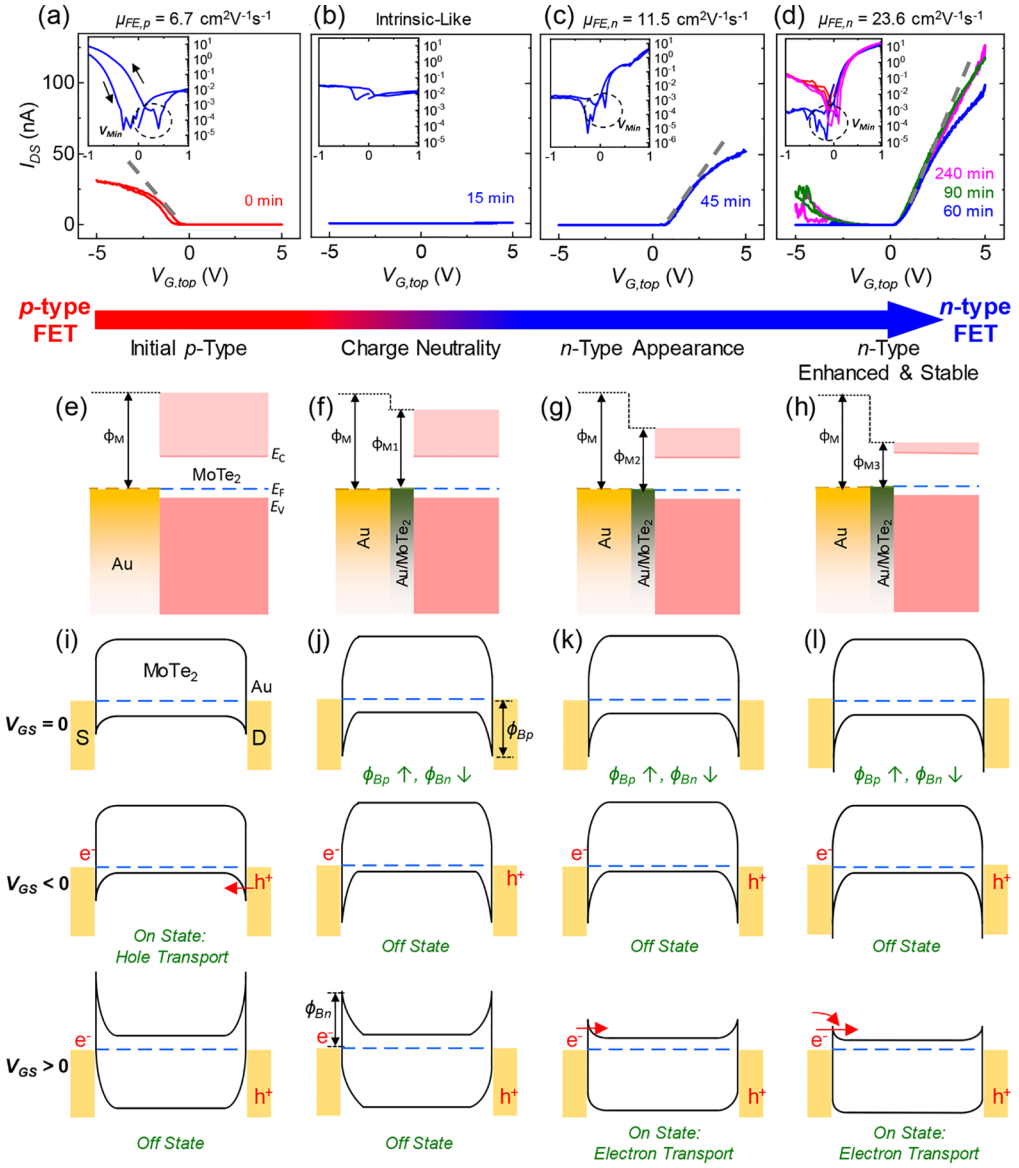

Figure 5. Visualizing the polarity change process and elucidating its underlying mechanism. (a–d) Polarity change process of top-gate h-BN/$MoTe_2$ FET during 150 °C thermal annealing, measured in ambient environment. V_{DS} = 50 mV. The plots in (b–d) share the same *y*-axis label with the plot in (a). (e–h) Corresponding band diagrams of the vertical $MoTe_2$–Au contact from the initial state and during the annealing process. (i–l) Corresponding electrostatically gated band diagrams of the transistor with horizontal source–gate–drain structure in the four stages and for V_{GS} = 0, V_{GS} < 0, and V_{GS} > 0 (assuming V_{DS} = 0 for simplicity in depicting the diagrams).

effect on the h-BN-encapsulated $MoTe_2$ crystal in the channel region, whereas it probably has caused oxidation and degradation in the uncovered $MoTe_2$ (Supplementary Figure S4). It is also indicated that the h-BN encapsulation is sufficiently impermeable to prevent Te loss from the covered $MoTe_2$ channels through 150 °C annealing (Supplementary Figure S1b). Upon varying the top h-BN thickness, we have also found the annealing-induced polarity change is independent of the encapsulating h-BN thickness (Supplementary Figure S5).

Persistency of p- to n-type polarity change has been consistently observed in all h-BN top- and double-encapsulated FETs (as detailed in previous sections), upon annealing at 150 °C, regardless of the carrying gases. The h-BN/$MoTe_2$ transistors are thermally annealed in vacuum or in the carrying gas of N_2, Ar, or air. Figure 4a shows that all pristine p-type conduction switches to n-type conduction after annealing, independent of carrying gas. It is noted that as the thickness and area of the devices are different, the on-state currents of the devices vary.

Meanwhile, annealing temperature can determine if the transistor polarity change occurs, and there appears to be a threshold temperature. The temperature dependence of the transfer characteristics is investigated in the temperature range from 22 °C (room temperature) to 350 °C. The polarity switch from p- to n-type exclusively occurs at annealing temperatures greater than 100 °C (Figure 4b). Figure 4c,d exhibits the time evolutions (during annealing) of mobility and on/off ratio varying with annealing temperature, respectively.

Polarity-Switched Transistor Performance and Benchmarking. A long-term stable carrier transport in ultrathin channels is important for realizing practical high-performance devices. We compare the measured transfer characteristics of the same device after thermal annealing and

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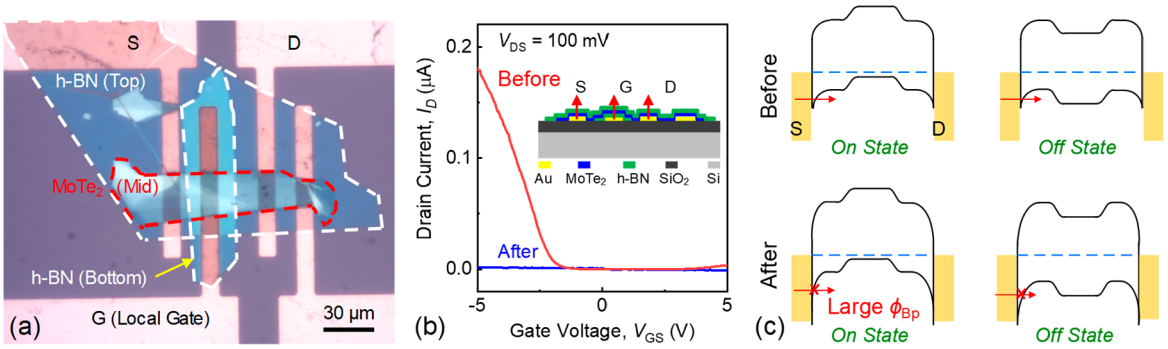

Figure 6. Further verification with deterministic control experiment on local gate FET to elucidate the mechanism of modifying the $MoTe_2$–Au Schottky contact on changing device transport polarity. (a) Optical microscopy image of the local gate $MoTe_2$ transistor encapsulated by h-BN. (b) I_D–V_{GS} characteristics of local gate $MoTe_2$ transistor before and after thermal annealing at 150 °C for 1 h. The inset shows the cross-sectional illustration of the device. (c) Corresponding electrostatically gated band diagrams of the local gate transistor with horizontal S–G–D structure at on state and off state before and after thermal annealing.

after preserving it in ambient environment for a long time. As shown in Figure 4e, the I_D–$V_{G,top}$ curves exhibit excellent repeatability and stability after 2 and 3 months. Continuous measurement over 36 h also showed very stable performance (Supplementary Figure S6). Figure 4f summarizes and benchmarks the specifications and performance of devices measured in this work against the other best n-type $MoTe_2$ FETs reported in the field,[41−46] illustrating that post-annealing polarity-switched devices are outstanding and among the very best in terms of measured mobility. Specifically, the highest mobility ($\mu_{FE,n}$ = 52.4 cm^2 V^{-1} s^{-1}) is attained in a h-BN/$MoTe_2$/h-BN device with a 9 nm thick $MoTe_2$ channel, and this is, to date, the highest mobility measured among thermally annealed $MoTe_2$ FETs.

Elucidating the Mechanism: $MoTe_2$–Au Schottky Contact Change *via* Thermal Annealing. With the $MoTe_2$ channel region well encapsulated by h-BN and showing no measurable material variation, it is clear by now that the observed polarity switch from p- to n-type has been very consistent and robust, regardless of back gate or top gate, SiO_2, or h-BN/SiO_2 substrate. We also find that the V_{Min} values remain stable, indicating the Fermi level of the annealed $MoTe_2$ channel is still closer to the valence band than to the conduction band (thus still p-type channel material). Therefore, this consistent polarity switch in all types of encapsulated devices examined above collectively suggests that, instead of the insulators and substrates, it is the $MoTe_2$–metal contact regions at S/D electrodes and their interplay with thermal annealing that are responsible for switching the polarity of device transport (p to n), as we systematically illustrate in Figure 5.

To visualize the p- to n-type polarity change process, we continuously measure the I_D–$V_{G,top}$ characteristics at different annealing stages. Figure 5a shows the p-type characteristics of the as-fabricated pristine transistor. After 15 min thermal annealing, the p-type I_D decreases by several orders of magnitude (Figure 5b). As thermal annealing continues, the transistor starts to exhibit n-type behavior. The data in Figure 5c (after 45 min thermal annealing) appear to be almost a "mirrored" n-type copy of that in Figure 5a (before annealing). With longer annealing, the n-type performance enhances moderately until the carrier concentration level reaches saturation.

All of the data and control experiments above suggest that the thermal annealing effects on the $MoTe_2$–Au Schottky contacts account for the observed polarity change. In fact, our earlier studies on Schottky contact MoS_2 FETs have also suggested that thermal annealing can modify TMDC–metal contacts by alloying or hybridization, thus changing the effective work function and Schottky barrier at the contacts.[47] Here, we perform X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy of $MoTe_2$ on Au before and after thermal annealing, as well as of $MoTe_2$ on SiO_2 as a reference. The $MoTe_2$ samples are fully encapsulated by thin h-BN flakes in both cases. Upon annealing, the XPS results (Supplementary Figure S7) exhibit distinct shifts of the Te $3d_{5/2}$ peak for few-layer $MoTe_2$ on Au, whereas, in contrast, no shift of the Te $3d_{5/2}$ peak is seen for $MoTe_2$ on SiO_2. Raman spectroscopy results also show a clear shift of the $MoTe_2$ peak when 1L $MoTe_2$ is annealed on top of Au (Supplementary Figure S8).

As illustrated in Figure 5, upon thermal annealing, owing to the $MoTe_2$–Au interaction, the Au–$MoTe_2$ composite exhibits lower work function compared to that of bare Au (Figure 5e–h). From the carrier transport perspective, electronic characteristics of the $MoTe_2$ transistor during thermal annealing are explained using band diagrams in Figure 5i–l. We consider $MoTe_2$ as an intrinsically p-type material due to built-in Te excess, which dictates that the Fermi level (E_F) should be closer to the valence band. Before annealing, the Schottky barrier height for holes (ϕ_{Bp}) is lower than that for electrons (ϕ_{Bn}). As a result, the Au–$MoTe_2$ contact has a lower contact resistance for hole transport, resulting in p-type transport behavior (Figure 5a,i). Figure 5j–l shows the band diagrams at V_{GS} = 0, V_{GS} < 0, and V_{GS} > 0, corresponding to the annealed conditions shown in Figure 5b–d. These indicate that work function reduction of the Au–$MoTe_2$ composite corresponds to a ϕ_{Bp} increase with the annealing time. On the other hand, the Schottky barrier height for electrons, $\phi_{Bn} = E_g - \phi_{Bp}$, decreases. When $\phi_{Bn} \approx \phi_{Bp}$, the device shows intrinsic-like I–V characteristics (Figure 5b,j). When ϕ_{Bn} further decreases and becomes smaller, the contact resistance for electrons is much lower than that for holes. Therefore, the observed p- to n-type polarity change during thermal annealing is attributed to the work function reduction due to the Au–$MoTe_2$ composite, which lowers the contact resistance for electrons but increases the contact resistance for holes. Meanwhile, V_{Min} values in Figure 5a,c,d do not shift noticeably after thermal annealing, which clearly indicates that intrinsic doping in the $MoTe_2$ channel material is not changed. Given this, we note that, for future technology considerations, when threshold voltage (V_T)

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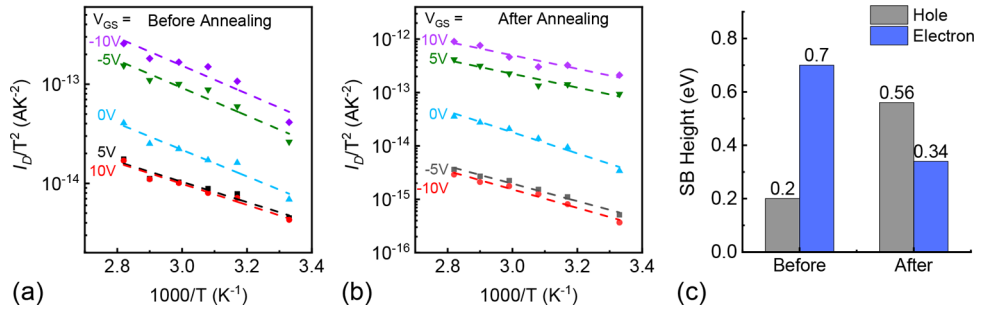

Figure 7. Extraction of Schottky barrier (SB) height for the h-BN/$MoTe_2$ FETs before and after thermal annealing. I_D/T^2 is plotted against $1000/T$ at different values of V_{GS} in the device with Au contacts (a) before and (b) after thermal annealing. The dashed lines are fitting curves. (c) Comparison of the SB heights for electrons and holes before and after thermal annealing. SB height of electrons (holes) is extracted at the off state (thermionic emission limited transport) with V_{GS} of 10 V (−10 V) from the slope of I_D/T^2 (in logarithm) *versus* $1/T$ plot.

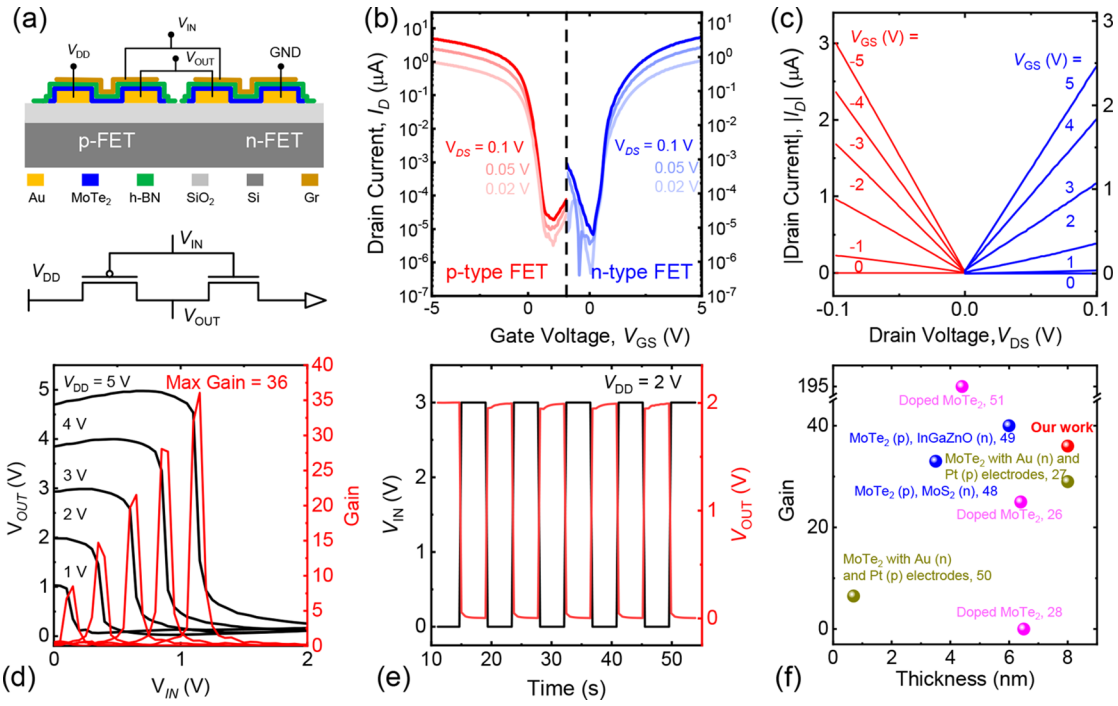

Figure 8. Monolithic $MoTe_2$ inverter utilizing the thermally controlled polarity change of the constitutive FETs. (a) Cross-sectional view of the $MoTe_2$ inverter and its circuit diagram. (b) Transfer characteristics (I_D−V_{GS}) of the p-FET (curves on left) and n-FET (curves on right). (c) Output characteristics (I_D−V_{DS}) of the p-FET (left) and n-FET (right). (d) Voltage transfer characteristics of the $MoTe_2$ inverter at varying supply voltage V_{DD} = 1, 2, 3, 4, and 5 V, showing almost ideal transition voltages. The right axis values indicate the voltage gain (g = $-dV_{OUT}/dV_{IN}$), which is as high as g = 36 at V_{DD} = 5 V. (e) Dynamic switching of the $MoTe_2$ inverter. (f) Benchmarking of this monolithic $MoTe_2$ inverter against reported heterogeneous inverters involving $MoTe_2$.

tuning is desired, the present polarity control method should be combined with techniques or processes that can efficiently modify V_T.

Further Experimental Verification: Local Gate Device, Schottky Barrier Height Extraction. The modification of $MoTe_2$−Au contacts by thermal annealing and its deterministic role on transport polarity change are further verified by control experiments on local gate devices that we have delicately made with meticulously prepared $MoTe_2$ and h-BN flakes, as shown in Figure 6a. The local gate (G) resides in the middle of the channel, and there is no overlap region, but there is distance (extension region) between the G and S/D electrodes. Its length is ∼1/4 of the channel length, as displayed in Figure 6a. The first and third electrodes from the left are used as S and D, and the second electrode is used as bottom local gate G, on top of which is an h-BN layer as gate dielectric, and $MoTe_2$ is transferred on top of h-BN as channel material and then fully encapsulated by a top h-BN layer. The FET shows high-performance p-type characteristics before thermal annealing (Figure 6b). After thermal annealing, the device shows much degraded p-type behavior but not n-type characteristics. The lack of p- to n-type change here clearly indicates that it is not some mysterious doping mechanism in the channel region that is accounting for the p- to n-type polarity change. Instead, this control experiment again strongly confirms that the $MoTe_2$−Au contacts play a key role in the polarity change. In fact, the mechanism illustrated in Figure 5 and Figure 6c very well explains the results from the local gate device, where after annealing Schottky barriers become high for holes, which blocks injection of holes into the channel from

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S/D, hence the observed degradation in p-type behavior. Note here the extension regions in the local gate device remain p-type.

Furthermore, Figure 7 presents the I_D-V_{DS} characteristics of few-layer $MoTe_2$ FETs at different temperatures in range of ~293−355 K (~20−82 °C), which are lower than the annealing temperature for polarity change. SB heights for electrons/holes are extracted at the off state (thermionic emission limited transport) for p-FET (before annealing, Figure 7a) and n-FET (after annealing, Figure 7b) from the slope of I_D/T^2 (in logarithm) *versus* $1/T$ plot. Upon thermal annealing, the SB height for holes increases from 0.2 to 0.56 eV, and the SB height for electrons decreases from 0.7 to 0.34 eV (Figure 7c). These results clearly provide direct and deterministic evidence of modifying relative SB heights for electrons/holes by thermal annealing.

It is worth noting that the transistor polarity change from p- to n-type is explained by simply modifying the Schottky barrier (SB) height through thermal annealing; it is fundamentally different from previously reported chemical doping. The mechanism of transistor polarity change also preserves the excellent electron and hole mobilities of h-BN/$MoTe_2$/h-BN heterostructures. The benefit from the h-BN encapsulation is to maintain $MoTe_2$ crystal intact. With comparison to $MoTe_2$ FETs on SiO_2 substrates, the annealed h-BN-encapsulated $MoTe_2$ devices are free of hysteresis effects. It not only leads to an enhanced electron mobility but also features superior stability and robustness.

Monolithic Inverter Demonstration by Utilizing the Polarity Control *via* Annealing. Finally, we design and demonstrate high-performance monolithic complementary inverters by directly exploiting the polarity control elucidated above to enable both p-FET and n-FET in $MoTe_2$ (unlike other inverters that employ two different 2D materials for p- and n-FET). Figure 8a shows the cross section of the Gr top-gate $MoTe_2$ inverter with h-BN encapsulation. The n-FET is realized by polarity change from an as-fabricated p-FET through thermal annealing; then another p-FET is added nearby on the same chip *via* the agile, deterministic all-dry stamp-transfer process for making 2D devices. Figure 8b depicts measured transfer characteristics of both FETs, featuring a high on/off current ratio of ~10^6. Figure 8c illustrates the linear I_D-V_{DS} curves with varying gate voltage of 0 to −5 V for p-FET and 0 to 5 V for n-FET.

An inverter is a "NOT" logic gate that outputs the opposite logic level of its input. Clean inverter operation is observed in Figure 8d for switching between logic "1" (~V_{DD}) and logic "0" (0 V). When V_{IN} is V_{DD} (logic "1"), the n-FET is turned on, and V_{OUT} decreases to near 0 (logic state "0"). When V_{IN} is pulled down to zero (logic "0"), V_{OUT} assumes V_{DD} (logic "1"), indicative of the complete input/output signal inversion. The slope of transfer function in the middle transition region provides a measure of the small signal voltage gain ($g = -dV_{OUT}/dV_{IN}$), which presents the responsivity of V_{OUT} variation to the change in V_{IN}. A high gain of g = 36 is achieved under supply voltage V_{DD} = 5 V (Figure 8d), validating this inverter can serve for 2D logic circuits. Another important figure-of-merit for an inverter is on its dynamic operations and cycling performance. This inverter is switched by a square voltage waveform (V_{IN}) applied to the gate, which causes the output voltage (V_{OUT}) to oscillate synchronously with a phase difference of π, as shown in Figure 8e. Figure 8f illustrates the comparison and benchmarking of all known inverters using $MoTe_2$, where previously reported inverters have been realized by using different materials for p- and n-FETs, including $MoTe_2/MoS_2$[48] or $MoTe_2$/InGaZnO heterostructures,[49] employing electrodes with different work functions,[24,50] or aluminum modification.[51] This demonstration of *monolithic* high-performance inverters solely using $MoTe_2$ as the channel material with p- and n-type controlled by simple thermal annealing modification of Schottky contacts provides possibilities toward rationally controlling polarity of arrays of devices to enable more complex logic functions and circuits, all in $MoTe_2$ with metal electrodes.

CONCLUSIONS

In summary, we have developed a dopant-free transistor polarity control method by modifying Schottky barrier height *via* thermal annealing. We realize $MoTe_2$ FETs from p- to n-type conduction with measured electron mobility up to 52.4 $cm^2\ V^{-1}\ s^{-1}$ and on/off current ratio of $I_{on}/I_{off} \sim 10^5$ or higher. The h-BN-encapsulated $MoTe_2$ FETs exhibit excellent stability and robustness, with versatile device configurations, manifesting the potential extension to other 2D semiconductors and contacting materials. The modification of Schottky barrier height for holes and electrons is derived from thermally induced work function variation. More generally, the contact engineering approach provides an alternative pathway to intentionally configure the transport polarity of Schottky contact FETs. Such nondestructive and dopant-free contact engineering techniques have enabled us to build high-performance all-$MoTe_2$ monolithic complementary logic circuits.

EXPERIMENTAL SECTION

Device Fabrication. All $MoTe_2$ FETs are fabricated by exfoliating $MoTe_2$ flakes from 2H-$MoTe_2$ bulk crystal and then stamp-transferred onto a SiO_2-on-Si substrate with prepattered source/drain (S/D) electrodes by employing an all-dry transfer method.[52] First, the electrodes are patterned and fabricated onto a Si wafer covered by 290 nm thick thermal oxide (SiO_2) using photolithography and Au deposition. The substrates with S/D electrodes are cleaned in acetone and isopropyl alcohol using a sonicator and dried using a N_2 gun. In the next step, a $MoTe_2$ flake with uniform thickness is transferred onto the SiO_2-on-Si substrate or on earlier transferred h-BN layer. During transfer, it is necessary to keep a ~2−4° anchor between the flake and the substrate in order not to trap bubbles in the interface between $MoTe_2$ and the substrate. For the h-BN-encapsulated transistors, the second transfer step is conducted by exfoliating h-BN flakes from h-BN bulk crystal. The shape of the h-BN flake is carefully chosen in order to fully encapsulate the $MoTe_2$ flake. The thin graphite flakes are exfoliated from graphite bulk crystal. After all of the transfer processes, the devices are annealed at the temperature of 80−350 °C in N_2 gas (78 Torr) with a constant flow rate of 102.4 sccm. All 2D materials ($MoTe_2$, h-BN, and graphene) are prepared by Scotch-tape exfoliation from high-quality single-crystal flakes onto PDMS stamps.

Material Characterization. Atomic force microscopy imaging is performed using an Agilent N9610A AFM in the tapping mode. Raman spectroscopy is performed using a customized micro-Raman system. Raman spectra of $MoTe_2$ flakes are measured in vacuum (~10 mTorr) at room temperature using a 532 nm green laser. The laser power is ~100−200 μW. EDS is measured using an XEDS and EBSD Oxford system (XMax 50 mm EDS, Nordlys high-resolution EBSD) that is integrated into the SEM system (Nova NanoLab 200).

Electrical Measurement. All measurements of the electronic characteristics are performed in the dark at room temperature using a semiconductor characterization system (Keithley 4200) and a customized probe station.

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ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.9b05502.

Figures of structure characterization (EDS, Raman, and XPS), performance of FETs (calibration of hysteresis, gate leakage, and cyclic testing), and control experiments (h-BN encapsulation and different contact metal) (PDF)

AUTHOR INFORMATION

Corresponding Author

Philip X.-L. Feng − *Department of Electrical Engineering & Computer Science, Case School of Engineering, Case Western Reserve University, Cleveland, Ohio 44106, United States; Electrical & Computer Engineering, University of Florida, Gainesville, Florida 32611, United States;* orcid.org/0000-0002-1083-2391; Email: philip.feng@ufl.edu

Authors

Xia Liu − *Department of Electrical Engineering & Computer Science, Case School of Engineering, Case Western Reserve University, Cleveland, Ohio 44106, United States;* orcid.org/0000-0003-1886-6825

Arnob Islam − *Department of Electrical Engineering & Computer Science, Case School of Engineering, Case Western Reserve University, Cleveland, Ohio 44106, United States;* orcid.org/0000-0002-3931-1506

Jing Guo − *Electrical & Computer Engineering, University of Florida, Gainesville, Florida 32611, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsnano.9b05502

Notes

The authors declare no competing financial interest.

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