Right-Angle Black Phosphorus Tunneling Field Effect Transistor

Matthew C. Robbins, Prafful Golani, and Steven J. Koester, *Fellow, IEEE*

***Abstract*—We report experimental demonstration of a right-angle black phosphorus (BP) tunneling field effect transistor (TFET). This device utilizes the effective mass anisotropy between the armchair (AC) and zigzag (ZZ) crystal orientations in BP as a means of inducing asymmetry between source and drain tunneling. As a result of this asymmetry, the BP TFET displays a higher I_{ON}/I_{OFF} ratio by 2 orders of magnitude and steeper *SS* than BP TFETs oriented along either the AC or ZZ direction only.**

***Index Terms*—black phosphorus, tunneling, effective mass, nanotechnology**

I. INTRODUCTION

RISING power consumption in advanced CMOS processors is a current limitation for the future of technology scaling. One primary cause for the end of traditional scaling is the inability to reduce the supply voltage due to the transistor subthreshold slope (*SS*) limit of ~60 mV/decade at room temperature. Because of this limitation, there have been extensive efforts to explore tunneling-field-effect-transistors (TFETs) due to their potential for achieving *SS* < 60 mV/dec [1]. The turn-off mechanism in TFETs involves gate modulation of band-to-band tunneling which is inherently a non-thermionic mechanism. Despite this promise, it has proven difficult to realize TFETs with steep slope and high on-state performance [2]. In III-V materials, staggered or broken-gap heterostructures [3],[4] are the main method for overcoming this issue, where a small effective band gap is created in the source to maximize I_{ON} while the drain utilizes a wider band gap to suppress ambipolar current. TFETs that utilize two-dimensional (2D) semiconductors [5],[6] have potential advantages due to enhanced scalability and electrostatic control, but using heterostructures to achieve the necessary injection asymmetry can be difficult to achieve in practice.

Black phosphorus (BP) has garnered significant attention for use in TFETs [7]-[10] due to its direct band gap, which is tunable between 0.3 eV and 2.0 eV depending upon thickness [11], as well as its light effective mass, which can be as low as $0.16m_0$ ($0.14m_0$) for electrons (holes) in the armchair (AC) direction [12]. Moreover, BP has a highly anisotropic effective mass with values of $1.18m_0$ ($0.89m_0$) for electrons (holes) in the zigzag (ZZ) direction [12]. This latter property can be exploited to create asymmetry between the source and drain tunneling currents, and also improve scalability. In fact, Ilatikhameneh, *et al*. [13] has proposed a device structure intended to exploit this

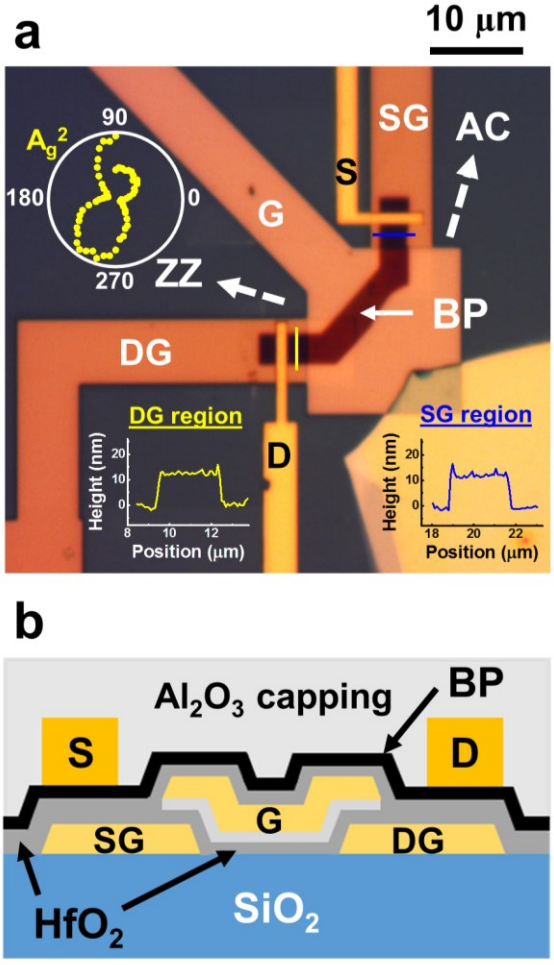

FIG. 1. (a) Top-view optical micrograph of right-angle (RA) black phosphorus (BP) TFET. The insets show the AFM line scans of the BP near the source and drain tunneling regions, as well as the polarized Raman characteristics. (b) Cross-sectional schematic diagram of BP TFET showing electrostatic gating configuration.

Manuscript received August, 23, 2019. This work was supported by the National Science Foundation (NSF) under Award No. ECCS-1708769. This work also utilized the University of Minnesota Characterization Facility which receives capital equipment support from the NSF through the University of Minnesota MRSEC under Award No. DMR-1420013. Portions of this work were conducted in the Minnesota Nano Center, which is supported by the NSF through the National Nanotechnology Coordinated Infrastructure under Award No. ECCS-1542202.

S. J. Koester and P. Golani are with the Department of Electrical and Computer Engineering, University of Minnesota, 200 Union St. SE, Minneapolis, MN 55455 (e-mail: skoester@umn.edu). M. C. Robbins was with the Department of Electrical and Computer Engineering, University of Minnesota, and is now with Honeywell Aerospace, Plymouth, MN 55441.

property, and simulations show that BP TFETs can be scaled to channel lengths of 2 nm while maintaining a I_{ON}/I_{OFF} above 10^4. This type of device is especially interesting because it can achieve this desirable injection asymmetry without using complex heterostructures. However, to date, this concept has not been used experimentally to improve BP TFET performance. In this work, we experimentally demonstrate a right-angle (RA) BP TFET with source (drain) regions oriented in the AC (ZZ) crystal directions. We show that this results in a TFET with higher I_{ON}/I_{OFF} ratio by 2 orders of magnitude and steeper *SS* than devices oriented along either the AC or ZZ direction only.

II. DEVICE FABRICATION

To fabricate the RA BP-TFET we use a triple-gated device structure similar to that previously reported in [8] and [14] which enables reconfigurable, independent electrostatic doping of the source, drain, and channel regions of the BP. In our original triple-gated device structure, two sets of perpendicular triple gates were utilized, where a single BP flake was aligned such that the AC and ZZ directions were oriented perpendicular to each set of gates. In our new device structure, shown in FIG. 1(a), the source and drain gates are placed orthogonal to each other and the channel gate is patterned as a large square that overlaps the source and drain gates.

The fabrication process largely follows that in [8] and is described briefly below. Starting with a Si/SiO_2 wafer, the source-gate and drain-gate electrodes were patterned first and consisted of 5 nm Ti /20 nm Pd. Next, atomic layer deposition (ALD) was used to deposit 10-nm of HfO_2 as a gate dielectric and 5-nm of $A1_2O_3$ as a gate spacer, followed by patterning of the channel-gate (consisting of 5 nm Ti /20 nm Pd) such that it overlaps the source-gate and drain-gate. After etching the $A1_2O_3$ gate spacer in the regions not under the gate electrode, ALD was again used to deposit 7 nm of HfO_2 as the gate oxide. A single BP flake was then exfoliated from a bulk crystal and aligned and transferred onto the gate structure and etched into the RA geometry. Atomic force microscopy (AFM) (performed after all device characterization had been competed) confirmed that the BP flake had nearly identical thicknesses of 12.7 $\pm$ 0.4 nm and 12.9 $\pm$ 0.4 nm in the drain and source tunneling regions, respectively. This result confirms that thickness variations do not play a role in the asymmetric characteristics.

Angle-resolved polarized Raman spectroscopy was used to identify the crystal orientation of the BP. Linearly polarized light with wavelength of 532 nm and spot size of ~0.5 µm was focused onto the BP channel. The inset to FIG. 1(a) shows a polar plot of the A_g^2 peak intensity (normalized to the A_g^1 peak intensity) as a function of incident beam polarization angle. The polar plot shows two fold symmetry [15], where the maximum and minimum intensity correspond to armchair (AC) and zigzag (ZZ) directions, respectively. While transmission electron microscopy (TEM) was not performed on these devices, we have previously confirmed that the orientation determined from optical techniques is consistent with TEM analysis [16].

The Raman characterization showed that the AC and ZZ orientations were misaligned by 18° from the BP-TFET transport directions. While this is larger than the 9° misalignment in [8], it is still suitable for making an initial assessment of the effectiveness of crystal anisotropy in enhancing TFET performance. Finally, Ti/Au metallization was patterned and lifted off next to make contact to the BP, followed by a 20-nm-thick passivation layer of ALD-deposited $A1_2O_3$. A cross-sectional diagram of the device is shown in FIG. 1(b).

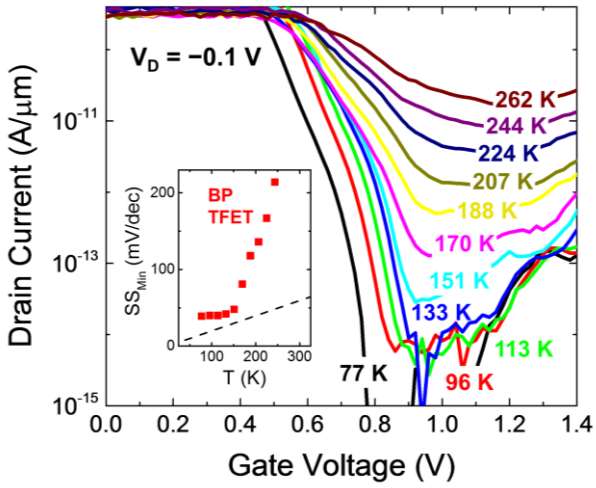

FIG. 2. Temperature-dependent transfer characteristics of an AC-only oriented TFET. Inset: Plot of *SS* vs. *T* showing freeze out of trap-assisted transport around 150 K. The dashed line shows $kT/q \times \ln(10)$.

III. RESULTS

We utilized reduced-temperature measurements to ensure that tunneling, rather than trap-assisted, current is the dominant transport mechanism in all devices tested. As an example, an AC-only-oriented TFET [8] was measured at temperatures ranging from 262 K to 77 K as shown in FIG. 2. Fitting the temperature-dependent data for 150 K < *T* < 262 K, gave an activation energy of 0.19 eV in the subthreshold regime,

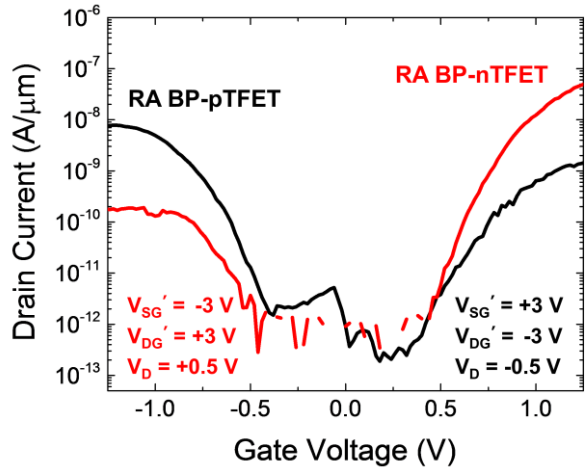

FIG. 3. I_D vs. V_G plots for RA BP pTFET (black) and nTFET (red) with symmetric relative source- and drain-gate bias voltages at V_D = -0.5 V and +0.5 V, respectively, and *T* = 77 K. (The nTFET characteristic has been shifted by -0.4 V for visual comparison).

indicating that higher-temperature transport is dominated by Shockley-Read-Hall (SRH) generation. However, for $T < 150$ K, except for a slight threshold voltage shift, the subthreshold transport is found to be independent of temperature. This trend is summarized in the inset to FIG. 2, which shows *SS* is nearly temperature independent below $T = 150$ K. This termination of temperature dependence indicates that the traps have been frozen out and tunneling is the primary transport mechanism in the subthreshold regime. Therefore, all measurements for the remainder of this paper were performed at $T = 77$ K.

Next, the transfer characteristics of the RA BP-TFET were measured and compared to those of the AC- and ZZ-only devices. In order to make a "fair" comparison, the values of the source- and drain-gate voltages had to be adjusted to ensure that the electrostatic doping on the source and drain sides were equal, thus ensuring that any remaining asymmetry could be attributed to the crystal orientation. To do this, I_D was measured in a p-MOSFET configuration where the source-gate was swept and the other gates were set at large negative voltages (ensuring the transistor was in the on-state) in order to determine the value at which the minimum current, I_{MIN}, was obtained. Based upon this knowledge, for the TFET measurements, the source- and drain-gate voltages were set such that they had equal values with respect to the voltage corresponding to I_{MIN}, and so we utilize the terminology V_{SG}' and V_{DG}' to represent source- and drain-gate voltages relative to the I_{MIN} point.

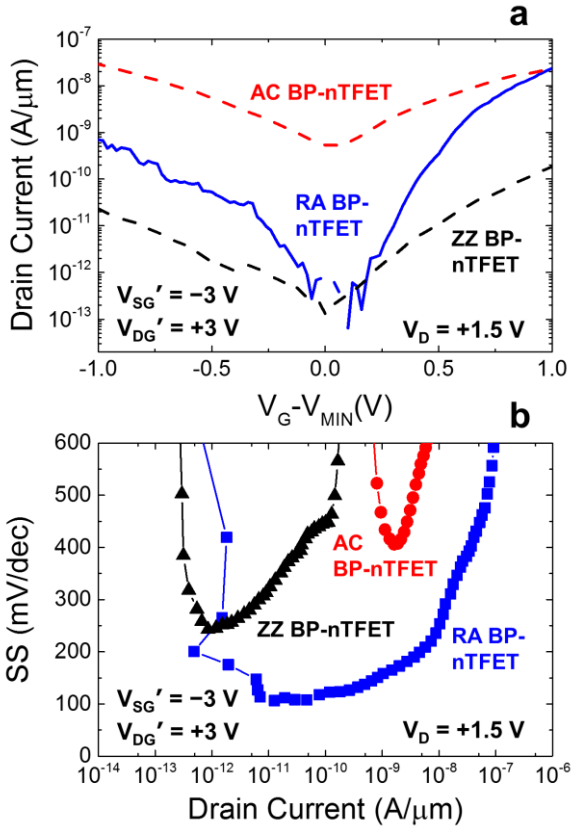

FIG. 4. (a) I_D vs. V_{GS} characteristics for AC-only (red), ZZ-only (black) and RA (blue) nTFETs under symmetric relative source- and drain-gate bias conditions at $V_D = +1.5$ V and $T = 77$ K (b) Subthreshold slope comparison for same devices in (a).

FIG. 3 shows the characteristics of the RA device, measured in both the nTFET and pTFET configurations. When measured as an nTFET, $V_{SG}' = -3$ V and $V_{DG}' = +3$ V, while in the pTFET configuration, $V_{SG}' = +3$ V and $V_{DG}' = -3$ V. The nTFET and pTFET were measured at $V_D = +0.5$ V and $V_D = -0.5$ V, respectively, and configured so that the source tunneling occurred in the AC direction and the drain tunneling was in the ZZ direction. Examining the two curves at $V_G = +1$V and $V_G = -1$V we can compare the tunneling current in the AC and ZZ direction at bias conditions of equivalent magnitude. This reveals an anisotropy of ~10^2 between the two directions.

To further explore the asymmetry, FIG. 4(a) shows the transfer characteristics of the RA BP nTFET alongside the isotropic AC- and ZZ-only nTFETs [8] at $V_D = +1.5$ V. The RA BP-TFET has I_{ON} roughly equal to that of the AC BP-TFET. However, in the AC BP-TFET, I_{MIN} is limited to ~1 nA/μm by ambipolar carrier injection, while in the current in the right-angle BP decreases to below 1 pA/μm, which is roughly equivalent to I_{MIN} for the ZZ BP-TFET. We further characterize the device improvement by plotting *SS* vs. I_D for the three TFETs (FIG. 4(b)) and see that the right-angle device has a *SS* twice as steep as the ZZ BP-TFET and four times as steep as the AC BP-TFET. This is because ambipolar carrier injection also degrades *SS* primarily by preventing the device from reaching the true off-state current (where tunneling at the source is turned off by tuning the channel potential). The RA BP-TFET is protected against this type of degradation due to effective mass anisotropy. Table I shows a summary of key metrics for all three devices based upon the data in FIG 4. We attribute the relatively low I_{ON} to the non-planar device geometry, which can increase the tunneling distance due to BP "bridging" at the boundary between the central gate and source- and drain-gates [8]. Improvements in *SS* can be made by reducing the gate dielectric thickness and fabricating the devices under more controlled environmental conditions. Therefore, substantial improvements in the TFET performance should be possible.

TABLE I. Comparison of BP nTFET performance.

Device	I_{ON} (nA/μm)	I_{ON}/I_{OFF}	SS_{MIN} (mV/dec)
AC nTFET	23	4.3×10^1	406 @ 2 nA/μm
ZZ nTFET	0.18	1.4×10^3	240 @ 0.9 pA/μm
RA nTFET	24	1.6×10^5	107 @ 20 pA/μm

IV. CONCLUSION

In conclusion, we have demonstrated a BP TFET with enhanced improved I_{ON}/I_{OFF} ratio and improved *SS* over symmetric BP TFETs. We achieved this by fabricating a right-angle device that utilizes the anisotropic effective mass in BP by ensuring source tunneling occurs along the low mass, AC crystal axis and drain tunneling occurs along the high mass, ZZ crystal axis. This experimental demonstration is an important step towards realizing TFETs with 2D materials that can achieve $SS < 60$ mV/dec with high I_{ON}.

REFERENCES

[1] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329-337, Nov. 2011. Doi: 10.1038/nature10679.

[2] H. Lu, and A. Seabaugh, "Tunnel field-effect transistors: state-of-the-art," *IEEE J. Elect. Dev. Soc*., vol. 2, pp. 44-49, May 2014. Doi: 10.1109/JEDS.2014.2326622.

[3] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, T. Kosel, M. Wistey, H. Xing, and A. Seabaugh, "AlGaSb/InAs tunnel field-effect transistor with on-current of 78 μA/μm at 0.5 V," *IEEE Elect. Dev. Lett*., vol. 33, pp. 363-365, Mar. 2012. Doi: 10.1109/LED.2011.2179915.

[4] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and I_{on} = 10 μA/μm for I_{off} = 1 nA/μm at V_{DS} = 0.3 V," IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 4-7, 2016. Doi: 10.1109/IEDM.2016.7838450.

[5] A. Szabo, S. J. Koester, and M. Luisier, "*Ab-initio* simulation of van der Waals $MoTe_2$-SnS_2 heterojunction TFETs for low power electronics," *IEEE Elect. Dev. Lett*., vol. 36, pp. 514-516, May 2015. Doi: 10.1109/LED.2015.2409212.

[6] T. Roy, M. Tosun, M. Hettick, G. H. Ahn, C. Hu, and A. Javey, "2D-2D tunneling field-effect transistors using WSe_2/$SnSe_2$ heterostructures," *Appl. Phys. Lett*., vol. 108, 083111, Feb. 2016. Doi: 10.1063/1.4942647.

[7] T. A. Ameen, H. Ilatikhameneh, G. Klimeck, and R. Rahman, "Few-layer phosphorene: An ideal 2D material for tunnel transistors," *Sci. Rep*., vol. 6, 28515, Jun. 2016. Doi: 10.1038/srep28515.

[8] M. C. Robbins, and S. J. Koester, "Crystal-oriented black phosphorus TFETs with strong band-to-band-tunneling anisotropy and subthreshold slope nearing the thermionic limit," International Electron Devices Meeting (IEDM), San Francisco, CA, Dec. 3-6, 2017. Doi: 10.1109/IEDM.2017.8268399.

[9] P. Wu, T. Ameen, H. Zhang L. A. Bendersky, H. Ilatikhameneh, G. Klimeck, R. Rahman, A. V. Davydov, and J. Appenzeller, "Complementary black phosphorus tunneling field-effect transistors," *ACS Nano*, vol. 13, pp. 1377-1385, Feb. 2019. Doi: 10.1021/acsnano.8b06441.

[10] P. Wu, and J. Appenzeller, "Reconfigurable black phosphorus vertical tunneling field-effect transistor with record high on-currents," *IEEE Elect. Dev. Lett*., vol. 40, pp. 981-984, Jun. 2019. Doi: 10.1109/LED.2019.2909176.

[11] S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey, and A. Roelofs,, "Tunable transport gap in phosphorene," *Nano Lett*., vol. 14, pp. 5733-5739, Oct. 2014. Doi: 10.1021/nl5025535.

[12] J. Qiao, X. Kong, Z.-X. Hu, F. Yang, and W. Ji, "High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus," *Nat. Commun*., vol. 5, 4475, Jul. 2014. Doi: 10.1038/ncomms5475.

[13] H. Ilatikhameneh, T. Ameen, B. Novakovic, Y. Tan, G. Klimeck, and R. Rahman, "Saving Moore's law down to 1 nm channels with anisotropic effect mass," *Sci. Rep*., vol. 6, 31501, Aug. 2016. Doi: 10.1038/srep31501.

[14] M. C. Robbins and S. J. Koester, "Black phosphorus p- and n-MOSFETs with electrostatically doped contacts," *IEEE Elect. Dev. Lett*., vol. 38, pp. 285-288, Feb. 2017. Doi: 10.1109/LED.2016.2638818.

[15] J. Wu, N. Mao, L. Xie, H. Xu, and J. Zhang, "Identifying the crystalline orientation of black phosphorus using angle-resolved polarized Raman spectroscopy," *Angew. Chem*., vol. 54, pp. 2366-2369, Feb. 2015. Doi: 10.1002/anie.201410108.

[16] N. Haratipour, Y. Liu, R. J. Wu, S. Namgung, P. P. Ruden, K. A. Mkhoyan, S.-H. Oh, and S. J. Koester, "Mobility anisotropy in black phosphorus MOSFETs with HfO_2 gate dielectrics," *IEEE Trans. Elect. Dev*., vol. 65, pp. 4093-4101, Oct. 2018. Doi: 10.1109/TED.2018.2865440