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ABSTRACT

Two buffer traps at E_C-0.7 eV and E_C-0.8 eV have been individually identified as causing threshold voltage and on-resistance instabilities in β-Ga_2O_3 Si ∂-doped transistors grown by plasma-assisted molecular beam epitaxy (PAMBE) on semi-insulating Fe doped β-Ga_2O_3 substrates. The instabilities are characterized using double-pulsed current-voltage and isothermal constant drain current deep level transient spectroscopy. The defect spectra are compared between transistors grown using two different unintentionally doped buffer layer thicknesses of 100 nm and 600 nm. The E_C-0.8 eV trap was not seen using the thicker buffer and is shown to correlate with the presence of residual Fe in thePAMBE buffer layer. The E_C-0.7 eV trap was unchanged in concentration and is revealed as the dominating source of the threshold voltage instability. This trap is consistent with the characteristics of a previously reported intrinsic point defect [Ingebrigtsen *et al.*, APL Mater. 7, 022510 (2019)]. The E_C-0.7 eV trap is responsible for ~70% of the total threshold voltage shift in the 100 nm thick buffer transistor and 100% in the 600 nm thick buffer transistor, which indicates growth optimization is needed to improve β-Ga_2O_3 transistor stability.

Beta-phase gallium oxide (β-Ga_2O_3) is a promising ultrawide bandgap material for next generation high voltage electronics due to its large bandgap of ~4.6–4.8 eV,[1–3] high theoretical breakdown field of ~8 MV/cm, and large Baliga figure of merit, meaning that a higher breakdown voltage can be achieved without increasing the device on-resistance. Already, β-Ga_2O_3 devices with high breakdown voltages and breakdown fields have been reported, surpassing limits of the competitive material systems of GaN and SiC.[4–6] Additionally, the large theoretical Johnson figure of merit for β-Ga_2O_3 devices indicates its potential for RF device applications.[7] Recently, cutoff frequencies of 27 GHz, 3.3 GHz, and 3.1 GHz have been demonstrated showing the promise for RF transistors.[8–10] One of the most impactful pragmatic advantages of β-Ga_2O_3 devices for future technology implementation is that β-Ga_2O_3 is available as large area substrates, meaning that epitaxial devices can be grown homoepitaxially, suggesting that dislocation-mediated degradation might not be a future limiting factor in performance and reliability.[11–14]

For β-Ga_2O_3 transistors, however, the ability to grow devices on semi-insulating (S.I.) substrates and/or buffer layers is crucial for achieving maximum device performance. To date, it is typical for S.I. β-Ga_2O_3 to be formed via intentional doping using Fe or Mg to pin the Fermi level deep within the bandgap. The possible challenge of this is that during device operation, occupancy of these states can vary, creating instabilities in transistor parameters. This phenomenon has been widely reported for GaN RF devices[15–17] and is already observed to be an issue for β-Ga_2O_3 devices.[18,19] There is also a concern for the thermal stability of the deep acceptor and donor dopants[20] at elevated temperatures and potential diffusion out of a S.I. substrate into epitaxially grown device layers. Recent work has shown diffusion characteristics for Fe, N, and Mg-doped β-Ga_2O_3.[21,22] This work focuses on the issue of Fe diffusion into epitaxial layers and builds from our previous work where two traps, at E_C-0.7 eV and E_C-0.8 eV, were detected in plasma-assisted molecular beam epitaxy (PAMBE) grown Si δ-doped β-Ga_2O_3 transistors on Fe doped S.I. substrates.[18] Here, a quantitative comparison and trap analysis was performed on β-Ga_2O_3 δ-doped MESFETs grown on Fe-doped S.I. substrates as a function of the unintentionally doped epilayer thickness between the substrate and

channel, commonly called the buffer. This enables clear differentiation between substrate-related and epitaxial layer-related sources of traps.

Two device structures were studied with buffer thicknesses of 100 nm and 600 nm as shown in Figs. 1(a) and 1(b), respectively. These structures were grown by plasma-assisted molecular beam epitaxy (PAMBE) on (010) edge-defined film-fed grown (EFG) Fe doped semi-insulating substrates. The growths were performed in an oxygen-rich condition with a substrate temperature of 700 °C using Si δ-doping to provide charge in the channel.[23] This results in high-quality material with Hall channel densities of 1.38×10^{13} cm^{-2} and 1.57×10^{13} cm^{-2} and mobilities of 65 cm^2/V s and 105 cm^2/V s for the 100 nm and 600 nm devices, respectively.[24]

The MESFETs were processed by first etching the source and drain contact regions, and then a heavily doped layer was regrown by MBE and patterned through a lift off process with a silicon dioxide mask. A Ti/Au/Ni source/drain metal contact was formed through electron beam evaporation and photoresist lift-off patterning with a one minute anneal at 470 °C in an N_2 atmosphere. This MBE regrowth contact process yields contact resistances of ~0.35–0.44 Ω mm.[24] After inductively coupled plasma-reactive ion etching plasma etching for mesa isolation, the Ni/Au/Ni Schottky gates were patterned through lift-off as well. More details of the processing techniques and growth are explained in the work by Xia *et al.*[25] This process resulted in transistors with maximum drain currents, I_D, between 140 and 180 mA/mm with a gate source voltage, V_{GS}, set to 0.0 V.

To study the impact of trap-induced instabilities in the transistor structures, two techniques were used: double-pulsed current-voltage (I-V) and isothermal constant drain current DLTS (CI_D-DLTS). The combination of these measurements allows traps to be characterized individually and the impact of each trap on the transistor stability to be quantified. Along with information learned from other studies, the physical sources of the traps can be identified and strategies to mitigate the trap-induced problems can be developed.

Using a Keithley SCS-4200, with two fast pulse modules, double-pulsed I-V was performed to understand the changes in the threshold voltage (V_T) and the on-resistance (R_{on}). In the pulsed I-V measurements, the quiescent bias controls the quasi-Fermi levels throughout the device, which enables the trap occupation in different regions of the device to be separately controlled during the measurements. Additionally, the characteristic curves can be measured before any significant trap emission occurs by the control of the pulse widths. Self-heating effects can complicate the defect analysis, but the fast pulsing nature of the measurement and low-power quiescent conditions mitigate self-heating effects. These qualities allow the total dispersion between the cases of traps filled and traps empty to be measured. In this study, zero-bias quiescent ($V_{GS,q} = V_{DS,q} = 0$ V) and high-V_{DS} pinch-off quiescent conditions are used.

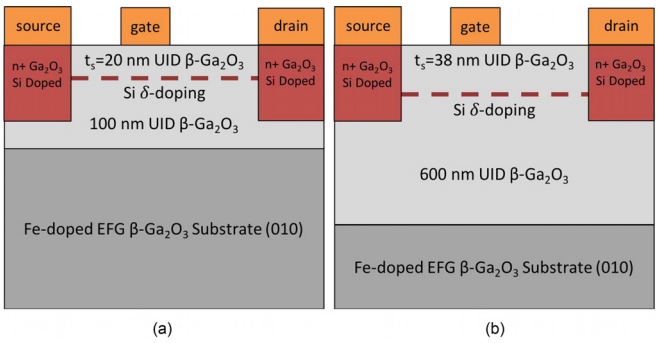

FIG. 1. Cross-sectional diagrams of the grown and processed MESFETs. The dashed line represents the silicon δ-doping channel. The Ohmic contacts utilize an MBE regrown heavily doped region to reduce contact resistance to the channel and metal. (a) is the 100 nm buffer sample with a gate-channel spacing of 20 nm, while (b) is the 600 nm buffer sample with a spacing of 38 nm.

While pulsed I-V gives insight into how total trapping effects manifest in terminal characteristics, isothermal CI_D-DLTS is a technique that determines the traps' energies and cross sections through temperature dependent exponential trap emission transients.[26] A high-V_{DS} pinch-off trap filling pulse is applied for 100 ms. Then, the device is biased to a fixed low V_{DS} and constant I_D in the saturation regime that is maintained by dynamically controlling V_{GS} to record the emission transients. Under these conditions, $\Delta V_{GS} \approx \Delta V_T$, where V_T is affected by trapping under the gate. The isothermal transients were done in a temperature range of 270 K–360 K in 10 K increments and analyzed following Ref. 26 to extract the time constant of each trap at each temperature. These data are used in an Arrhenius plot to extract the trap energy and cross section and to compare with previously reported data.

To determine the effect of traps on the channel charge in both pulsed I-V and gate-controlled (GC) CI_D-DLTS using the gate capacitance, the change in the threshold voltage can be calculated as a change in the sheet charge concentration in the channel, which is defined as

$$N_{T,sheet} = \frac{\varepsilon_s}{q t_s} |\Delta V_T|, \tag{1}$$

where ε_s is the β-Ga_2O_3 permittivity of 10.2 from Refs. 27 and 28, t_s is the spacer thickness between the gate and channel, and ΔV_T is the total threshold voltage instability due to one or more traps. The trap concentration allows for comparison of the MESFETs even with different spacer thicknesses.

The results of the pulsed I-V measurements, which are consistent over multiple devices on each sample, indicate significant dispersion in both V_T and R_{on} as shown in Fig. 2. The difference in the curves at each quiescent condition is caused by the change in trap occupation. The zero bias condition is the empty condition with more charge in the channel and a more negative V_T, while the high-V_{DS} pinch-off condition has a more positive V_T, indicating filled traps and a reduction in channel charge. Under a pinch-off condition with a high-V_{DS}, the channel charge no longer screens the buffer from the electric fields, which allows electrons to be pushed into the buffer as described in Ref. 18. The V_T instability was only observed after pulsing with $V_{GS} \leq V_T$, indicating surface states are not playing a role in the V_T instability and the traps are in the buffer. The buffer traps are expected to fill through the raised electron quasi-Fermi level in the buffer due to gate leakage.[18] In addition to the threshold voltage shift, there is also an observed dynamic R_{on} shown in Figs. 2(c) and 2(d), which is also due to trapping effects. While the R_{on} effects are interesting to study for device performance concerns, this study focuses on the impact of traps on V_T. The threshold voltage instabilities measured in this work are done in the saturation regime, which is not sensitive to R_{on} effects. Additionally, since the traps are in the buffer region, as explained above and in detail in Ref. 18, surface states are not significantly influencing the threshold voltage.

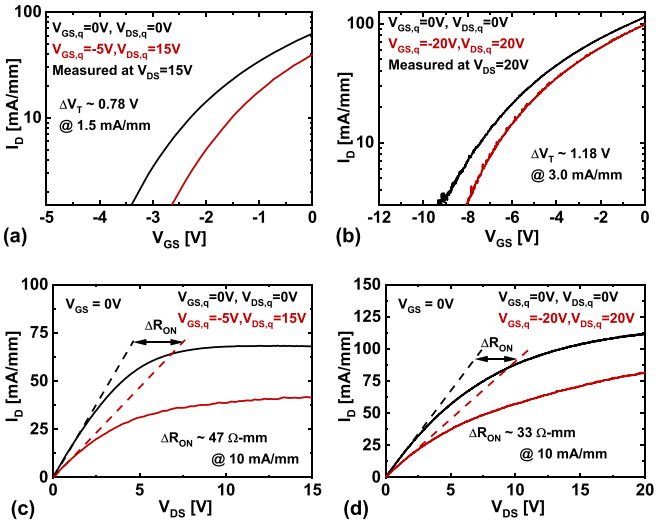

FIG. 2. Double-pulsed 50 μs pulsed current-voltage transfer curves for the (a) 100 nm buffer thickness and (b) 600 nm buffer thickness MESFETs with quiescent conditions shown in the figures. The double-pulsed output curves are also plotted in (c) and (d) for the 100 nm and 600 nm buffer, respectively. The zero-bias quiescent condition (black) represents the nontrapped state, while the high-V_{DS} pinch-off quiescent condition (red) exacerbates the trapping effect. Both devices show dispersion between the two conditions, indicating an electron trapping mechanism below the channel is responsible.

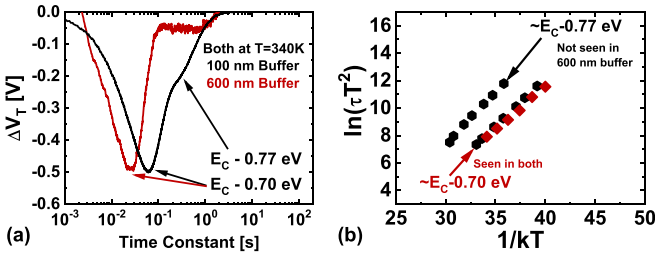

FIG. 3. Isothermal analysis of gate voltage transients in (a) is done from 270 K to 340 K where the gate voltage was dynamically adjusted to maintain drain currents of 1.5 mA/mm and 3.0 mA/mm for the 100 nm and 600 nm buffer samples, respectively. Two trap levels are revealed at approximately 0.77 eV (shoulder of 100 nm curve) and 0.70 eV below the conduction band by extracting from the Arrhenius plot in (b). The flat region after the peak in the 600 nm curve is temperature independent and has no discernible peak; therefore, it is not expected to be a trap emission.

When looking at devices with different layer thicknesses, the measured V_T shift itself is not useful to be directly compared because it depends on both the trap concentration and spacer thickness as shown in Eq. (1). The trap concentration is the best metric for comparison because it removes the influence of device design. For example, even though the 600 nm buffer sample's ΔV_T in Fig. 2(b) was about 0.4 V larger than the 100 nm buffer sample in Fig. 2(a), the total $N_{T,sheet}$, calculated using Eq. (1), is slightly smaller in the 600 nm buffer sample with a concentration of $1.8 \times 10^{12}\,\mathrm{cm}^{-2}$ compared with $2.2 \times 10^{12}\,\mathrm{cm}^{-2}$ in the 100 nm buffer sample. The larger V_T shift with a smaller trap concentration is due to the larger spacer thickness in the 600 nm sample. To compare a device level parameter, an effective ΔV_T can be calculated using the trap concentrations above assuming a 20 nm spacer to allow for a direct comparison of ΔV_T. Using Eq. (1), ΔV_T values of 0.65 V and 0.78 V are calculated for the 600 nm and 100 nm buffer samples, respectively. This calculation indicates a 0.13 V smaller effective ΔV_T in the 600 nm buffer sample, which is consistent with the reduced impact of the Fe-doped substrate on trapping effects which is shown in the defect spectroscopy results next.

Isothermal GC CI_D-DLTS was done on both MESFETs to identify traps that may be present, which can be linked to the threshold voltage behavior observed in the pulsed I-V measurements. Measurements made on the 100 nm buffer MESFET revealed two distinct electron trap levels, one appearing as the dominant negative peak and the other as a smaller magnitude shoulder, shown in Fig. 3(a). The E_C-0.7 eV trap is responsible for ~70% of the signal, determined by dividing its peak height to the sum of both the E_C-0.7 eV and E_C-0.8 eV peak heights. In contrast, measurements made on the MESFET with the 600 nm buffer revealed the presence of only one DLTS peak, and therefore, the E_C-0.7 eV is fully responsible for the dispersion. The single peak in the 600 nm buffer's spectrum was slightly shifted (~30 ms) in the main peak time constant. This shift could be due to the higher current level in the 600 nm buffer MESFET. Nonetheless, the correct method to compare traps detected by DLTS in any material or device is to compare the full Arrhenius characteristics for a trap, where the trap emission properties (activation energy and cross section) can be observed over a wide range of temperature measurements, not just at a single peak temperature. This enables unambiguous comparisons. The Arrhenius data for all the detected traps in both MESFET samples are shown in Fig. 3(b). It is clear that the main DLTS peak seen for the 100 nm buffer MESFET aligns with the single trap seen for the 600 nm buffer MESFET, having a trap activation energy of E_C-0.7 eV. As will be discussed below, this trap matches a trap seen in several prior works done on gallium oxide material test structures and was attributed to an intrinsic point defect source. The Arrhenius data, in Fig. 3(b), for the shoulder trap seen in the 100 nm buffer MESFET are clearly distinct from the main trap, with an energy level at E_C-0.8 eV. Even with the seemingly close energy level positions (~<0.1 eV difference), the distinct nature of both traps is clear, suggesting different physical sources for each.

The lack of the E_C-0.8 eV trap in the 600 nm thick buffer MESFET is telling, especially after considering the Fe concentration profile obtained using secondary ion mass spectroscopy (SIMS), which is shown in Fig. 4. There is a measurable Fe concentration tail extending from the substrate approximately 200 nm into the epitaxial layer before it falls below SIMS detection limits of $1 \times 10^{15}\,\mathrm{cm}^{-3}$. Since the 600 nm buffer increases the separation of the Fe doped substrate and the channel, it is proposed that the E_C-0.8 eV level's absence in the CI_D-DLTS links this trap to the presence of Fe impurities in β-Ga_2O_3. This is due to the regions of higher concentration of Fe being significantly farther from the channel and thus can no longer influence the threshold voltage significantly because of a small channel to substrate capacitance.

To gain more insights into the physical sources for the E_C-0.8 eV and 0.7 eV traps, Fig. 5 compiles a wide range of trap Arrhenius characteristics from a wide range of DLTS studies made on β-Ga_2O_3 substrate materials grown by edge defined film fed growth (EFG) and Czochralski (CZ) methods, on substrates having different crystal orientations, and on materials that had been exposed to high energy particle radiation. The MESFET-based CI_D-DLTS Arrhenius data are replotted in this figure to compare with prior material-level studies.

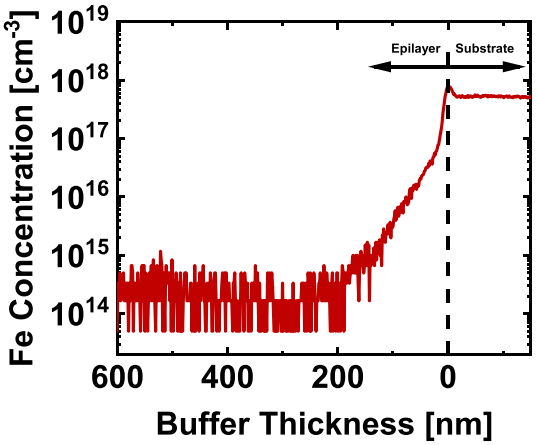

FIG. 4. Fe SIMS profile for the thick UID that shows Fe tail from the substrate into the epitaxial layer. The MBE/substrate interface is at 0.0 nm buffer thickness. The tail of the Fe from the substrate hits the detection limit near ~200 nm into the buffer. Therefore, the 600 nm buffer has approximately 400 nm UID material with an Fe concentration below the detection limit before the channel.

The results are unambiguous. First, the E_C-0.8 eV trap seen here in the MESFET studies clearly matches a trap that has already been linked to Fe impurities.[32,33] In fact, theoretical work has suggested the physical configuration of this defect to be a Fe_{Ga} substitutional point defect, though it is not yet clear whether the Ga site is the preferential octahedral site (Ga_{II}) or the tetrahedral (Ga_I), both of which have similar energies.[32] What is important is the source of this trap is likely to be Fe, as conjectured in this work directly through its contribution to the V_T shift on the MESFET. It should be noted in the prior literature, this E_C-0.8 eV trap has been labeled as the E2 trap.[32,34] Second, the E_C-0.7 eV trap observed by CI_D-DLTS on the MESFET

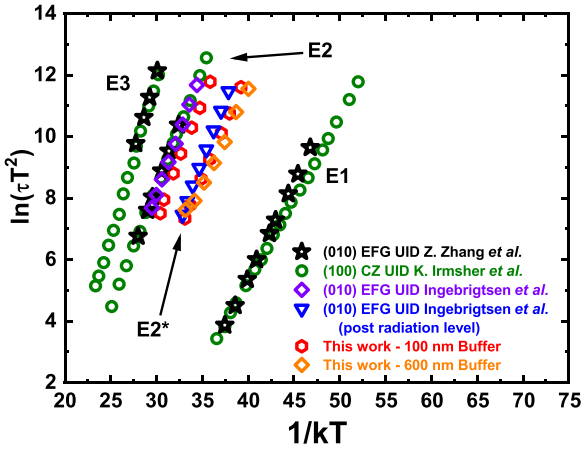

FIG. 5. Combined Arrhenius plot including bulk samples[29,30] for accurately comparing reported trap levels. The E_C-0.7 eV level measured here and the previously reported E2* level agree closely in Arrhenius space and are linked to an intrinsic defect.[31] The disappearance of the E_C-0.8 eV level in the 600 nm buffer sample indicates it is related to the Fe from the substrate, which is consistent with other reports.[32,33]

aligns with the previously reported E2* trap, which has been connected to intrinsic defect sources via high energy particle radiation studies using DLTS.[31] Moreover, density functional theory calculations predict that several intrinsic point defect structures can generate an energy level in this energy range, including V_{Ga} and Ga_O defects.[31] While the precise physical source of this native defect is still under investigation, what is important here is the intrinsic origin of this trap. Considering the large effect this E_C-0.7 eV trap has on the measured transistor V_T shift indicates significant growth optimization is still necessary to mitigate its effect from ~1 V to an acceptable level around less than 0.1 V.

In conclusion, two trap levels, at E_C-0.7 eV and E_C-0.8 eV, are shown to directly cause threshold voltage instabilities in β-Ga_2O_3 transistors grown by PAMBE on Fe doped gallium oxide substrates. The E_C-0.8 eV level has been correlated with Fe_{Ga} defects, and its impact on the V_T instability is mitigated when the buffer thickness is increased. In this device design, a 600 nm buffer is sufficient to mitigate the Fe-related V_T instability. On the other hand, the concentration of the E_C-0.7 eV level is found to be unaffected by the buffer thickness, which is consistent with its prior assignment to a native point defect source. Since this level is responsible for ~70% of the V_T instability in the 100 nm buffer sample and all the V_T instability in the 600 nm buffer sample, it is important to further optimize growth conditions in order to eliminate this primary source for the V_T instability that is currently observed for PAMBE-grown β-Ga_2O_3 devices.

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