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The upgraded camera for the prototype Schwarzschild-Couder Telescope of the Cherenkov Telescope Array

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ABSTRACT

The Schwarzschild-Couder Telescope (SCT) is a mid-size telescope proposed for the Cherenkov Telescope Array. In order to substantially improve the field of view and image resolution compared to i traditional Davies-Cotton telescopes, innovative solutions are foreseen in the design, like the use of Silicon Photomultipliers (SiPM) as light sensors and waveform digitizers for recording the fast light signals from atmospheric showers.

A project is now underway to upgrade the camera by increasing its pixel count to $11,328$ pixels and field of view of $8.0°$. The camera electronics has been completely redesigned by using new waveform digitizer and trigger ASICs with the final goal of lowering the gamma-ray energy threshold and therefore provide an excellent instrument tailored for extended sources investigations and multi-messenger astronomy.

Keywords: Cherenkov Telescope, TARGET, SiPM

1. INTRODUCTION

The Cherenkov Telescope Array (CTA) is an array of Imaging Atmospheric Cherenkov Telescopes (IACTs) for detecting gamma rays with energies ranging between 20 GeV and 300 TeV.[1] Such gamma rays can be detected via Cherenkov light emission of secondary charged particles, produced in the interaction with the atmosphere. Several telescopes will be used as a ground array to increase the probability of a shower detection, moreover, by optimizing of the geometrical configuration at ground and by exploiting a stereoscopic reconstruction, a robust rejection of background can be obtained. The current CTA project consists of two array sites, one in the Northern and one in the Southern hemisphere to cover the entire sky. The CTA observatory will consist of three sizes of telescopes, small-, mid- and large-sized telescopes to most efficiently cover the energy range of interest. The different telescopes design has benefitted from the expertise acquired in the last generation of Cherenkov telescopes, namely the High Energy Stereoscopic System (H.E.S.S.), the Major Atmospheric Gamma Imaging Cherenkov Telescopes (MAGIC) and the Very Energetic Radiation Imaging Telescope Array System (VERITAS).[2–4]

Traditionally, Cherenkov telescopes have been designed following Davies-Cotton single mirror optics, however better focusing and greater field of view can be achieved by using the Schwarzschild-Couder optics,[5] as done by the ASTRI and the Gamma-ray Cherenkov Telescope (GCT)[6,7] small-size telescopes of CTA.

A prototype telescope (pSCT) has been constructed to prove a new dual-mirror optics design on the scale of a mid-sized telescope for CTA. The telescope will have a field of view of $8°$ with an angular pixel size of $0.067°$. This improvement of the optical performance requires a camera of approximately $0.45\ m^2$, providing a pixel size of millimeter scale.

The pSCT is currently located at the Fred Lawrence Whipple Observatory (FLWO) in Arizona, it has been inaugurated on January 17, 2019 and its commissioning is ongoing.

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2. THE UPGRADED PSCT CAMERA

A lot of efforts are going in the design of a better performing camera electronics, from new photon sensors to new digitizing electronics, with the aim of enhancing performance and lowering noise, especially at trigger level.

The main challenge in detecting the Cherenkov light from showers in a telescope like pSCT is that duration is very short – $\mathcal{O}(1ns)$ – and that the pixel sizeis very small, approximately 6×6 mm^2, for a corresponding high pixel density and a very compact electronics placement.

The current pSCT camera meets this challenge by using SiPMs as photon sensors and a specially designed application specific integrated circuit (ASIC), the TARGET chip, as the core of the front-end electronics.[8,9] The modules currently mounted on the pSCT camera are using the 7^{th} version of the TARGET chip, i.e. TARGET7, that is able also to provide a fast trigger path. Unfortunately, the noise level in TARGET7 was exceeding the pSCT camera requirements. It was then decided to split the trigger and digitization tasks in two separate ASICs, the T5TEA for bias control and trigger and the TARGET-C[10] for digitization only. This change will significantly reduce the noise on both digitized signals and the trigger, allowing for single photon triggering and resolution.

The photon sensors and readout electronics are integrated into camera modules that consist of two parts, the Focal Plane Module (FPM) and the Front-End Electronics (FEE) (see Figure 1).

The FPM of each camera module holds 64 SiPM pixels that are mounted on 4 quadrants and connect to individual boards for preamplification (see Figure 2). To ensure the temperature stabilization of the SiPMs, the sensor assembly is cooled by a peltier, that is visible in the metallic cage opening between the FPM and the FEE, driven by a micro-controller located on the FEE.

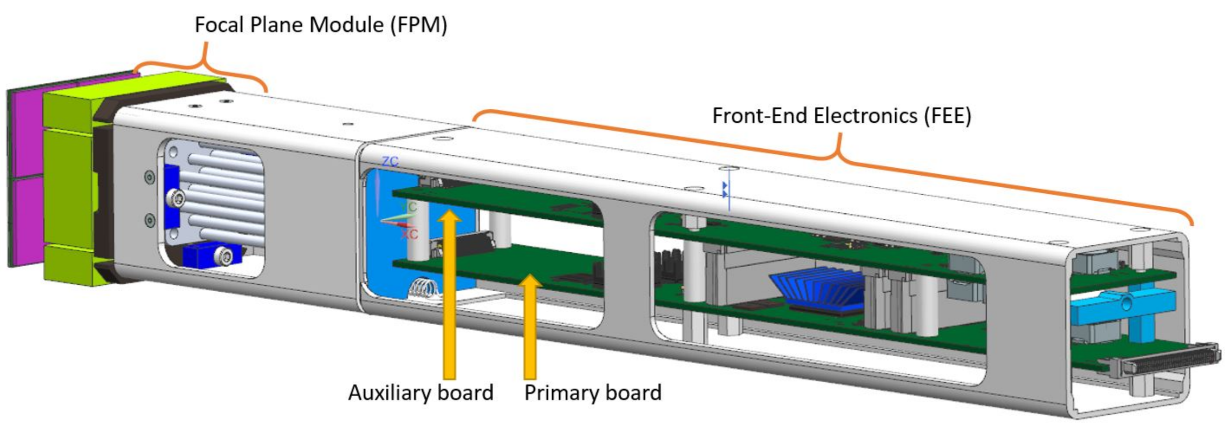

Figure 1. Drawing of the pSCT camera module divided into an FPM (front) and a FEE (rear) parts. Between the two, the peltier cooling is visible through the opening of the metal cage. Inside the casing, the FEE module is made by an Auxiliary and a Primary boards.

The camera body is designed to hold 177 modules which cover the entire focal plane of the pSCT optics. Currently it is equipped with 25 modules providing 1600 pixels which cover a field of view of 2.7°. More details on the current status of the pSCT camera can be found in.[11]

The camera modules slide into the hexagonal camera body and connect to a main circuit board called backplane. The backplane handles individual power control and monitoring for up to 32 modules, as well as synchronous clock distribution and physical routing of network connections between the modules and modified network switches. Furthermore, it includes the trigger logic for combining the camera module trigger signals using a single FPGA that looks for triggers in 3 adjacent pixels within a coincidence window of a few nanoseconds. Found coincidences are latched to a 1 ns clock and a readout request, including the necessary timing information, is sent to all connected camera modules.

The pSCT camera upgrades can be summarized as follows:

- new generation of photon sensors,

- improvements in the camera module electronics,
- full population of the camera body with all 177 modules with consequential re-evaluation of the heat management system,
- redesign and improvement of the backplane electronics and auxiliary systems.

We will now focus on the first two points.

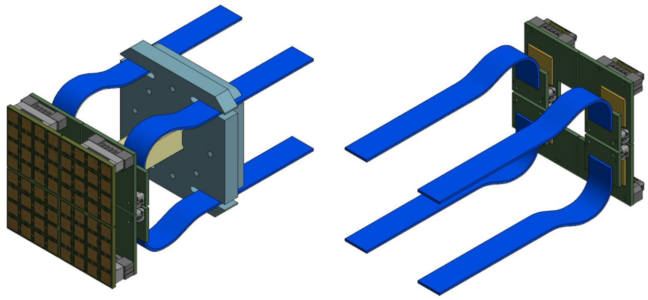

Figure 2. Arrangement of FPM. The SiPMS are located on 4 independent boards (quadrants), each interfaced to a smaller board housing the SMART ASICs for amplification.

2.1 The Focal Plane Module

The upgraded pSCT camera will be equipped with a new generation of Silicon Photomultipliers (SiPMs) based on the High Density technology (NUV-HD devices) developed by Fondazione Bruno Kessler (FBK). The SiPMs belonging to latest generation of 6×6 mm^2 SiPMs (called "NUV-HD3") are more sensitive to the near ultraviolet wavelengths, their photon detection efficiency (PDE) being optimized to match the spectrum of the Cherenkov light, and the cross talk has been reduced. They exhibit a peak photon detection efficiency greater than 50% and a reduced temperature dependence of gain and photon detection efficiency around 0.5 % per celsius.

A few more key features of the FBK NUV-HD3 sensors are:

- a dark rate of 150 kHz/mm^2, when operated with a bias voltage of 6 V above the specific breakdown voltage,
- a SiPM microcell size of 40 μm,
- optical crosstalk between microcells within a pixel of less than 20%, and
- a cell recovery time of 100 ns.

More information on the third generation of the FBK NUV-HD sensors can be found in[12] and.[13]

Figure 3 shows the PDE measured on SiPMs of different sizes and of different productions (labeled type 2 and type 3). The results a very similar behaviour of the different devices, with PDE peaking around 350 nm with a value larger than 50%.

In current camera modules, the photon sensors are connected to the readout electronics via 30 cm long micro-coaxial ribbon cables. These cables are routed along the aluminum module housing and electromagnetic interference can disturb the non-amplified SiPM signals. This problem is expected to be mitigated by using better filtering on the power regulators, moving the signal amplification circuits closer to the SiPMs, and only transmitting amplified signals via the cables.

A custom ASIC, the SMART chip,[13] is currently being developed to amplify 16 SiPM channels. It will provide shaping and amplification of the analog signals, as well as individual current measurements and bias voltage control for the SiPMs. The small packaging allows the chip to be deployed close to the SiPM boards and transmit the amplified signals via shorter cables to the readout electronics. This also neatens the infrastructure

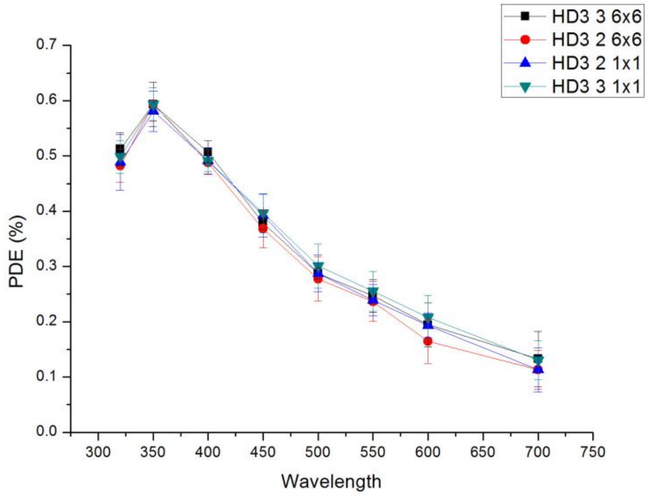

Figure 3. Photon detection efficiency as a function of wavelength measured on different devices of same technology.

configuration on the two FEE boards which gives more flexibility to optimize module operation. The SMART will be controlled via a Serial Peripheral Interface (SPI) bus from the FPGA of the FEE module.

The combined performance of the NUV-HD photon sensors with the first revision of the SMART ASIC and a TARGET C readout is shown in Figure 4. A second revision of SMART ASIC is currently being fabricated and tested.

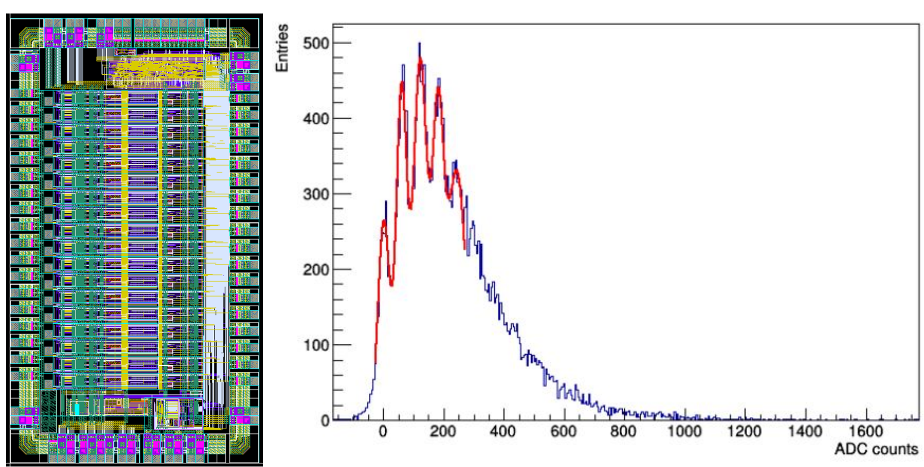

Figure 4. A micro-photograph of SMART v2 (left) and charge distribution of amplified signals from SiPMs obtained with SMART v1 (right)

2.2 The Front End Electronics Module

In order to contain the electronics noise to the lowest levels, the FEE module has been completely re-designed and it has been split into two boards, and Auxiliary and Primary board. Thanks to the similarity between the pSCT and the CHEC cameras, a common layout strategy was implemented, that is to keep well-separated areas for analogue and digital/power circuitry (see Figure 5, therefore by isolating the analog and digital noise sources and avoiding any noise return path on the analog chain.

Each board is collecting 32 analog signals therefore the trigger and digitization tasks are evenly divided between the two boards, housing 2 TARGET-C and 2 T5TEA chips each.

The FEE module performs several tasks:

- communicates with the SMART amplifiers to control the SiPM bias; and the signal shaping parameters;
- controls the T5TEA chips for setting the signal pedestal and providing fast triggers;
- digitizes the analog signals from the SiPMs via the TARGET-C chips;
- stabilizes the sensors temperature by communicating with the micro-controller;
- communicates with the backplane for data trasfer and slow control.

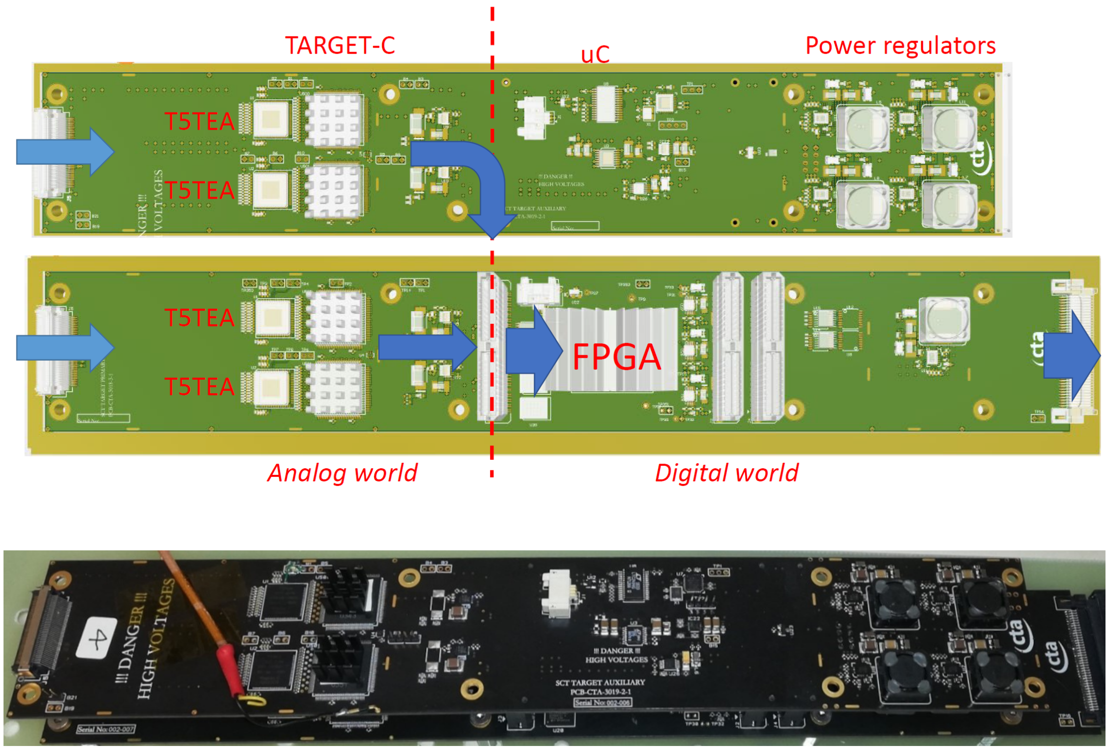

Figure 5. (top) Sketch of the upgraded camera FEE module, the Auxiliary and Primary boards are shown on top and bottom, respectively. Both boards have been logically divided into an analog and digital/power sections. (bottom) Picture of the prototype FEE module currently under test.

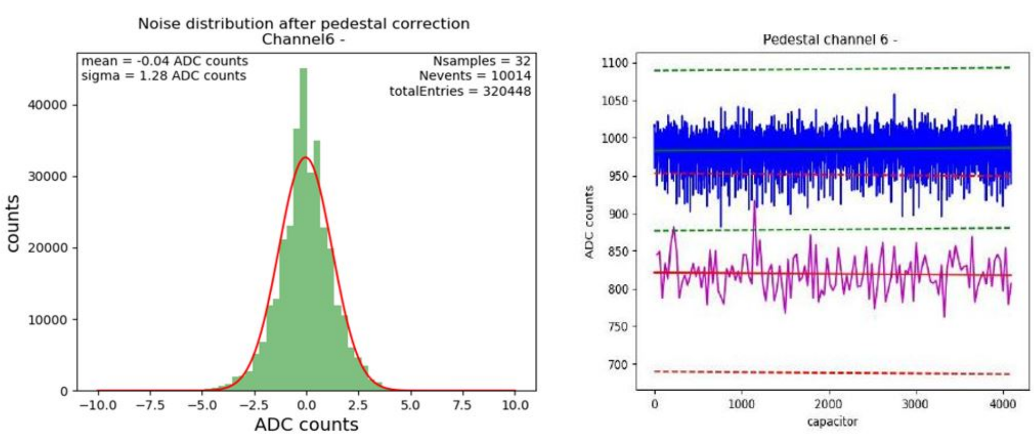

Figure 6. Distribution of the cell pedestal (left) and dependence on the cell number (right).

A Xilinx Artix-7 FPGA (XC7A100T-FGG484) is located on the Primary board, it is responsible for setting up the TARGET-C and T5TEA chips. Furthermore, the FPGA retrieves the digitized data, formats them and sends them to the backplane connector via Gbit UDP protocol. Moreover, the FPGA is also interfaced to the micro-controller that is managing a Peltier cell, located between the FPM and FEE, to maintain the sensors at stable temperature.

The first 4 prototypes of the FEE modules have been produced and are now under test by the institutions involved in the camera upgrade. Figure 6 shows the preliminary pedestal distribution, the overall noise level is 1.3 ADC counts only, and the mean value versus the capacitor cell from which no evident structure can be seen.

An important test has been done to evaluate the level of cross-talk between adjacent channels that can be due to the ASIC or trace routing. A 200 mV pulse, 8 ns width, has been injected in one channel (#9 in Figure 7). An average cross-talk value of 0.37 ± 0.12 % can be measured.

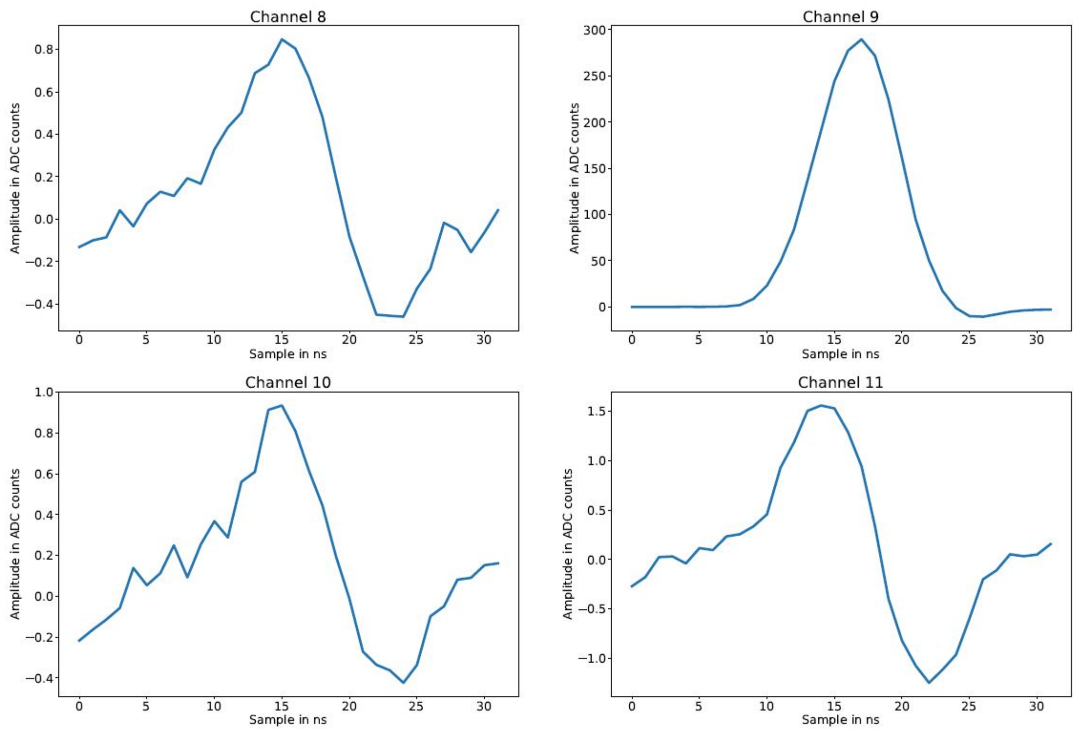

Figure 7. Cross-talk measurement. A 200 mV pulse is applied on channel #9 and the adjacent channels are checked for spurious signal.

3. SUMMARY AND OUTLOOK

The pSCT camera is undergoing a very important upgrade program. The purpose is two-fold: on one hand, to maximize the field of view, on the other hand to achieve a low trigger threshold that will allow the pSCT to start a physics campaign.

The camera electronics, in particular, is facing a major revision:

- new SiPM sensors with high PDE will be installed;
- dedicated ASIC for amplification near the sensors is being designed and tested;
- low-noise front-end electronics based on new trigger and digitization ASICs is also being designed and tested.

The current timeline for this upgrade project has the year 2019 mostly intended for prototyping, 2020 for construction of subsystems, and 2021 for the integration of the subsystems.

The pSCT upgrade program is part of NSF MRI and INFN funding. The current timeline for this upgrade project prioritizes the years 2019 for prototyping, 2020 for construction of subsystems, and 2021 for the integration of the subsystems and commissioning.

4. ACKNOWLEDGEMENTS

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* *https://www.cta-observatory.org/consortium_acknowledgments/*