Optimized Stress Testing for Flexible Hybrid Electronics Designs

Hang Gao, Ganapati Bhat, Umit Y. Ogras, and Sule Ozev
School of Electrical, Computer, and Energy Engineering
Arizona State University
Tempe, AZ, USA
{hgao44, gmbhat, umit, sule.ozev}@asu.edu

***Abstract*—Flexible hybrid electronics (FHE) is emerging as a promising solution to combine the benefits of printed electronics and silicon technology. FHE has many high-impact potential areas, such as wearable applications, health monitoring, and soft robotics, due to its physical advantages, which include light weight, low cost and the ability conform to different shapes. However, physical deformations in the field can lead to significant testing and validation challenges. For example, designers must ensure that FHE devices continue to meet their specs even when the components experience stress due to bending. Hence, physical deformation, which is hard to emulate, has to be part of the test procedures for FHE devices. This paper is the first to analyze stress experience at different parts of FHE devices under different bending conditions. We develop a novel methodology to maximize the test coverage with minimum number of text vectors with the help of a mixed integer linear programming formulation. We validate the proposed approach using an FHE prototype and COMSOL Multiphysics simulations.**

***Index Terms*—Flexible hybrid electronics, test, COMSOL Multiphysics, stress, integer linear programming**

I. Introduction

Flexible electronics, including silicon wafer on plastic substrates, have been around since the 1960s. They have proliferated into the marketplace in recent years with roll-to-roll fabrication of a Si:H solar cells on flexible steel and organic polymer substrate [1]. They can enables a variety of energy harvesting and flexible display solutions [2][3]. However, the performance of flexible devices is still not up to par with performance of integrated circuit components, thus preventing their use in high performance devices.

Flexible hybrid electronics (FHE) is emerging as a promising solution to combine the benefits of printed electronics and silicon technology [4][5]. FHE has many high-impact potential areas, such as wearable applications, health monitoring, and soft robotics [6][7][8][9], due to its physical advantages, which include light weight and the ability conform to different shapes by bending and stretching.

To ensure specified functionality under various bending and twisting conditions, FHE devices impose new design, test, and design automation challenges [5][10]. For example, bending can reduce the maximum power generated by a photovoltaic cell by more than 50% [11] and increase the mechanical stress [12]. Similarly, it can damage the connection between the pins of the rigid ICs and flexible substrate. To account for this effect, the specifications of the design need to be augmented into a new dimension that defines the flexibility of the substrate. This specification needs to include worst case bending and twisting conditions. In order to take this requirement into account during the design phase, a new metric, called *flexibility* has been defined and constraint-based optimization algorithms have been developed for designing FHE boards [13].

FHE devices pose additional burdens on the board test process as well. Traditionally, rigid boards are tested through the application of pre-defined test patterns with the help of a tester along with on-board and on-chip structures, such as the JTAG interface [14][15]. During testing, the boards are kept on a flat surface without any mechanical stress. Unfortunately, this form of testing is not adequate for FHE devices for two reasons. First, the characteristics of traces and solder joints on FHE substrates change when the devices are bent or twisted [16][17]. Electromechanical simulations can help determine the worst case bending/twisting conditions and predict the stress induced by the mechanical stimulus. However, it is not possible to fully correlate the electrical parameters measured in neutral and bent/twisted states due to process variations. Second, mechanical stress can cause fractures after manufacture, which will make the devices fail only after bending and twisting [18][19]. Due to these two issues, FHE devices must be tested under bending conditions, which induce different levels of stress on different locations of the FHE boards. Therefore, a thorough test procedure needs to apply many types of mechanical stress to FHE devices to cover worst case scenarios [17][18][19].

The application of mechanical stress on the FHE devices can be accomplished via a specialized test set-up [20] where one side of the FHE board is fixed and a force is applied to the other side. From this perspective, the fixed location of the board and the location where the force is applied can take on many values. For instance, one edge of the board can be fixed at multiple locations, spread out by centimeters, where the force can be applied from any other edge, and location. Figure 1 shows this concept for a simplified board layout with 12 solder joints, and 3 traces, each of which can be a fault. Point A is chosen as the fixed location, and Point B is chosen as the moving location. Points AB generate a mechanical stress pattern with the faults distributed along the cantilever formed by these two points. When the force, F, is applied,

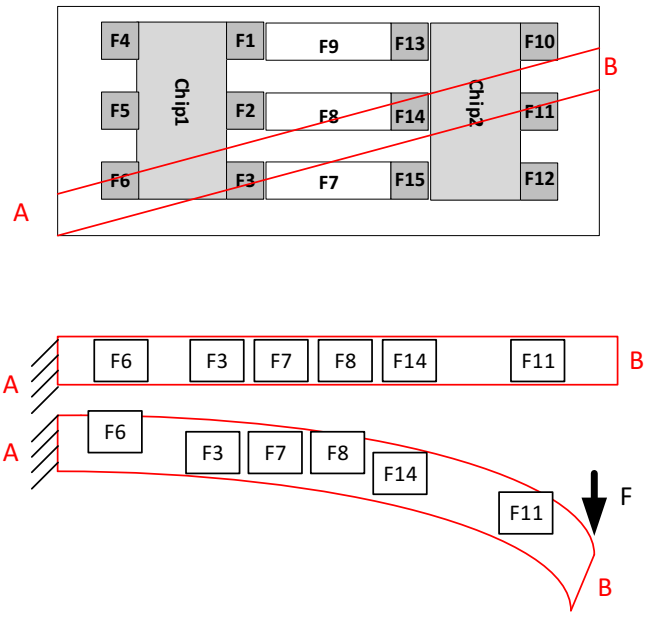

Fig. 1. Illustrative example of an FHE board with rigid components, solder joints, and traces generating potential parametric and catastrophic faults along the chosen mechanical stress pattern AB.

the faults will be stressed to varying degrees depending on their location on the cantilever [5]. The choice of the fixed and moving positions (AB) results in $O(n^2)$ potential stress patterns, where n is the number of distinct positions along the edges of the board. Application of multiple mechanical stress patterns necessitates re-positioning the board, with a large test time overhead (hundreds of milliseconds to seconds), thereby increasing test cost and reducing the throughput. Thus, methodologies are needed to reduce this mechanical test overhead for FHE boards as much as possible to keep the overall product cost at a manageable level.

This paper addresses the problem of optimizing the mechanical stress patterns for FHE boards such that all potential fault locations are stressed adequately during testing to ensure proper operation in the field. Our goal is the reduce the number of bending and twisting conditions (defined by one fixed and one moving location) to eliminate the unnecessary combinations. We observe that each trace or solder joint will reside on the path of multiple mechanical stress patterns. Hence, there is considerable redundancy in mechanical stress application when all n^2 combinations are taken into account. We define the minimum stress conditions based on the specification of bending and twisting curvature as dictated by the application. We determine the maximum stress in each potential fault location based on this curvature and optimize mechanical stress patterns to cover all fault locations with this level of stress. We conduct our experiments on a prototype FHE [5] designed as a device wearable around the wrist. We use the COMSOL multiphysics environment to evaluate the stress conditions for each fault location and integer linear programming (ILP) to optimize the stress patterns.

II. Related Work

Flexible electronics refer to integrated circuits implemented on bendable, rollable, conformable, or elastic substrates [21][22], while the term *flexible hybrid electronics* implies integration with rigid ICs [4][23]. This integration aims at combining the physical advantages of flexible electronics with the superior performance and power consumption of traditional silicon technology [5].

Flexible devices introduce new challenges to design automation and test due to the need to apply mechanical stress during testing [13][16]. Mechanical stress is needed to ensure proper operation in the field and can be in the form of bending and twisting [18]. In several recent studies, flexible devices are tested under three types of mechanical stress, convex and concave radius of curvature, and torsional stress [18][24]. It is shown that the parameters of a flexible OPAMP change significantly under various stress conditions, necessitating multiple stress test patterns.

In [25], a mechanical stress unit is designed for electrical characterization under mechanical stress. This unit can bend or twist the FHE in multiple ways. An apparatus that can bend the FHE device along its length or width is presented in [26][17]. The board is placed between two parallel plates, where one plate is moving to enable the bending operation. The movable plate is moved with a speed of 50 mm/s to enable bending. Electrical characteristics of the traces on the board show significant shift under mechanical stress. In [19], a test mechanism is generated to duplicate an application-specific operation condition, i.e. bending of the arm. The part is placed on this apparatus and electrical test are conducted before, during, and after bending. The experiments show significant shifts in trace and solder characteristics during bending. Majority of these shifts recover in the flat position while a subset of traces and solder joints experience irreversible damage. In [27], a 4-point stress testing mechanism is developed to bend and twist the board in multiple axes. Again, the authors report change in electrical characteristics of the traces and solder joints.

Prior and ongoing work in the testing of FHE devices clearly show the need for mechanical stress testing. However, application of all possible stress patterns would be costly in terms of test time and would limit throughput. The goal of this paper is to determine an optimum set of critical mechanical stress patterns to exercise the board as specified.

III. Methodology

FHE devices need to be mechanically stressed during test process in order to ensure their correct operation in the field. This stress that results from bending or twisting can be modeled in general by fixing a point along one of the edges of the FHE board, and applying a force at another location, creating a curvature pattern along the beam formed by the two ends. We use COMSOL, a multi-physics simulator, to evaluate the stress along the beam at various locations. During testing, we stress the solder joints as well as traces to make sure their electrical characteristics are up to specifications and to detect any latent fractures. Thus, each solder joint or trace is

a potential fault, either parametric or catastrophic, that needs to be tested, as illustrated in Figure 1. The faults are stressed to different levels depending on their location along each beam.

The flow of the proposed optimization approach is outlined in Figure 2. We start with the FHE layout as well as the bending/twisting specification, which is expressed as a radius of curvature (ROC) [28]. We also set a stress multiplier, α, which is the allowed *overstress* amount. The minimum value of α is 1, and the maximum value determined is experimentally. We build the FHE layout in COMSOL multiphysics simulator and label potential fault locations. We simulate various bending/twisting conditions (by bending the device between two points, AB) to determine a critical spacing parameter, k, where the stress is almost identical through vertical dimension with respect to the line formed by AB. Next, we choose exhaustive mechanical stress patterns through dividing each edge by this increment, k, forming potential end points for mechanical stress. Thus, if the FHE dimensions are $W \times L$, there are $2(W+L)/k$ potential fixed (A) and moving (B) positions for the entire FHE board. Each combination AB forms a cantilever for mechanical stress application. Then, we determine the displacement amount, D, that provides the specified ROC for each cantilever AB. Each cantilever AB

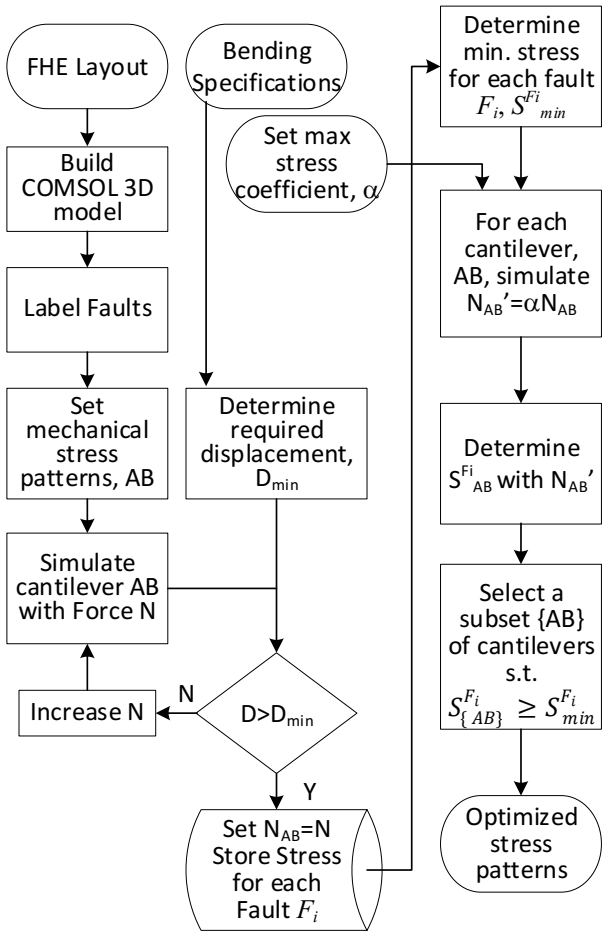

Fig. 2. Flow of the proposed mechanical stress optimization methodology

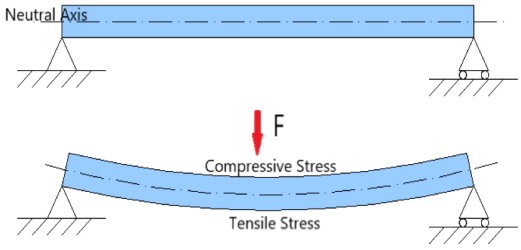

Fig. 3. Bending Stress

is simulated with progressively increasing force to meet this displacement requirement. Once the necessary force is found, it is stored along with the stress it causes at each fault location.

Next, we analyze the stresses at fault locations. For each fault, F_i, we determine the minimum required stress, $S^{F_i}_{min}$ as the maximum stress that fault experiences under any of the cantilevers. We form a new matrix where the force is increased by its stress multiplier, α and the new stress amounts are determined. Our optimization goal after this step is to determine a minimum set of chosen stress patterns, $\{AB\}$, such that each fault undergoes the required minimum stress.

A. Stress in Cantilever

Normal stress is a stress that when a member is loaded by an axial force, which is typically expressed in terms of "N/m^2"[29] equation as shown in:

$$\sigma = \frac{F}{A} \tag{1}$$

where F is the applied force and A is the cross-sectional area.

Bending stress is a more specific type of normal stress. Adding a load on a beam, top fibers undergo a compressive stress, the bottom fibers undergo a tensile stress. On the neutral axis, the stress is zero, as shown in Figure 3[29]. We can express the stress along a cantilever as:

$$\sigma_b = \frac{My}{I_c} \tag{2}$$

where M is the bending beam moment, I_c is moment of inertia of the beams cross section, and y is vertical distance away from the neutral axis. For a more realistic rectangle model, as shown in Figure 4, the moment of inertia in two dimensions, x-axis, and y-axis, can be expressed as in Equation 3:

$$I_{cx} = \frac{bh^3}{12} \quad I_{cy} = \frac{hb^3}{12} \tag{3}$$

Equation 3 can be used to pre-select a subset of cantilevers where stress at potential fault locations are maximized. Since relying on first-level approximations is not adequate, we also use the COMSOL multiphysics simulator to determine the actual stress exerted by a given stress pattern AB.

B. Radius of Curvature and Displacement

Each application has its own flexibility specifications. For instance, a device designed to be worn on the wrist has different bending requirements than a device designed to be

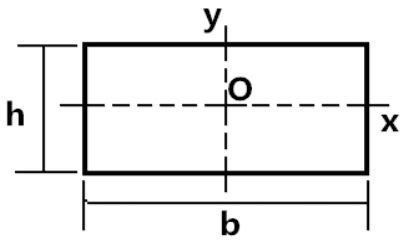

Fig. 4. The rectangle model

worn on the arm. Similarly for a wrist-wearable device, the bending requirements depends on whether it is intended for adults, children, or infants. Based on the application needs, one can determine the worst case bending scenario. Along the same example, a wearable device for infants (e.g. used in hospitals for tracing) has a much more stringent bending requirement, where a radius of curvature can be determined based on the average size of an infant. The ROC therefore is a specification dictated by the application. Based on the specified ROC, we can determine the simulation parameters. This process is illustrated in Figure 5. The flexible device is bent to fit an average adult wrist with a given radius, R.

In our simulation platform, we need to fix one end of the cantilever and apply force on the other end, causing a displacement. This displacement amount needs to match the given ROC requirements. This is illustrated in Figure 6, where the points AB represent the two ends of the cantilever under no stress conditions and points AE represent the same two ends under the stress conditions. D represents the displacement of cantilever's moving end, and R represents the radius of curvature. The slice of the circle with end points AE have the same length, L, as the cantilever, which results in an central angle, θ. Thus, for a given cantilever with length, L, and the radius of curvature specification, R, we can determine the displacement, D, using Equation 4. The required displacement amount varies with the length of each cantilever.

$$D = R(1 - \cos\frac{L}{R}) \tag{4}$$

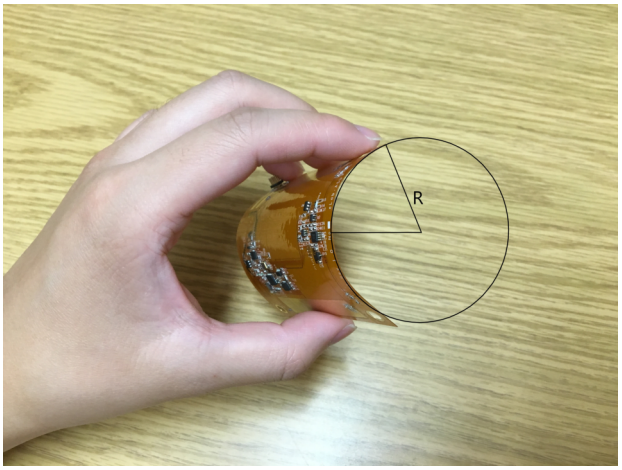

Fig. 5. Bending the FHE based on a given radius of curvature

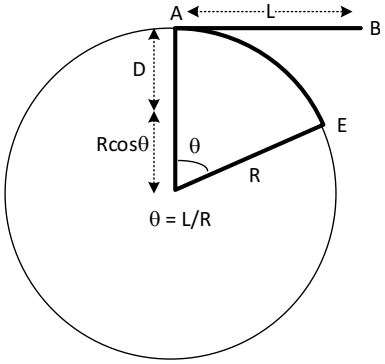

Fig. 6. Determining required displacement, D, from the given bending specifications as radius of curvature, R, and the cantilever length, L.

C. Optimization Algorithm

After simulating each cantilever with the required displacement amount in COMSOL, we determine the stress experienced by each fault. For a given fault, there may be multiple cantilevers that stress it to various degrees. Since we are trying to meet a maximum ROC requirement, we need to ensure that each fault undergoes the maximum stress amount taken over all cantilevers. That will be our minimum stress requirement.

We can move forward with our optimization with the minimum stress requirement. However, this may result in the selection of all cantilevers. Thus, we provide a margin to allow faults to be covered with multiple cantilevers. We define a multiplier factor, $\alpha > 1$, to stress faults beyond their required minimum. This parameter α is determined experimentally from initial characterization samples. By increasing the force applied by a factor of α, we ensure that fewer cantilevers are selected for stress. We use Integer Linear Programming (ILP) formulation for the optimal selection of cantilevers.

In ILP, we first define a coverage matrix denoted by A. In our formulation, A is an $N \times M$ matrix, where N is the number of faults, and M is the number of simulated cantilevers. If cantilever j stresses a given fault F_i to the minimum required amount $S_{min}^{F_i}$, it is said to cover that fault. Hence, the corresponding entry in A is set to 1, while all the other entries of A in that row remain as 0. We also define three additional matrices as follows. b is $N \times 1$ matrix and c is an $M \times 1$ matrix with all entries equal to 1. Finally, the entries of the $M \times 1$ matrix x are set to either 0 or 1 by the optimization process to minimize $c^T x$ subject to the following constraints:

$$\min\ c^{\mathrm{T}}\mathrm{x}\ ,\ \text{subject}\ \begin{cases} \mathrm{Ax} \geq \mathrm{b} \\ x_i \in 0{,}1 \end{cases}$$

IV. Results and Discussion

We illustrate the simulation setup and the optimization process through an FHE prototype built at ASU [5]. The dimension of the board is 3cm×6cm. As shown in Figure 7, the prototype contains 12 rigid chips and various interconnects between them. Table I shows the location and parameters of

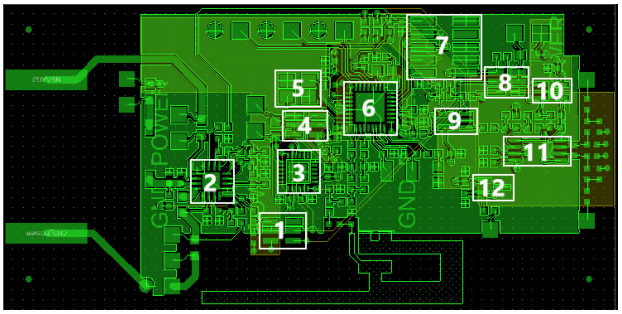

Fig. 7. Prototype FHE Layout where the marked numbers are the rigid chip locations

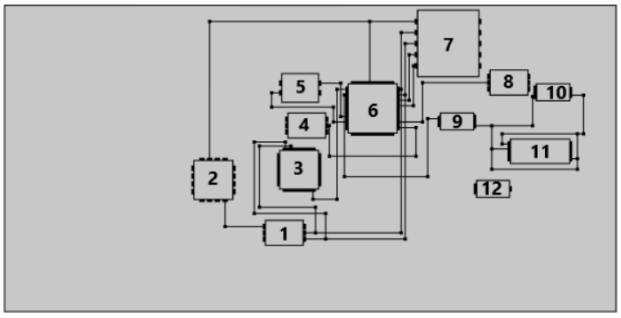

Fig. 8. Pins and Wires on Substrate

the 12 chips on the prototype. We construct a 3D model of the layout in COMSOL (as illustrated in two dimensions in Figure 8) and simulate this layout under multiple bending/twisting combinations. This process is illustrated in Figure 9 for two mechanical stress patterns. We observe that stress occurs mostly along the cantilever formed by the endpoints of the stress pattern. We also observe that the layout can be divided into grids where the stress is nearly identical. Based on this observation, we determine a minimum spacing to form the cantilevers. We set this spacing to where stress along the *width* of the cantilever is nearly identical (less than 1% difference in stress). This enables us to determine the potential mechanical stress patterns (AB) to exhaustively explore the entire layout. Through simulations, we find the critical spacing to be 1.5cm.

TABLE I
ALL BLOCKS PARAMETERS(UNIT: MM)

Block	Width	Depth	Height	X	Y	Z
Substrate	30	60	0.3	0	0	0
1	2.45	3.7	0.6	6.5	30.7	0.3
2	3.8	3.8	0.6	11	37.6	0.3
3	3.8	3.8	0.6	12	29.2	0.3
4	2.45	3.7	0.6	17	28.5	0.3
5	2.8	3.6	0.6	20.5	29.2	0.3
6	4.8	4.8	0.6	17.5	21.5	0.3
7	6.5	6	0.6	23	13.5	0.3
8	2.45	3.7	0.6	21.2	8.7	0.3
9	1.65	3.25	0.6	17.8	14	0.3
10	1.65	3.25	0.6	20.65	4.6	0.3
11	2.4	5.8	0.6	14.5	4.6	0.3
12	1.65	3.2	0.6	11.2	10.5	0.3

Before simulating each cantilever, we also observe that some of the stress patterns do not exert sufficient stress on any of the fault locations. We use Equation 2 and Equation 3 to eliminate cantilevers that will not exert sufficient stress on any of the fault locations. Next, we construct the 3D model of each viable cantilever, which includes solder joints and traces along the cantilever, to simulate under varying applied force.

Analysis of the prototype layout leads to 192 faults, including all the traces and solder joints. In this work, we assign one fault for each vertical and horizontal segment. If the trace is long, it can be divided into more segments, resulting in more faults in the layout. We set the required radius of curvature as 15cm. Setting the cantilever width 1.5cm generates 84 potential cantilevers (excluding fixed/movable pairs on the same edge). Majority of these cantilevers do not stress any component or generate stress conditions that are too weak.

After the initial analysis of stress using Equations 2 and 3, we determine 27 cantilevers that stress the fault locations. Note that application of all 27 mechanical stress patterns would result in unreasonably long test time as the device needs to be re-positioned between subsequent stress patterns. From the given ROC requirement, and using Equation 4, we determine the required displacement amount for each cantilever. We then form the 3D COMSOL model of each cantilever and simulate the stress under various force conditions. We find the force needed to obtain the required displacement amount. For each cantilever and fault location, we determine the mechanical stress under this necessary force. Next, we use the stress multiplier α to increase the force for each cantilever. The coverage matrix, A is determined based on this new force amount. Then, we use our ILP formulation to select the subset of cantilevers that provide the necessary stress.

Table II summarizes the results on the experimental device. When α is 1, we only apply the necessary amount of force based on the ROC specifications, severely limiting the number of cantilevers that can provide this level of stress. 19 out of 27 cantilevers are selected under this condition, resulting in roughly 30% reduction in the number of mechanical stress patterns. As α increases, more cantilevers cover each fault, and the number of selected stress patterns decreases accordingly.

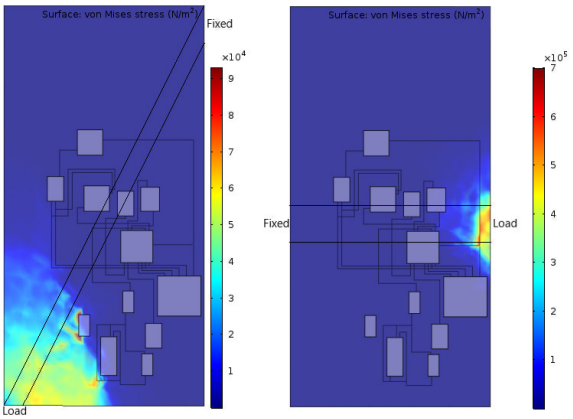

Fig. 9. Stress on the entire board layout for two mechanical stress patterns.

TABLE II
NUMBER OF SELECTED MECHANICAL STRESS PATTERNS BASED ON STRESS MULTIPLIER

α	1	5	10	50	100
Cantilevers	19	14	13	10	10

V. CONCLUSIONS

FHE devices are expected to proliferate into the consumer market with explosive growth. However, testing of FHE devices introduces the additional complexity of needing to use mechanical stress patterns in the form of bending and twisting. Since electrical characteristics may shift during mechanical stress and traces and solder joints can fracture, it is necessary to apply multiple stress patterns to ensure that all traces and joints are tested under worse case conditions. This paper presented a methodology to enable selection of an optimum set of mechanical stress patterns to cover all potential fault locations and exert the required mechanical stress as dictated by the application. The proposed methodology is validated using an FHE prototype and COMSOL simulations.

Acknowledgment: This work was supported in part by NSF Grant SHF-1617562, NSF CAREER Award CNS-1651624, Semiconductor Research Corporation under task ID 2712.003, and DARPA Young Faculty Award (YFA) Grant D14AP00068.

REFERENCES

[1] W. S. Wong and A. Salleo, *Flexible Electronics: Materials and Applications*. Boston: Springer US, 2009, ch. 1.

[2] F. R. Fan, W. Tang, and Z. L. Wang, "Flexible Nanogenerators for Energy Harvesting and Self-Powered Electronics," *Advanced Materials*, vol. 28, no. 22, pp. 4283–4305, 2016.

[3] "All-Organic Active Matrix Flexible Display," *Applied Physics Letters*, vol. 88, no. 8, p. 083502, 2006.

[4] J. Sheats, "Truly Wearable Electronics," in *Proc. of FlexTech Alliance Workshop: Flexible Hybrid Electronics Challenges and Solutions*, July 2014.

[5] U. Gupta, J. Park, H. Joshi, and U. Y. Ogras, "Flexibility-Aware System-on-Polymer (SoP): Concept to Prototype," *IEEE Trans. Multi-Scale Comput. Syst.*, vol. 3, no. 1, pp. 36–49, 2017.

[6] G. Bhat, R. Deb, V. V. Chaurasia, H. Shill, and U. Y. Ogras, "Online Human Activity Recognition using Low-Power Wearable Devices," in *Proc. Int. Conf. on Comput.-Aided Design*, 2018, pp. 72:1–72:8.

[7] G. Bhat, R. Deb, and U. Y. Ogras, "OpenHealth: Open Source Platform for Wearable Health Monitoring," *IEEE Design & Test of Computers*, 2019, Available [Online]: https://elab.engineering.asu.edu/wp-content/uploads/2019/02/OpenHealth_preprint.pdf.

[8] M. Patel and J. Wang, "Applications, Challenges, and Prospective in Emerging Body Area Networking Technologies," *IEEE Wireless Commun.*, vol. 17, no. 1, pp. 80–88, 2010.

[9] N. Lu and D.-H. Kim, "Flexible and Stretchable Electronics Paving the Way for Soft Robotics," *Soft Robotics*, vol. 1, no. 1, pp. 53–62, 2014.

[10] K.-T. Cheng and T.-C. Huang, "Design, Analysis, and Test of Low-Power and Reliable Flexible Electronics," in *Proc. VLSI Test Symp. (VTS)*, 2010, p. 82.

[11] J. Park *et al.*, "Flexible PV-cell Modeling for Energy Harvesting in Wearable IoT Applications," *ACM Trans. Embedd. Comput. Syst. (TECS)*, vol. 16, no. 5s, p. 156, 2017.

[12] N. Bednar, A. Caviasca, P. Sevela, N. Severino, and N. Adamovic, "Modelling of Flexible Thin-Film Modules for Building and Product Integrated Photovoltaics," *Solar Energy Materials and Solar Cells*, vol. 181, pp. 38–45, 2018.

[13] G. Bhat *et al.*, "Multi-Objective Design Optimization for Flexible Hybrid Electronics," in *Proc. Int. Conf. on. Comput.-Aided Des. (ICCAD)*, 2016, pp. 1–8.

[14] C. W. Yau and N. Jarwala, "A Unified Theory for Designing Optimal Test Generation and Diagnosis Algorithms for Board Interconnects," in *Proc. Int. Test Conf.*, 1989, pp. 71–77.

[15] B. Van Ngo, P. Law, and A. Sparks, "Use of JTAG Boundary-Scan for Testing Electronic Circuit Boards and Systems," in *IEEE AUTOTESTCON*, 2008, pp. 17–22.

[16] T.-C. Huang, J. Marsh, S. H. Goodwin, and D. S. Temple, "Innovative practices on design test for flexible hybrid electronics," in *2018 IEEE 36th VLSI Test Symposium*, 2018, p. 1.

[17] R. Chen, J. Chow, C. Taylor, J. Meth, and S. Sitaraman, "Adaptive Curvature Flexure Test to Assess Flexible Electronic Systems," in *Proc. IEEE Electronic Components and Tech. Conf.*, 2018, pp. 236–242.

[18] R. L. Chaney, D. R. Hackler, D. G. Wilson, and B. N. Meek, "Physically Flexible High Performance Single Crystal CMOS Integrated with Printed Electronics," in *Proc. IEEE Work. On Microelectronics And Electron Devices (WMED)*, 2014, pp. 1–4.

[19] P. Lall, J. Narangaparambil, A. Abrol, B. Leever, and J. Marsh, "Development of Test Protocols for the Flexible Substrates in Wearable Applications," in *Proc. IEEE Intersociety Conf. on Thermal and Thermomechanical Phenomena in Electron. Syst.*, 2018, pp. 1120–1127.

[20] W. C. Young and R. G. Budynas, *Roark's Formulas for Stress and Strain*, 7th ed. New York, London: McGraw-Hill, 2002, ch. 8.

[21] T.-C. Huang, J.-L. Huang, and K.-T. Cheng, "Robust Circuit Design for Flexible Electronics," *IEEE Design and Test of Computers*, vol. 28, no. 6, pp. 8–15, 2011.

[22] A. Nathan *et al.*, "Flexible Electronics: The Next Ubiquitous Platform," *Proc. of IEEE*, vol. 100, no. Special Centennial Issue, pp. 1486–1517, 2012.

[23] R. L. Chaney, D. R. Hackler, D. G. Wilson, and B. N. Meek, "FleX™ Silicon-on-Polymer™: Flexible (Pliable) ICs from Commercial Foundry Processes," in *Proc. of GOMACTech (Government Microcircuit Applications and Critical Technology) Conf.*, March 2013.

[24] D. E. Leber, B. N. Meek, S. D. Leija, D. G. Wilson, R. L. Chaney, and D. R. Hackler, "Electromechanical Reliability Testing of Flexible Hybrid Electronics Incorporating FleX Silicon-on-Polymer ICs," in *Proc. IEEE Works. on Microelectronics and Electron Devices (WMED)*, 2016, pp. 1–4.

[25] B.-J. Wen and T.-S. Liu, "Bending-Characteristic Measurement of Flexible Electronics by Using Fast Optimal Sliding Mode Control Method," in *Procc of SICE Annual Conference*, 2010, pp. 1872–1874.

[26] S. Grego, J. Lewis, E. Vick, and D. Temple, "Development and Evaluation of Bend-Testing Techniques for Flexible-Display Applications," *J. of the Society for Information Display*, vol. 13, no. 7, pp. 575–581, 2005.

[27] D. van den Ende1 *et al.*, "High Curvature Bending Characterization of Ultra-Thin Chips and Chip-on-Foil Assemblies," in *European Microelectronics Packaging Conf. (EMPC)*, 2013, pp. 1–6.

[28] R. C. Stephens, *Strength of Materials: Theory and Examples*. London, England: Edward Arnold, 1971, ch. 3.

[29] J. Parker, "Normal Stress, Bending Stress, & Shear Stress," 2010, http://www.strucalc.com/normal-stress-bending-stress-shear-stress.