Sputtered Aluminum Oxide and p^+ Amorphous Silicon Back-Contact for Improved Hole Extraction in Polycrystalline $CdSe_xTe_{1-x}$ and CdTe Photovoltaics

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***Abstract* — A thin layer of Al_2O_3 at the back of $CdSe_xTe_{1-x}$/CdTe devices is shown to passivate the back interface and drastically improve surface recombination lifetimes and photoluminescent response. Despite this, such devices do not show an improvement in open-circuit voltage (V_{OC}.) Adding a p^+ amorphous silicon layer behind the Al_2O_3 bends the conduction band upward, reducing the barrier to hole extraction and improving collection. Further optimization of the Al_2O_3, amorphous silicon (a-Si), and indium-doped tin oxide (ITO) layers, as well as their interaction with the $CdCl_2$ passivation process, are necessary to translate these electro-optical improvements into gains in voltage.**

***Index Terms* — CdTe, Al_2O_3, a-Si, passivating oxides, photovoltaic cells, charge carrier lifetime**

I. Introduction

Thin film CdTe photovoltaics have advanced significantly during the past several years, becoming the most widespread thin film technology for photovoltaic energy generation as well as a cost-effective solution for utility scale electrical generation. With improvements in fabrication processes, research scale small devices have recorded efficiencies as high as 22.1% [1] while commercial modules have achieved 18.6% [2]. Recent developments in module technology continue to drive down the cost of CdTe-generated electricity. Utility scale solar costs are projected to fall as low as ¢1/kWh in the near future while the current lowest cost of utility scale electricity reported with CdTe photovoltaics is ¢3.8/kWh [3].

While CdTe technology has advanced rapidly, there are still challenges to be overcome. Historically CdTe has been plagued by a large voltage deficit. The V_{OC} in many devices range from 820-860 mV as opposed to the 1.2 V that is theoretically possible [4]. The goal of this work is to adapt the passivated contact technology which has become prominent in the best silicon-based devices to reduce the voltage deficit found in CdTe devices [5]. The Al_2O_3, having a large bandgap of approximately 7 eV [6], creates a large barrier to both electrons and holes when it is deposited on 1.5 eV bandgap CdTe. However, when highly-doped a-Si:H is deposited behind a thin layer of Al_2O_3, it causes upward band bending that can allow hole extraction while maintaining the barrier to electrons, and thus should reduce interface recombination, increasing the carrier lifetime, and ultimately the V_{OC}. In oxide-passivated silicon devices, it has been shown that the ability to extract holes is highly dependent upon the oxide thickness, with an optimal thickness of ~1.3 nm. This thickness provides the necessary barrier to electrons while remaining thin enough to allow hole transport through quantum tunneling [7].

Double heterostructures with Al_2O_3 and $CdSe_xTe_{1-x}$ have recently been shown to produce carrier lifetimes >400 ns, several orders of magnitude greater than the typical lifetimes found in CdTe [8]. Additionally, using Al_2O_3 only at the back of an otherwise typical MZO/$CdSe_xTe_{1-x}$/CdTe device has shown lifetimes increased from several nanoseconds to several hundred nanoseconds. Photoluminescence experiments further show an increase in photoluminescent intensity of several orders of magnitude when a thin layer of Al_2O_3 is deposited at the back. Despite these improvements, these structures do not result in a higher V_{OC}. The presence of a p^+ layer at the back

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enables hole extraction, and thus could be expected to create an improvement in V_{OC}. Arizona State University has recently demonstrated a monocrystalline CdTe device with an open-circuit voltage of greater than 1V and efficiency greater than 17% using a MgCdTe barrier layer and passivated a-SiC_y:H hole-selective contact [9].

In this work, a thin layer of aluminum oxide, followed by a layer of highly doped amorphous silicon were deposited as a passivating oxide and hole-contact behind $CdSe_xTe_{1-x}$/CdTe films with the intent of improving the implied V_{OC} and ultimately the measured V_{OC} of these devices.

II. Experimental Details

The devices used in the study were deposited on NSG TEC 10 soda lime glass coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). A 100 nm $Mg_xZn_{1-x}O$ (MZO) buffer layer was deposited using RF sputter deposition with a 4-inch diameter magnetron at 140 W. $CdSe_xTe_{1-x}$ films were sublimated using an optimized deposition process followed by sublimation of the CdTe layer. This study used both a 20% and 40% CdSe composition in the $CdSe_xTe_{1-x}$ source material and as-deposited films had a band-gap of ~1.40-1.42 eV from transmission measurements and Tauc plot. The $CdSe_xT_{1-x}$ vapor source was heated to 575ºC and films of 1 µm thickness were deposited. After deposition of $CdSe_xTe_{1-x}$, the sample was moved to the CdTe sublimation vapor source without breaking vacuum and a film ~2.7 µm thick was deposited. The CdTe sublimation source temperature was maintained at 555ºC. All samples were fabricated in the superstrate configuration. The bandgap of the film was graded from ~1.42 eV near the MZO/ $CdSe_xTe_{1-x}$ interface to 1.5 eV at the back due to Selenium diffusion into the CdTe as shown in [10]. After the deposition of the CdTe layer, the substrate was removed from vacuum and Al_2O_3 was deposited via magnetron sputtering with a 4-inch diameter planar magnetron. The sputtering was performed in a 5 mTorr Argon atmosphere with 8% Oxygen. RF power was maintained at 240 W. Al_2O_3 was deposited to a thickness of 2 nm for devices.

The samples were then shipped to Arizona State University for deposition of highly boron-doped (p-type) hydrogenated amorphous silicon (a-Si:H) and Indium Tin Oxide (ITO). The a-Si:H was deposited via PECVD at 250ºC at a pressure of 4 Torr and RF power of 100 W. Gas flows were 40 sccm of SiH_4, 197 sccm of H_2, and 18 sccm of 3% trimethylborane (TMB) diluted in H_2. The a-Si:H layer thickness was 8nm. A 70nm layer of ITO was then sputtered using a 90/10 In_2O_3/SnO_2 target. The sputtering process was performed at room temperature, 500 W (DC power), and 5.5 mTorr, which yielded a film with sheet resistance of 150 ohm/square. The samples were then shipped back to Colorado State University.

A dry $CdCl_2$ treatment was performed on the entire structure in a 40 mTorr nitrogen background. $CdCl_2$ is known to promote recrystallization and grain growth in the $CdSe_xTe_{1-x}$ and CdTe as well as the graded $CdSe_xT_{1-x}$ layer. The film stack was exposed to $CdCl_2$ vapor for 600 seconds at approximately 450ºC, followed by an anneal at 400ºC for 1500 seconds. After the $CdCl_2$ treatment, the films were rinsed with deionized water to remove residual $CdCl_2$ from the surface.

Thereafter, the films were heated to ~140ºC, and CuCl was deposited on the film surface for 120 seconds. This was followed by 240 seconds of annealing at 220ºC, both in a 40 mTorr nitrogen background. Two back electrode configurations were used. The back electrode for some devices was formed by spraying carbon and nickel paints in a polymer binder. Other devices received a 200 nm thick evaporated layer of silver in lieu of the carbon and nickel paint. Figure 1 shows a schematic of the full device structure with the carbon and nickel paint. The individual cells were delineated using a mask and bead blasting to fabricate 25 small scale devices on the substrate. The devices had an area of ~0.60 cm^2.

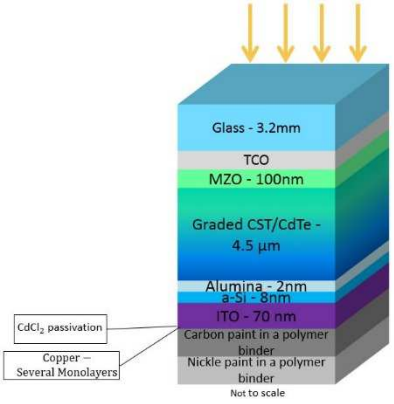

Fig. 1. Schematic of the $CdSe_xTe_{1-x}$/CdTe graded absorber device with a layer of Al_2O_3 and p^+ doped amorphous silicon (not to scale).

III. Results

Figure 2 shows large increases in photoluminescent response as additional back contact layers are added to the $CdSe_xTe_{1-x}$ devices. This data clearly shows that back-contact processing steps change defect properties through the absorber, including the front junction, where PL is excited and recorded. The addition of the Al_2O_3 results in an increase in PL from approximately 30k counts to more than 100k counts. This is followed by an even greater increase up to 400k counts with the addition of the a-Si:H, ITO and a silver back contact. Finally, when the device was annealed in air at 200°C for 10 minutes, the PL doubled again to more than 700k counts. Combined, the addition of Al_2O_3, a-Si:H ITO, and Ag with an anneal increased the PL response by more than an order of magnitude, from the baseline $CdSe_xTe_{1-x}$ device.

In order for alumina to be successfully incorporated into a device structure, it is expected that it will need to be kept extremely thin, likely less than 2nm to allow for quantum tunneling. However, in order to better understand the

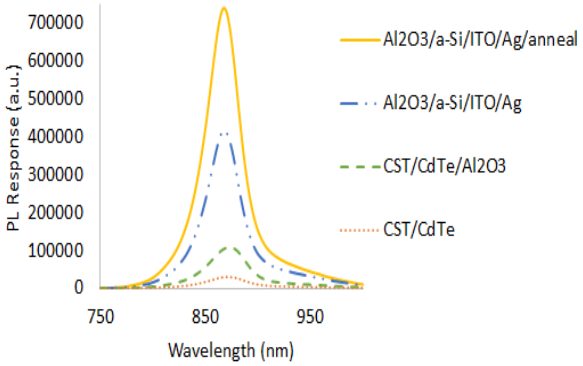

Fig. 2. PL response of devices with Al_2O_3 and Al_2O_3/a-Si/ITO/Ag at the back compared to a reference device with C/Ni back contact. PL was measured with 520 nm excitation from the glass/junction side. Laser power was 15mW and beam size was 7mm^2.

mechanics behind the passivation, Al_2O_3 films of various thicknesses were deposited. It was found that when only Al_2O_3 was deposited behind the CdTe, the PL response grew as the Al_2O_3 became thicker, as seen in Figure 3. Additionally, no peak-shift was noted as the alumina became thicker, which indicates that the increased oxide thickness is not significantly affecting the amount of selenium diffusion from the $CdSe_xTe_{1-x}$ into the CdTe during the $CdCl_2$ treatment.

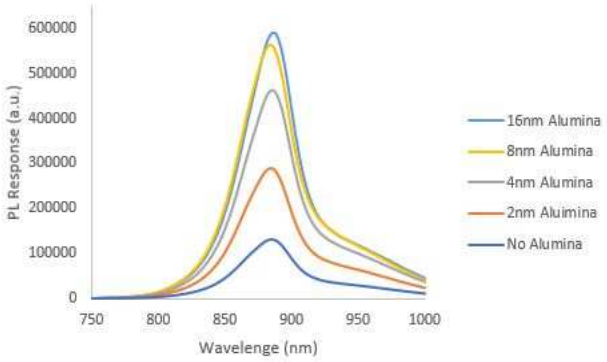

Fig. 3. PL Spectra for $CdSe_xTe_{1-x}$/CdTe devices with various thicknesses of Al_2O_3 deposited at the back

Although increasing the alumina thickness shows a dramatic increase in the photoluminescence when it is very thin, the marginal gain diminishes rapidly at alumina thicknesses greater than 4nm, as shown by the peak PL intensities in Figure 4. The increased photoluminescence is important because it serves as a key precursor to developing increased open circuit voltages in CdTe devices, as will be discussed shortly.

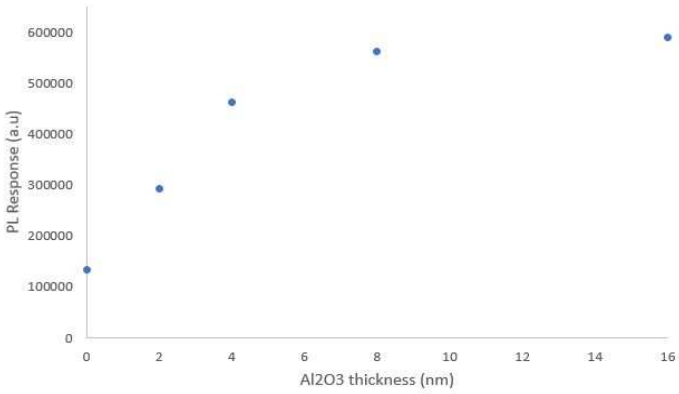

Fig. 4. PL intensity versus Al_2O_3 thickness

Similar to the substantial increase in steady state photoluminescence, Time-Resolved Photoluminescence (TRPL) measurements show that the addition of the alumina at the back surface greatly increases the carrier lifetime. Whereas a typical "baseline" $CdSe_xTe_{1-x}$/CdTe device fabricated during this study has measured lifetimes from 10-30ns, devices with Al_2O_3 displayed carrier lifetimes of 150ns, as seen in Figure 5. The fact that the absorber structure and thicknesses were kept consistent throughout this study indicates that the alumina has a strong passivating effect at the back interface. These device lifetimes are amongst the highest measured for polycrystalline CdTe and are comparable to double-heterostructure lifetimes.

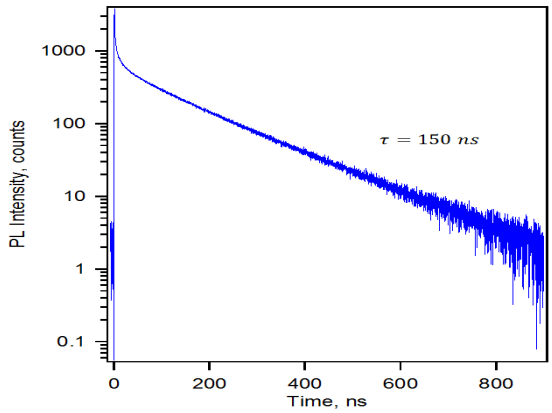

Fig. 5. TRPL decay curve for $CdSe_xTe_{1-x}$/CdTe/Al_2O_3/a-Si/ITO/Ag device. Two exponential fit shows a carrier lifetime of 150 ns

The $CdSe_xTe_{1-x}$/CdTe films used in this study were known to have a mean surface roughness of approximately 1µm. This substantial film roughness paired with the thin Al_2O_3 made it necessary to confirm that the alumina was forming a continuous and conformal layer when deposited via magnetron sputtering. Figure 6 shows the Scanning Electron Microscope (SEM) and Energy Dispersive Spectroscopy (EDS) images which shows that the aluminum and oxygen signals seem to be consistent across many separate grains, although it is difficult to determine

100% coverage due to the surface roughness causing shadowing effects that reduce the apparent signal, causing the dark spots in Figs 7B and 7C. The fact that the same dark patterns are seen on the elemental maps of Cd, Te, and Se, elements which are known to be present everywhere, indicates that the reduced signal is likely caused by shadowing and not a lack of alumina in these locations. These were test structures fabricated specifically for investigating the conformality of the Al_2O_3 layer, and as such did not have the additional layers needed to create devices.

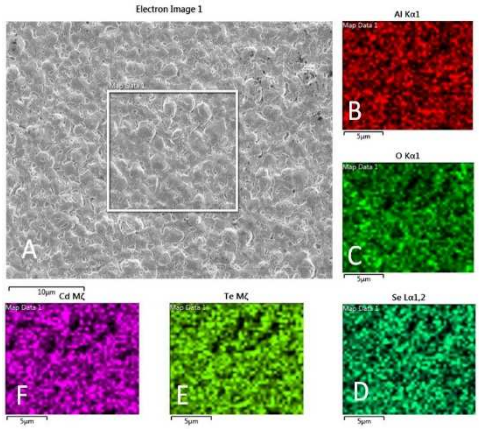

Fig. 6. (A) SEM electron image, (B, C, D, E, F) EDS scans for Aluminum, Oxygen, Selenium, Tellurium, and Cadmium, respectively.

Next, we describe solar cell device characteristics. Figure 7 shows the best performing device fabricated during this experiment compared to a typical CSU 18% $CdSe_xTe_{1-x}$/CdTe device with a Tellurium back contact and Carbon/Nickle paint back electrode. From this, it is clear that voltage and current extraction through the passivating oxide and subsequent layers remains problematic.

Although further optimization is required to maximize the performance of the Al_2O_3/a-Si/ITO structure, there is clear evidence that the addition of a highly doped a-Si layer is

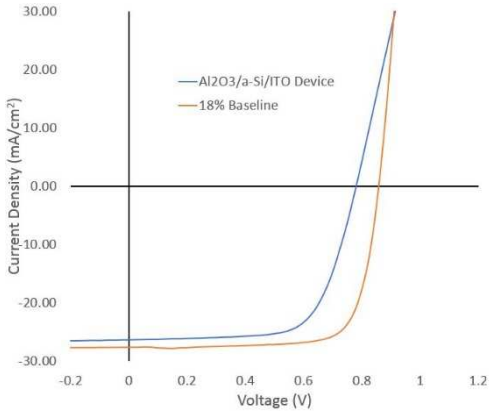

Fig. 7. J-V graph comparing the performance of a device with Al_2O_3, a-Si, and ITO to a typical 18% $CdSe_xTe_{1-x}$/CdTe device.

beneficial for reducing the barrier to carrier extraction through upward band bending. Figure 8 shows a comparison of a $CdSe_xTe_{1-x}$/CdTe device with Al_2O_3 and C/Ni at the back to a device with Al_2O_3, a-Si:H, and ITO before the C/Ni paint. Al_2O_3, being highly insulative, creates a large barrier to current extraction. But the addition of the a-Si:H and ITO allows for easier hole extraction by reducing the barrier and removing the "kink" in the J-V curve.

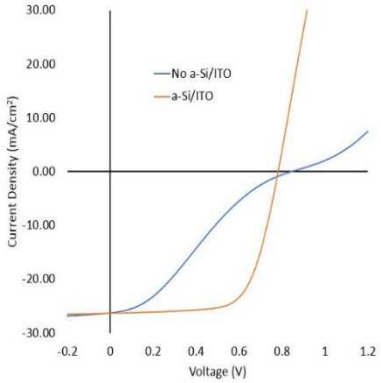

Fig. 8. J-V graph comparing the performance of a device with Al_2O_3, a-Si:H, ITO and C/Ni at the back against a device with only Al_2O_3 and C/Ni

IV. DISCUSSION

The significant increases in photoluminescent response and carrier lifetimes that occur with the addition of alumina and amorphous silicon leave little doubt that the back surface is being passivated. The specific mechanism at work, however, is still being debated. The two most prominent theories are that the rear interface is being passivated by a fixed negative charge in the alumina, or by the formation of a thin layer of TeO_2 between the CdTe and Al_2O_3. A fixed negative charge in the Al_2O_3 is the commonly cited explanation for surface passivation in silicon photovoltaic technologies [11] and has been suggested as a possible mechanism in CdTe technology by Kuciauskas *et al* [12]. Alternatively, Perkins *et al* have suggested that thin TeO_2 layers form between the CdTe and Al_2O_3 during the $CdCl_2$ treatment [13]. This TeO_2 may be providing chemical passivation by removing defects and preventing an abrupt CdTe/ Al_2O_3 interface.

Although the exact mechanism is still being studied, the massive increase in PL signal provides compelling evidence for interface passivation. Maximizing the photoluminescence of devices is a powerful strategy because of the positive correlation between PL response and the implied V_{OC} that the device can produce. Ross and Miller *et al* describe the relationship between the radiative efficiency and the potential voltage of a photovoltaic device [14]-[15] It is important to note that in the study covered in this manuscript, the integrated PL is used as a reasonable proxy for external radiative efficiency. As the PL increases, the implied voltage increases. The implied voltage indicates the open circuit voltage that could be achieved if there were perfectly selective contacts and no losses in the

electrodes. The measured V_{OC} being lower than the implied V_{OC} is a clear indication of non-selective contacts.

The PL response of the devices in these studies continually grew as alumina and then amorphous silicon were added to the back. It is therefore reasonable to assume that these devices might also produce a greater voltage at open circuit. The current-voltage plots presented here make it apparent that that is not yet the case. It is important to note that the PL correlates positively with the *implied* voltage, which may not necessarily manifest as a measured voltage if there are losses elsewhere in the system. The device structures presented in this study need further optimization to extract the increased potential voltage. Currently, the devices with the Al_2O_3/a-Si structure produce reduced current and voltage compared to the baseline. Several probable issues with the current design have been identified. First, the alumina thickness may need to be adjusted from the current thickness of 2 nm. Studies of passivating oxides on silicon indicate that the ideal thickness is between 1.3 and 1.7 nm, so it may be that the increased alumina thickness in this study exceeded the tunneling distance for many carriers, hindering their collection. Additional alumina deposition methods may need to be explored, as it may become difficult to sputter less than 2 nm layers while maintaining uniformity. Secondly, the best devices in this study occurred when the $CdCl_2$ treatment, which is necessary to passivate and recrystallize the CdTe, was performed after the alumina, a-Si, and ITO had been deposited. This is likely due to the need for either a layer of TeO_2 or Cl at the CdTe/Al_2O_3 interface. At this time, it is unknown what effect the $CdCl_2$ had on these subsequent layers, but it may have affected the doping levels in the a-Si, among other things. A reduction in the doping level of the a-Si would certainly affect the amount of band bending and the efficacy of hole extraction. Finally, CuCl is well known to both dope CdTe and improve the back contact, however the relatively high series resistance seen in these devices may indicate that the copper is not passing through the layers of Al_2O_3, a-Si, and ITO in sufficient quantities. The affect of CuCl on these layers is similarly unknown.

Finally, it should be noted that the devices that exhibited the highest PL responses were all fabricated with the silver back electrode, but the devices with highest photovoltaic conversion efficiency were all fabricated with a C-Ni paint back electrode. The ITO/Ag combination is a proven back contact/electrode in other technologies, so it is again likely that the $CdCl_2$ is interfering with this interface. Techniques for removing $CdCl_2$ residues that may be present at various interfaces are currently being investigated.

V. Conclusions

Although previous work has shown that adding a thin layer of sputtered Al_2O_3 behind the $CdSe_xTe_{1-x}$/CdTe absorber drastically improves the carrier lifetime, there has not currently been a commensurate improvement in the V_{OC}. The addition of a highly p-doped layer of amorphous silicon behind the Al_2O_3 reduces the back barrier and improves carrier collection. The significant increase in photoluminescence corresponds with an increase in the implied V_{OC} and should correspond with an increase in measured V_{OC} (assuming selective contacts). This increase in the measured V_{OC} was not observed in the samples in this study. and further optimization of the passivating oxide and subsequent layers is expected to improve the voltage beyond the typical values of 820-860 mV currently measured.

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