Effect of Process Temperature and Copper Doping on the Performance of ZnTe:Cu Back Contacts in CdTe Photovoltaics

Anna Kindvall, Amit Munshi, Tushar Shimpi, Adam Danielson, and Walajabad S. Sampath

Department of Mechanical Engineering, Colorado State University, Fort Collins, Colorado, 80523, United States

***Abstract* — CdTe photovoltaic devices with a ZnTe back contact have the potential to improve device performance and stability. After performing a sweep of ZnTe deposition and annealing temperatures, device performances were evaluated. Copper doping was performed after the ZnTe depositions by sublimating CuCl. Initial results indicate that ZnTe deposited and annealed for 20 minutes at 250°C improved device performance in terms of fill factor, J_{SC}, and V_{OC} as compared to other deposition temperatures. Copper doping also impacted device performance and a longer copper treatment on ZnTe led to a 17.6% device.**

***Index Terms* — ZnTe, Thin-film PV, Back contacts, CdTe**

I. Introduction

The demand for solar energy is ever growing. Over the past few years solar energy has been among the two fastest growing new electricity sources in the United States [1]. Thin-film solar production accounted for about 5% of the total solar market production in 2017 [2]. Cadmium telluride (CdTe) is one of several thin-film technologies. The appeal for CdTe solar is due to low cost, faster manufacturing and fastest energy payback time amongst all energy sources except wind with a small carbon footprint [3]. The leader in thin film CdTe module manufacturing is First Solar with over 17GW of modules installed world wide [4].

Continually improving photovoltaic efficiencies without an increase in manufacturing cost will help further lower the levelized cost of energy. CdTe has a nearly ideal bandgap for photovoltaic conversion of about 1.45eV. CdTe is a *p*-type semiconductor with valence band offset very close to that of zinc telluride (ZnTe). The advantage of the band alignment between CdTe and ZnTe is that it allows holes generated in CdTe to tunnel through ZnTe into the metal back contact without being impacted by the Schottky barrier [5].

Copper doping is quite complicated for use in CdTe solar cells since copper can diffuse into the CdTe device at modest temperatures. Copper can build up at the front interface of CdTe/buffer causing the device to shunt and the performance to drop [6]. In addition, Cu can exist as an interstitial defect that can be highly mobile and can act as an n-type defect [7]. Adding a ZnTe layer to the back contact can limit the copper diffusion, while also still keeping the CdTe/ZnTe interface copper rich [8]. In some studies a ZnTe layer at the back of CdTe is shown to form a more ohmic contact leading to improved device stability and reliability as compared to non ZnTe back contacts [9].

II. Methods

A. Device Fabrication Techniques

Devices were fabricated in superstrate configuration. Glass substrates were received from the manufacturer with a fluorine doped tin oxide layer as the transparent conductive oxide (TCO). The glass used in the following experiments was NSG TEC 10 soda lime glass. All glass substrates were cleaned and prepared before depositing the films.

Using an RF magnetron, 100 nm of an $Mg_xZn_{1-x}O$ (MZO) layer was deposited on the TCO. The MZO layer is a high resistivity transparent (HRT) layer currently used as a replacement for cadmium sulfide (CdS) as more current can be generated at lower wavelengths of light. After the deposition of the MZO layer, the sample is prepared for the advanced research deposition system (ARDS) where films are deposited via sublimation [10]. The sublimation sources were used to deposit $CdSe_xTe_{1-x}$ (CST) and CdTe. Layers of CST were generally 1.5 microns thick followed by 3-4 microns of CdTe. Devices fabricated for this experiment were ~4.8 microns thick. After the CdTe deposition, while still under vacuum the sample was indexed into the cadmium chloride ($CdCl_2$) source. The $CdCl_2$ passivation treatment significantly improved device performance and helps the CdTe

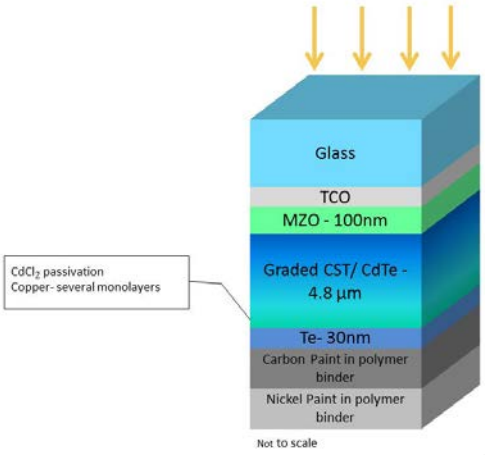

Fig. 1. Schematic of baseline device structure. (Not to scale)

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recrystallize while removing stacking faults [11]. After $CdCl_2$ passivation treatment, the substrate cooled under vacuum for 5 mins, before excess $CdCl_2$ on the sample was rinsed off with deionized water. Argon gas was then used to dry the sample off before the back contact deposition.

Following this, device structures deviated from a standard baseline device and samples with an additional thin layer of ZnTe. Baseline devices underwent a copper chloride (CuCl) treatment after the $CdCl_2$ rinse. The standard CuCl process included a preheat for 95 s at 330°C, CuCl deposition for 140 s at 190ºC, and an anneal for 240 s at 200°C. The copper (Cu) treatment acts as a *p*-type dopant for the back of the CdTe. After copper treatment, the baseline device received 30 nm of evaporated tellurium. The baseline devices were then finished by spraying carbon paint and nickel paint in a polymer binder to form the back electrode as seen in Fig. 1.

The ZnTe layer was deposited after the $CdCl_2$ passivation. Using an RF magnetron, the ZnTe layer was sputter deposited in argon at 18 mTorr. The power density applied to the ZnTe target was 7.4 kW/m^2. The sputter system had a built-in heater to be able to control temperatures. Each sample was heated to the deposition temperature and was held at that temperature for 15 minutes. Each deposition was calibrated to 100 nm as

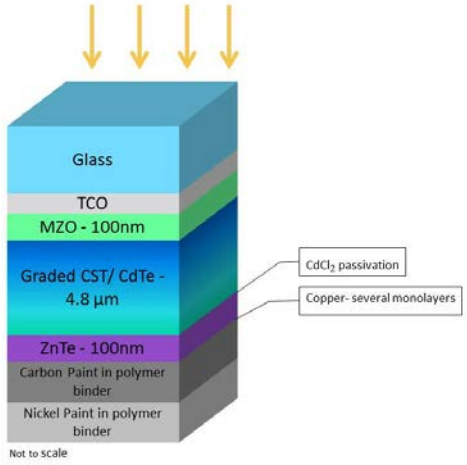

Fig. 2. Schematic of device structure with ZnTe back contact. (not to scale)

to view the impact of temperature on the sample. In terms of device performance, ZnTe has been found to be sensitive to deposition temperature and annealing temperature [12], [13]. In this study, ZnTe films were deposited at 350ºC, 250ºC, and 150°C. Once the 100 nm was deposited, samples were annealed for 20 minutes at the deposition temperature and pressure. After annealing, devices were cooled for two hours before removing the samples from vacuum. The ZnTe devices explored different copper treatment times, while maintaining the same copper process temperatures. After copper treatments, the ZnTe devices then were finished with the carbon and nickel paint in a polymer binder for the back electrode as seen in Fig. 2.

B. Characterization and Measurement Techniques

Device performance was evaluated using several characterization methods. A profilometer was used to determine ZnTe film thicknesses and deposition rates. Current density versus voltage (JV) measurements were completed to determine device performance characteristics and parameters. JV measurements occurred at room temperature (~23°C). Capacitance-voltage (CV) measurements were performed to analyze carrier concentrations within devices. External Quantum efficiency (QE) measurements were taken to observe how specifically the rear surface of the device performed.

III. Results

A. ZnTe Process Temperature Sweep

All samples had standard copper treatments as to identify the effects of the ZnTe deposition temperatures. The standard process includes preheating the sample for 95 s at 330°C, CuCl deposition of 140 s at 190ºC, and annealing for 240 s at 200°C all under vacuum. Samples cooled for up to 5 minutes before further processing steps occurred.

For the samples displayed in the JV plots displayed in Fig. 3, the best ZnTe film was deposited at 250°C. This device had better open-circuit voltage (V_{OC}), a higher fill-factor, and a higher short-circuit current (J_{SC}) as compared to the 150°C sample. As the temperature reached 350°C the JV plot for the device began to show a rollover and high R_{sh} leading to poor device performance. Nominal values can be observed from Table 1.

Despite the differences in the JV plots, the QE measurements appeared to be very similar among each other except for the 350°C sample. This may suggest that the absorber properties were not substantially affected by the deposition of ZnTe:Cu. Deposition and back-contact parameters may need to be improved to enhance device performance. The plot of QE versus wavelength is displayed in Fig. 4.

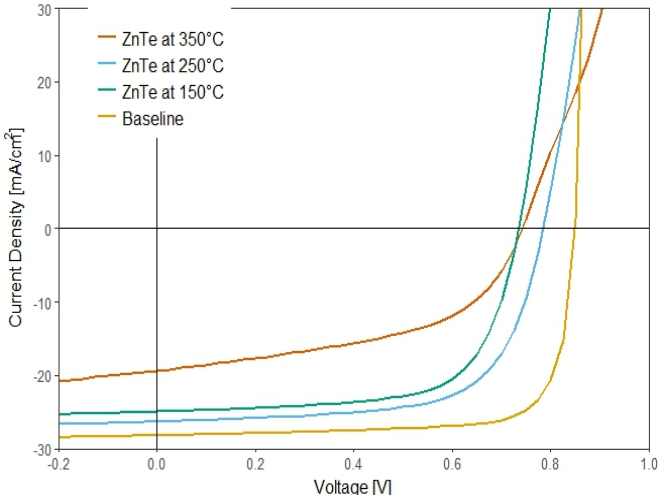

Fig. 3. JV plot of the ZnTe devices at different deposition temperatures and the baseline without ZnTe.

TABLE I
SUMMARY OF DEVICE PERFORMANCE

	J_{SC} (mA/cm^2)	V_{OC} (mV)	Fill Factor (%)	Efficiency (%)
Baseline	28.2	849	77.6	18.58
ZnTe at 350°C	19.4	742	50.7	7.28
ZnTe at 250°C	26.3	786	66.4	13.72
ZnTe at 150°C	25	735	67.3	12.35

The CV data displayed an interesting trend with the ZnTe samples as seen in Fig. 5. The carrier concentration (N_A) in case of baseline device was seen to be consistent across the thickness while ZnTe:Cu device exhibited an increase in carrier concentration towards the back. This appears to be an effect of high Cu concentration towards the back surface as compared to baseline device where the Cu dopant appears to be evenly distributed within the absorber.

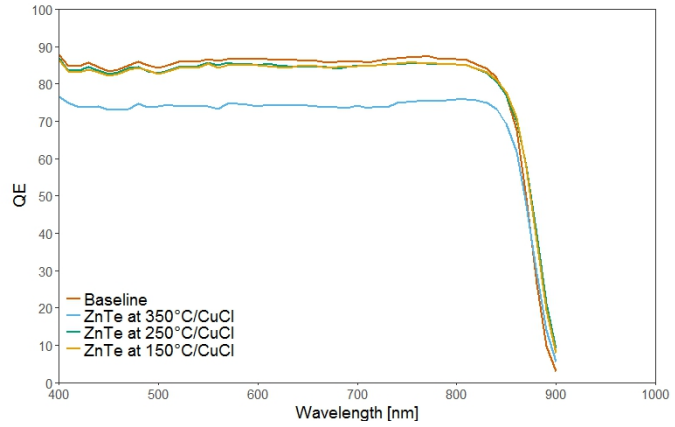

Fig. 4. QE plot of the baseline device without ZnTe and ZnTe devices at different temperatures.

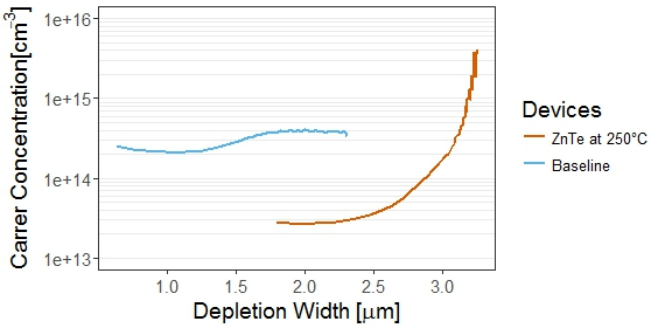

Fig. 5. CV data for the baseline device and ZnTe at 250°C.

B. Copper Doping

After analyzing the results above, the effectiveness of the copper doping was explored. Copper doping was explored based on the Fig. 5 and the premise that not enough copper was added to the ZnTe device. To prove the need for more copper, an experiment was conducted with no intentional copper doping and a longer copper treatment.

The device structure for the baseline and ZnTe samples were maintained the same as the previous samples. The ZnTe films in this experiment were deposited at 250°C for consistency.

The longer copper treatment (LCT) included a 120 s in the preheat source which is at 330°C, 280 s in the CuCl source at 190ºC, and 560 s in the anneal source which is at 200°C.

Fig.6. displays the JV curves for the different copper doping treatments. The devices with no intentional copper doping did not perform as well as the devices with copper. The longer copper treatment seemed to have improved both the baseline device and the ZnTe device in terms of J_{SC}, V_{OC}, and fill factor. Device parameters can be found in Table 2.

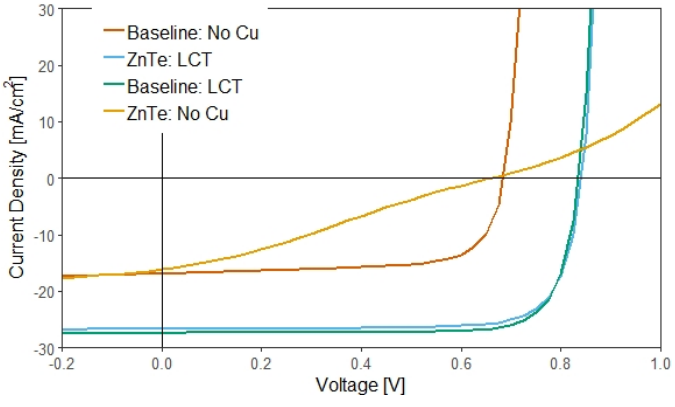

Fig. 6. JV plot of devices with no intentional copper doping and with a long copper treatment (LCT).

TABLE 2
SUMMARY OF DEVICE PERFORMANCE

	J_{SC} (mA/cm^2)	V_{OC} (mV)	Fill Factor (%)	Efficiency (%)
Baseline: No Cu	16.9	686	70.7	8.2
ZnTe: No Cu	16.1	661	27.5	2.94
Baseline: LCT	27.4	836	79.7	18.24
ZnTe: LCT	26.7	841	78.7	17.66

The carrier concentration vs depletion width data for the devices with and without intentional copper doping seems to vary greatly as seen in Fig. 7. The no-intentional-copper devices have a lower carrier concentration than the devices with intentional copper doping. The baseline with copper doping and the ZnTe device with copper doping have very similar profiles throughout the full device.

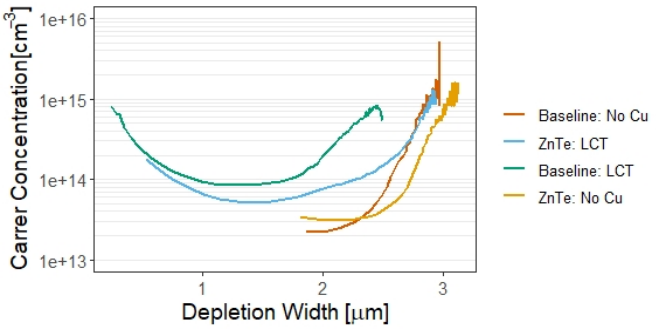

Fig. 7. CV data for the baseline device and ZnTe devices with and without intentional copper doping.

IV. CONCLUSIONS AND FUTURE WORK

It has been verified that substrate temperature during ZnTe deposition has a substantial effect on device properties. The ZnTe deposition and annealing temperature of 250°C provided good device performance.

Adjusting the copper doping on baseline and ZnTe devices also impacted performance. The no intentional copper devices had lower J_{SC}, V_{OC}, and fill factor. The longer copper treatment baseline and ZnTe devices had a much better performance and the two devices were very comparable.

While the above devices have not been optimized, it is apparent that ZnTe deposition temperature and copper doping have a significant impact on ZnTe device performance.

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