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Analysis of CdTe photovoltaic cells for ambient light energy harvesting

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Abstract

This paper investigates the suitability of CdTe photovoltaic cells to be used as power sources for wireless sensors located in buildings. We fabricate and test a CdTe photovoltaic cell with a transparent conducting oxide front contact that provides for high photocurrents and low series resistance at low light intensities - and measure the photovoltaic response of this cell across five orders of magnitude of AM1.5G light intensity. Efficiencies of 10% and 17.1% are measured under ~1 W/m^2 AM1.5G and LED irradiance respectively, the highest values for a CdTe device under ambient lighting measured to date. We use our results to assess the potential of CdTe for internet of things devices from an optoelectronic, as well as a techno-economic perspective, considering its established manufacturing know-how, potential for low-cost, proven long-term stability and issues around the use of cadmium.

Introduction

The use of photovoltaic cells to power internet of things (IoT) devices in buildings has the potential to significantly reduce the maintenance issues associated with batteries and presents a significant market opportunity [1], [2]. A large number of photovoltaic technologies have been investigated for their effectiveness at converting ambient light from incandescent, compact fluorescent or LED bulbs into electrical energy including silicon, III-V, perovskite and organic PV devices [3]–[5]. Despite being the most successful thin-film photovoltaic technology in the solar power market, the use of CdTe to power IoT nodes has been little investigated. This is despite the many advantages of the technology for this application including its ~1.4 eV bandgap that is relatively well matched to typical indoor light spectra as compared to silicon [1], its proven stability as compared to perovskite and organic PV materials [6], its lower cost than III-V cells and its established manufacturing base. Furthermore, CdTe solar panels are known to perform better than their silicon counterparts under low level diffuse radiation [7].

Studies of CdTe PV cells under low light intensity have shown them to have a superior relative efficiency and voltage at low intensities than comparable c-Si and GaAs cells [8]. CdTe/CdS solar cells show an efficiency of around 11% under 1000 W/m^2 AM1.5G standard test conditions (STC) and retain around 8 % efficiency at 1 W/m^2, while the open-circuit voltage remained as high as 600 mV under low light conditions. More recently, a similar efficiency of 9% was measured for a CdTe cell under 8 W/m^2 AM1.5G with an open-circuit voltage of 600 mV – the fitted series resistance, R_s, for these cells was 150 ohm.cm^2 at the lowest light intensities. The only measurements of CdTe cell performance under typical indoor light sources in the literature is for a cell with an efficiency of 9.5% under STC, that increases to 10.9% under 9.1 W/m^2 compact fluorescent lighting - a smaller increase than might be expected for CdTe under a better matched spectrum [9].

In this paper, we use measurements on an existing CdTe photovoltaic cell to discuss the physical changes and innovations needed to construct a good indoor CdTe device. We present a CdTe photovoltaic cell with a transparent conducting oxide (TCO) front contact and measure its performance versus light intensity across five orders of magnitude AM1.5G and under low level LED irradiance. We

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discuss the implications of going to low light intensities; where the generated photocurrent reduces 3 orders of magnitude while the photovoltage is, ideally, decreasing logarithmically. In a silicon cell at low light intensities, SRH recombination results in a stronger decrease in voltage, making them less suitable for indoor applications, but most thin-film cells, including ours, show close to the expected behaviour. The fill factor behaviour depends on a range of contributors, resistances and ideality factor; while series resistance is expected to increase, and does a little, but becomes less relevant because of the strongly reduced currents. Furthermore, we discuss how the cost and manufacturing scale of this technology offer significant benefits to its widespread use, while highlighting potential ROHS challenges in the use of cadmium in electronics devices.

Methods

The devices used in this study were fabricated using an in-line thin-film device fabrication system at Colorado State University. The substrate used for these devices were TEC10 soda-lime glass with ~400 nm of fluorine-doped tin oxide (FTO) deposited by the glass manufacturer that serves as the transparent conducting oxide. The substrates were thoroughly cleaned using detergent based industrial glass cleaner (Micro 90) and an ultrasonic cleaner. After drying the rinsed glass in isopropanol vapor, a 100 nm of $Mg_xZn_{1-x}O$ (MZO) buffer layer was deposited from a single sputter target using RF sputter deposition under argon environment with ~5% oxygen [10]. The RF power was maintained at 180 W during the deposition of the film. The thickness of the deposited MZO layer was confirmed using a profilometer. After sputter deposition of the MZO layer, the substrate was moved to an in-line fabrication system with 9 process stations. This system allows deposition and passivation treatment of film stacks without intermediate exposure to air and substantially reduces interfacial defects within the fabricated devices. The substrate is placed on an end-effector mechanism that travels through the 9-station process station system through a magnetic transfer mechanism. The substrate transport mechanism is an externally controlled using a LabView program that was optimized for this process. The sequence of deposition and dwell time in each deposition or treatment source is programmable and is given in Table 1. Each process station has a bottom source heater that heats the material for deposition and a top source heater that maintains the temperature of the substrate. The system of top and bottom heater also enables better control of temperature gradient to ensure uniform film deposition. There is a pyrometer located outside the preheating station that records the substrate temperature when it exits the preheating station. Table 1 summarizes the processing conditions for the deposition of the absorber film stack. The temperature of the graphite deposition sources are maintained within ±1°C of the setpoint using PID controllers and the temperature is verified using redundant thermocouples. The CdSeTe composition used for this study had 40% CdSe in the source material and the as-deposited films had a band-gap of ~1.41 eV measured using optical transmission measurements and the Tauc plot method.

Table 1: Summary of fabrication conditions for CdSeTe/CdTe graded absorber and CdCl2 defect passivation.

Process step:	Pre-heat	$CdSe_xTe_{1-x}$ deposition (x = 40%)	CdTe deposition	$CdCl_2$ deposition	Cool
Top temperature (°C)	620	420	500	425	-
Bottom temperature (°C)	620	575	555	450	-
Dwell time (s)	140	360	180	600	180
Thickness (µm)	-	~ 1.5 – 2.0	~3.5	-	-

The cooling station did not have any active heaters. It is a blank station with a containment enclosure that allows the substrate to cool to temperature below 200°C before being removed from the deposition system and being exposed to air. This helps in reducing uncontrolled oxidation of the fabricated film

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on exposure to atmosphere. The $CdCl_2$ passivation treatment leaves a thin residual layer of $CdCl_2$ that is rinsed off using deionized water.

Following the deposition and defect passivation of the absorber film, the substrate was introduced into a three-station vacuum system that is designed for Cu-doping of the devices. This system is similar in construction to the above described 9-station system where a sample is transported between stations using a magnetic transfer arm. The three process stations here are preheating, CuCl deposition and Cu annealing. Processing conditions for CuCl treatment are summarized in the Table 2.

Table 2: Summary of CuCl doping conditions.

	Pre-heat	CuCl	Cu anneal
Top temperature (°C)	330	170	200
Bottom temperature (°C)	330	190	200
Dwell time (s)	90	110	220

During the CuCl treatment, the substrate is preheated to ~140°C. CuCl is used to deposit a highly controlled layer of Cu by reduction of CuCl at the set temperature. Following the deposition of Cu, the annealing process diffuses small amounts of Cu into the film that acts as the p-type dopant while remaining Cu at the surface, enabling the formation of an ohmic contact. After the CuCl treatment, the substrate is removed from the system and introduced into a single-station metal evaporator to deposit ~30 nm of Te which has been found to be advantageous in improving open-circuit voltage of the fabricated devices [11], [12]

Following this step, carbon and nickel in a polymer binder were applied by spraying one layer of each on the back surface of the device. After allowing the paint to dry and cure over 60 minutes, 25 cells with an area of ~0.65 cm^2 were masked and delineated. Thin lines of indium were drawn on the delineated regions using a solder iron that formed the n-contact. A schematic of this device structure is shown in Figure 1 (a) and a representative device performance is shown in Figure 1 (b). Device efficiency of over 19% has been achieved using similar device structure fabricated using the above described method [12].

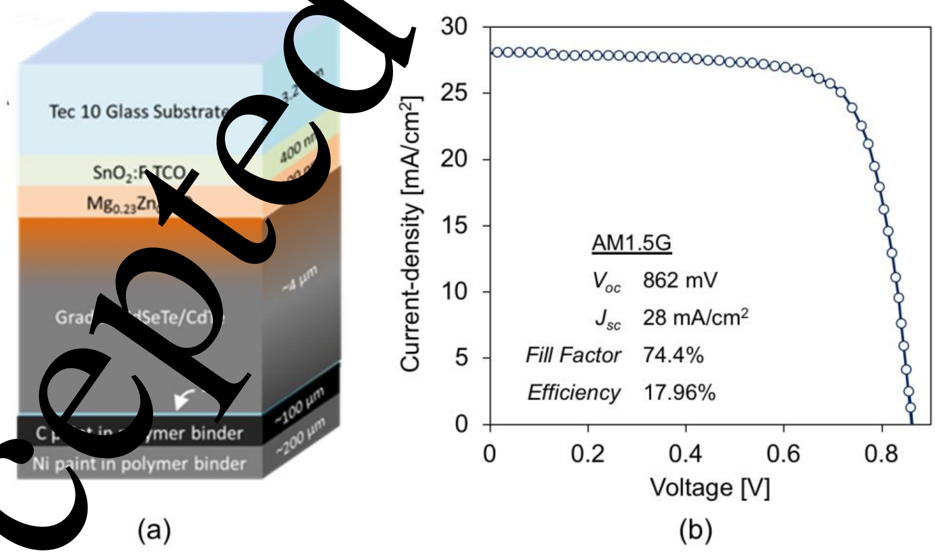

Figure 1: (a) Schematic of device structure (not to scale) under study and (b) Representative device performance immediately after cell fabrication.

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The photovoltaic cells 1 sun characteristics were measured using a Solar Simulator that included an Oriel 3A Class AAA Solar Simulator and an AM1.5G optical filter designed to simulate the AM1.5G solar spectrum. Current–voltage sweeps were conducted using a Keithley 2400. A mono-Si reference cell, calibrated by National Renewable Energy Laboratory's Solar cell/Module Performance Group on March 6, 2018, was used when establishing 1 sun light intensity while a temperature control stage kept samples at 25 ºC. The indoor photovoltaic performance measurement setup was housed in a dark box and used the same electronics as for 1 sun measurements, but the cell was illuminated using a dimmable Philips Hue E26 LED bulb. The intensity of this low-level illumination was controlled using the bulbs set points and was measured at the cell using a calibrated Si photodiode. The intensity of light on the solar cell was set for each measurement taken over a 0.2 – 3 W/m^2 range to mimic the expected illumination conditions in an office environment [6]. The external quantum efficiency (EQE) measurement setup included a Xe lamp, a monochromator and filter wheel assembly to isolate light of a specific wavelength, and optical mirrors to guide the light onto the PV cell stage. The system measured the quantum efficiency by comparing the current from the device to a calibrated Si photodiode.

Results

For the tests undertaken across multiple light intensities, cells at the edge of the substrate were used, owing to probing limitations in the low light set-up, that exhibit slightly lower efficiency than the best cells in the centre of the glass substrate. The current-voltage curve for a typical CdTe PV cell used for low light measurements is presented in Figure 2(a) and shows an efficiency of 14.3% under 1 sun conditions with an open-circuit voltage of 840 mV, a short-circuit current density of 27.7 mA/cm^2 and a fill factor of 66%. Across five orders of magnitude decrease in AM 1.5G light intensity, as shown in Figure 2 (c), the V_{oc} of the measured cell decreases from 840 mV to 520 mV. The fill factor of the device increases with decreasing light intensity owing to the reduced impact of series resistance as the light generated current decreases. The efficiency of the device is presented in Figure 2 (b) and shows an initial increase to coincide with the increase in fill factor, but then a decrease as the reducing V_{oc} impacts efficiency. Overall the device performance under low-light AM1.5G compares well to other CdTe PV cells in the literature with an efficiency of 10% measured under 0.76 W/m^2 irradiance. Under the lowest light intensity, 0.14 W/m^2, the single cell maintains an open-circuit voltage of 495 mV and a maximum power point voltage (not shown) of 387 mV and an efficiency of 8.65%. The cell maintains significant power output and a stable operating voltage at very low light intensities.

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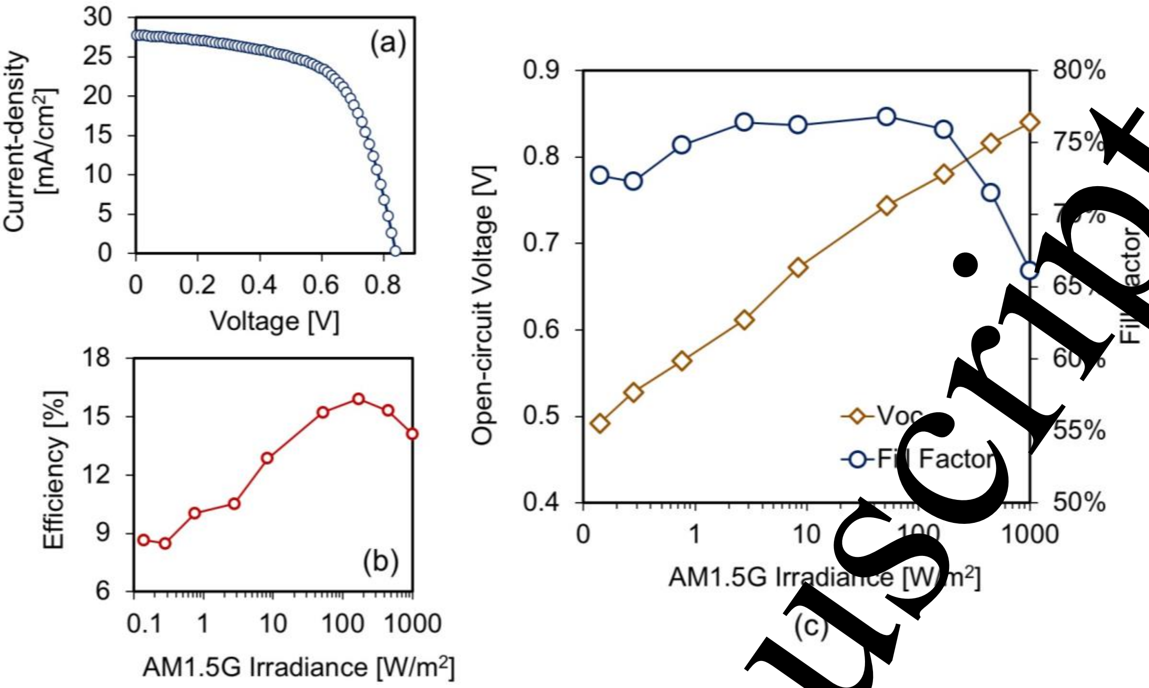

Figure 2: (a) Open-circuit voltage (green diamonds) and Fill Factor (blue circles) versus AM1.5G light intensity and corresponding fits to the data (dashed lines), (b) the measured external quantum efficiency of the cell, and (c) the measured photovoltaic conversion efficiency versus AM1.5G light intensity.

A fit of the electrical parameters of the cell to these measurements allows us to investigate the impact they have on the cell performance at different light intensities. We fit a two-diode model to the data, as given in Equation 1 where, J, is the total current density, J_L, is the light-generated current density, J_{oi}, is the recombination current in diode i, V, is the applied voltage, n_i, is the ideality factor of diode i, R_s, is the series resistance, R_{sh}, is the shunt resistance, T, is the junction temperature, and k is the botlzmann constant. We begin by assuming the ideality, $n_1 = 1$ and we set a limit to the maximum possible R_{sh} of $1x10^6$ ohm.cm^2.

$$J = J_L - J_{o1}\left\{exp\left[\frac{q(V+JR_s)}{n_1 kT}\right] - 1\right\} - J_{o2}\left\{exp\left[\frac{q(V+JR_s)}{n_2 kT}\right] - 1\right\} - \frac{V+JR_s}{R_{sh}} \quad (1)$$

Our model results fit the plots of V_{oc} and *Fill Factor* closely, as shown in Figure 2 (c). The fitted electrical parameters are provided in Figure S1 of the Supplementary Information. We found that J_{o2} dominates at all light intensity for our devices with an ideality of n_2 ~2 up to 200 W/m^2 before increasing to ~4 at 1000 W/m^2, while the shunt resistance, R_{sh}, of the device decreases with light intensity – a high shunt resistance is vital to maintain high performance at low light intensity where shunt pathways can be the main loss in most cells under low-light conditions [14]. Our parameter fit shows how our CdTe cell is uniquely suited to low light IoT applications and explains why significant voltages are produced even at the lowest light intensities. The series resistance, R_s, also remains low across all light intensities, < 7 ohm.cm^2, indicating the quality of the TCO contact layer. In comparison to silicon cells, where the current path changes with light intensity and impacts R_s, in our cells, it remains relatively low as the only current path is through the TCO and there is no metal contact pattern.

Finally, to gauge how the cell will operate under indoor light conditions, we measure its efficiency under low-light LED irradiance in a 0.2 – 2.9 W/m^2 range – similar to 100 – 1000 lux levels in buildings, and given the widespread use of a-Si for indoor photovoltaic products, we compare it to a commercial

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a-Si photovoltaic cell (a Powerfilm Solar OEM module). The results are plotted in Figure 3. Again, for the CdTe cell, the V_{oc} remains above 500 mV across all light intensities. The peak efficiency measured is 18.45% under 2.9 W/m^2 while an efficiency of 15.2% is measured under the lowest light intensity of 0.2 W/m^2. The cell efficiency remains above 17% at a light intensity as low as 1 W/m^2 – these values are the highest measured for CdTe IPV cells under ambient lighting and compare favourably to other thin-film technologies such as the commercial a-Si product which has an efficiency of 5-6% and in the low light range, and GaAs where a maximum efficiency of ~20% has been measured using a flexible cell under 1.3 W/m^2 LED lighting [1]. This high efficiency is partly attributable to the close match between the absorption and carrier collection of the 1.41 eV device as shown by the measured EQE of the device, presented in Figure 4 (a), to the measured incident spectrum from the LED lamp, also shown, and highlights the close match between the EQE of the device where it remains over [illegible]0% in a 400 - 830 nm range, with the peak of the spectrum between a 500 – 700 nm range.

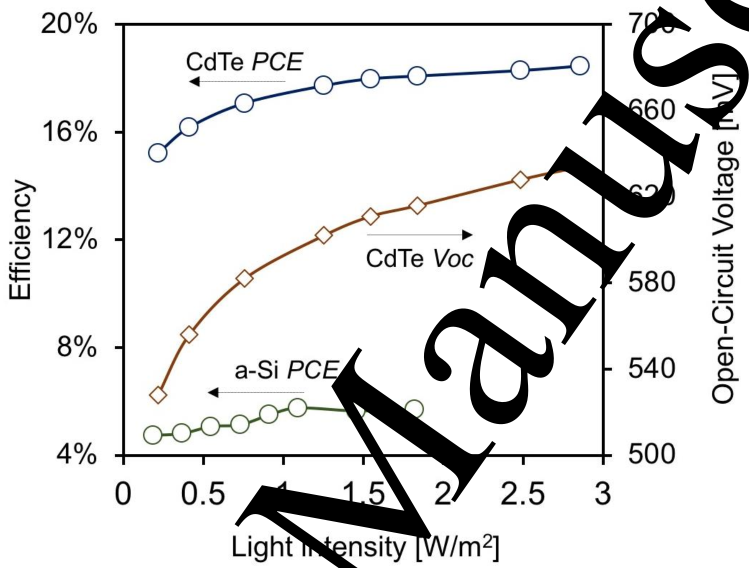

Figure 3: The CdTe PV cell efficiency and Open-Circuit Voltage under low intensity LED irradiance that is equivalent to ~200-2000 lux.

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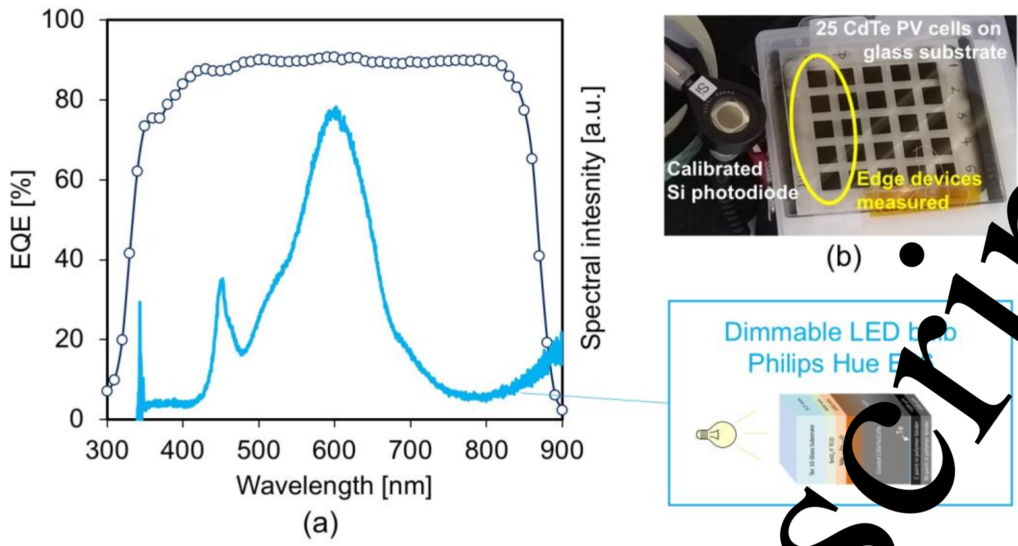

Figure 4: (a) The measured external quantum efficiency of one of our CdTe devices plotted against the measured emission spectrum from the Philips Hue E26 set to 'white light', and (b) an optical image of the glass substrate with 25 CdTe photovoltaic cells.

Discussion

Although below the best indoor PV devices in terms of efficiency, CdTe has impressive performance at very low light levels. Combined with the know-how available around its manufacturing at scale, CdTe solar modules long-term stability and the low manufacturing cost compared to other PV technologies, CdTe is a strong contender for indoor PV applications. In this section we discuss the physical changes and innovations required to make CdTe a leading option for indoor PV.

Optical

While the efficiency of our cells under LED illumination is significant, it falls below the >30% values now measured with perovskite and organic devices [15], [16], and far below the maximum values of ~60% predicted by detailed balance limit of efficiency measurements for optimum 1.9-2.0 eV bandgap devices [1], [9]. The same detailed balance calculations give ~40% as the maximum efficiency possible for a 1.41 eV device under white LED illumination. Therefore, to improve the efficiency of CdTe indoor photovoltaic devices, two options include using materials and device engineering to improve the efficiency of these devices above 17% (discussed below) or to build upon the research into wide-bandgap ternary CdTe alloys that incorporate Zn or Mn to increase the cell bandgap to 1.7-1.8 eV which would increase the expected efficiency to ~50% [17]. For indoor photovoltaic devices, however, it could be argued that efficiency is not as important a metric as for solar energy harvesting and that CdTe devices have additional advantages over other technologies that we discuss below.

Electrical

As discussed in the previous section, the carrier transport of these CdTe devices compare well to the other indoor photovoltaic devices under ambient lighting. As with all indoor devices, strong consideration must be given to minimize shunt resistance that often acts as the main parasitic resistive loss mechanism for devices under ambient lighting because of the very low currents produced. In our devices, the shunt resistance appears high as compared to compared to Si and a-Si and somewhat explains the strong performance at low light levels. As discussed in the previous sections, the addition of additional compounds to increase the bandgap is desirable. This would likely necessitate a change in contact materials for the ohmic contacts that will have some impact on the electrical characteristics.

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Cost

Our modelling recently established the cost to manufacture single-junction CdTe solar modules at 42.44 US$/m^2 [18]. This represents the number for a large ~1 m^2 module produced in a factory with a maximum production capacity of 300 MW/year. Producing smaller IoT modules would lead to a loss in economies of scale both in terms of the final product size, that will be on the cm^2-scale, and production capacity, when only MWs are likely to be required each year. This number implies a minimum cost to produce a 10 cm^2 IoT module of ~4 US cents. We consider this value the minimum possible and a better understanding of the impact of economies of scale is required to determine the exact cost of the technology for IoT applications as we have seen undertaken for perovskites [19], [20]. Nevertheless, CdTe is likely to be a low-cost option for IoT applications which, combined with the high prices that can be obtained in this growing market [21], can justify the likely increase in production cost. Currently, CdTe companies ship GWs of solar modules each year and this market is likely to increase in the future as the solar power market grows. In the interest of diversification of revenue streams, the indoor IoT space is expected to grow to a US$1 Bn market by 2025 [1]. Although smaller than the solar power market, capturing a portion of it would add a significant revenue stream for established CdTe manufacturers. The high prices that can be obtained for products in this market could likely support manufacturing in higher cost regions such as the USA and EU and act as a testing ground for new technologies before production is scaled to enter the wider solar power market.

Implications of using Cadmium

Owing to the use of Cd, any discussion on CdTe for indoor photovoltaics must include a section on the restriction of hazardous substances (ROHS) regulations. Currently, the most comprehensive regulations have been enacted in the EU where the ROHS directive 2011/65/EU came into full effect on the 22nd July 2019 and applies to all electrical and electronic goods regardless of their type, design or purpose. The Directive bans anyone from placing on the EU market electrical and electronic equipment (EEE) in which any homogeneous material contains more than the tolerated maximum concentration values (MCVs) of six substances including Cadmium. In fact, the tolerated MCV for each restricted substance is 0.1%, or 1,000 parts per million (PPM), except for cadmium which has a stricter limit of 0.01% or 100 PPM. In this context a homogeneous material is one that has a uniform composition throughout, or any component of the finished product that cannot be removed or detached by any action such as unscrewing or cutting, i.e., the whole CdTe IPV panel can likely be treated as a homogenous material placing a limit on the thickness of the CdTe material that is a function of the thickness of the other materials in the PV stack. The glass substrate will make up the majority of a stack, and in our experiments has a thickness of ~2 mm, placing a limit on the thickness of the CdTe film of ~640 nm (assuming the film is 50% Cd). While this is thinner than the current device design, photovoltaic films of this thickness are reasonable for indoor applications owing to the strong absorption of the shorter wavelengths in CdTe, and suggests a well-designed CdTe IPV device on glass should satisfy ROHS regulations. More generally, some types of EEE are exempt from restrictions on the use of hazardous substances including photovoltaic panels for public, commercial, industrial or residential use. In practice, under Waste Electrical and Electronic Equipment regulations [22], photovoltaic module manufacturers such as First Solar are responsible for the full life-cycle of their modules including the collection and recycling of panels. First Solar modules have been designed for recycling where 90% of the material in each module is recoverable and they have built recycling facilities all over the world [23].

Conclusions

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CdTe is the most successful thin-film photovoltaic technology on the solar power market today. Here, we investigated the suitability of a CdTe photovoltaic cells to be used as a power source for wireless sensors located in buildings to expand the range of applications for this technology. Our cell structure was fabricated with a TCO front contact that provided for high photocurrents and low series resistance at low light intensities – leading to significant power output and stable operating voltages at very low light intensities. Efficiencies of 10% and 17.1% were measured under 1 W/m^2 AM1.5G and LED irradiance respectively indicating CdTe devices are very suited to operation under low-light indoor conditions. While a greater understanding of the impact of economies of scale on the likely IoT module price is required, CdTe is a low-cost technology and it is likely that the higher prices obtainable in the IoT market will offset the extra cost in manufacturing small modules. While consideration is needed to ensure CdTe IPV modules will pass ROHS regulations in each geographic market, it is clear that this technology has significant potential to power the internet of things.

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