Reconfigurable and Dense Analog Circuit Design using Two Terminal Resistive Memory

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***Abstract*— Metal-oxide based bipolar Resistive RAM (RRAM) is one of the most promising candidates for the future non-volatile data storage. Due to unique properties e.g., small footprint, ability to modulate resistance states in wide ranges dynamically, hysteresis and CMOS compatibility, RRAM can be a fruitful candidate for analog circuit design. However, the recent literature only scratches the surface of this interesting prospect. In this paper, a single RRAM behavior is studied under temperature, voltage and process variations from an analog design standpoint. A comparative study is performed between two analog circuits namely, Common Source (CS) amplifier and differential amplifier with traditional passive resistors and with passive resistors replaced by RRAM along with two other design examples where RRAM can be integrated into analog circuits. Our study shows that blind swapping of passive resistors with RRAM in analog circuits can actually degrade the performance metrics. We propose techniques such as usage of RRAM Low Resistance State (LRS) to recover the loss. We also note that hyperbolic I-V characteristics of RRAM can inherently improve the linearity of RRAM based analog designs. Simulation results indicate that RRAM based amplifiers can achieve 30X area reduction, 120% higher bandwidth with only ~9% reduction in gain. The resistance modulation property of RRAM is applied to realize a source degenerated amplifier with reconfigurable linearity, to a constant transconductance bias circuit to avoid resistance trimming and to design a programmable active low pass filter. The proposed designs are benchmarked against contemporary analog designs using emerging nonvolatile memories.**

***Index Terms*—Analog design, Bandwidth, Gain, Linearity, Resistive RAM.**

I. Introduction

CONVENTIONAL analog circuits are plagued by Silicon area and power both of which scales poorly with technology. The footprint of analog designs is largely dominated by the passive resistors and capacitors. Significant area and power are also invested in trimming circuits to adjust various parameters, biasing circuits, and resistor and capacitor values at run-time. Replacing the passive components by a more compact and scalable device can potentially solve the above challenges. In this context, emerging resistive Non-Volatile Memories (NVMs) such as memristor, Resistive RAM (RRAM) (a variant of memristor), spin memristor and Domain Wall Memory (DWM) have been explored as alternative devices to replace passive resistors [1-11]. A substantial amount of research is devoted to evaluating memristor in analog circuits such as differential amplifier [3], comparator [4], Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC) [1-2]. RRAM can offer less parasitic capacitance than polysilicon-based passive resistors and its non-linear I-V characteristics can be utilized to improve the linearity of analog amplifiers. Unlike its passive counterpart, RRAM equips designers with resistance tuning capability. This can be beneficial to compensate for dynamic and statistical variation induced resistance fluctuation. A detailed study of RRAM's behavior from analog design perspective also unfolds a host of design challenges due to RRAM's intrinsic variability [12, 13], retention failure [14-16], limited endurance [17], and nonlinear I-V characteristics [17]. These challenges need to be adequately addressed by devising appropriate solutions and trade-offs need to be understood to gauge RRAM's potential as a viable candidate in analog circuits.

Our initial study reveals that blindfold replacement of the resistor with an RRAM can actually have negative consequence such as poor gain due to resistance fluctuation of RRAM under small signal biasing. Fig. 1 (a)-(b) shows a 4.5X loss in gain when a ~76K Ohm passive drain resistor of a Common Source (CS) amplifier is replaced with an RRAM programmed to the same resistance in High Resistance State (HRS). The loss in gain is eliminated by realizing the fact that RRAM is less sensitive to variation in Low Resistance State (LRS) and employing series connected RRAMs in LRS to increase the equivalent resistance.

In summary, the following contributions are made in this paper:

- We study the performance metrics like gain, bandwidth, and linearity of CS and differential amplifier with circuits realized by a resistor and RRAM respectively and propose substantial area reduction using RRAM.
- We improve the bandwidth of amplifiers with RRAM by utilizing its inherent low area capacitance.

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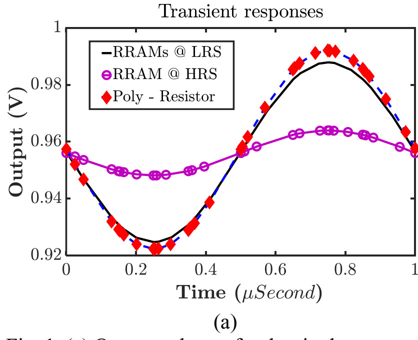

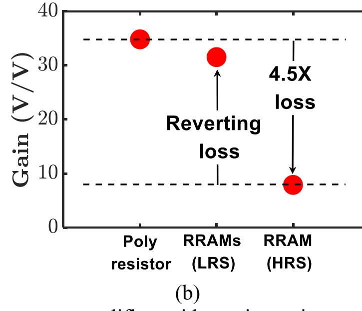

Fig. 1. (a) Output voltages for the single stage common source amplifiers with passive resistance, stack of RRAMs at LRS and RRAM at HRS. (b) Reduction in amplifier gain when passive resistance is replaced by RRAM at HRS. This loss of gain can be recovered by using series connected RRAMs at LRS.

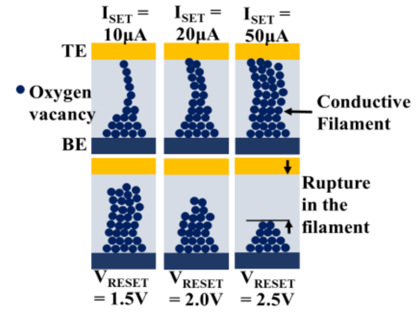

Fig. 2. Multilevel Cells (MLC) in RRAM can be achieved by changing SET current and RESET voltage. Higher SET current may widen the filament or form multiple filaments. Higher RESET voltages rupture the CF more.

- We demonstrate RRAM can be used in constant transconductance bias circuits and the resistance tuning property can potentially avoid the need for bulky trimming circuits.
- We study the active low pass filter with RRAM and show that the cut-off frequency can be dynamically changed.
- We identify the integration challenges of RRAM in analog design.
- We develop solutions e.g., series connected RRAMs to minimize the voltage across a single RRAM and selection of operating mode to address linear I-V relation, endurance and retention issues.

The rest of the paper is organized as follows. In Section 2, we describe the basics of RRAM. Performance of an isolated RRAM is discussed in terms of process, voltage and temperature variation in Section 3. Analog design examples based on RRAM are discussed in Section 4. Amplifier variability analysis is performed in Section 5. Process integration and resistance tuning challenges are discussed in Section 6. Finally, we draw a conclusion in Section 7.

II. Background Of Rram

In this section, we present the basics of RRAM and its modeling and simulation setup.

A. Basics of RRAM

RRAM is designed by sandwiching an oxide material between two metal electrodes i.e. Top Electrode (TE) and Bottom Electrode (BE). The operations of RRAM devices are believed to rely on the formation and partial oxidation of a Conductive Filament (CF) [17, 18], which is responsible for resistance switching and charge transport in both LRS and HRS. The current in LRS is attributed to electron drift through a metallic-like CF [17, 18]. Charge transport through HRS is due to a Trap Assisted Tunneling (TAT) process via the oxygen vacancy traps located in the oxidized portion of the filament [18, 19]. The resistance switching of RRAM involves three elementary processes such as formation, SET and RESET. The switching event from HRS to LRS is called the SET process. Conversely, the switching event from LRS to HRS is called the RESET process. The switching modes of metal–oxide RRAM can be broadly classified into unipolar and bipolar switching modes. In unipolar switching, the switching direction depends on the amplitude of the applied voltage but not on the polarity of the applied voltage. In bipolar switching, the switching can only occur at the reverse polarity.

B. RRAM Model and Simulation Setup

For simulation and analysis, we have used the ASU RRAM Verilog-A model [20] which is bipolar HfOx based resistive switching memory. Equations (1)-(5) are the key governing equations of RRAM behavior [20, 21]. Here, g is the average gap distance between the electrode and the tip of the CF, v_0 is the velocity dependent on the attempt-to-escape frequency, E_{ag} (E_{ar}) is the activation energy for oxygen ions to migrate from one potential well to another in the generation (recombination) process [22], L is the thickness of the switching material, a_0 is the hopping site distance, V is the applied voltage across the cell, γ is the field local enhancement factor that accounts for the polarizability [23] of the material. $I_0, V_0, g_0, v_0, g_1, \beta$, and γ_0 are fitting parameters.

$$I_{CF} = \frac{S_{CF}V_{CF}}{\rho(L-g)} \quad (1)$$

$$I_{hop} = I_0 \times exp\left(-\frac{g}{g_0}\right) \times sinh\left(\frac{V}{V_0}\right) \quad (2)$$

$$\frac{dg}{dt} = -v_0\left[exp\left(-\frac{qE_{ag}}{kT}\right)exp\left(\frac{\gamma a_0}{L}.\frac{qV}{kT}\right) - exp\left(-\frac{qE_{ar}}{kT}\right)exp\left(\frac{\gamma a_0}{L}.\frac{qV}{kT}\right)\right] \quad (3)$$

$$\gamma = \gamma_0 - \beta\left(\frac{g}{g1}\right)^3 \quad (4)$$

$$g(t+dt) = g(t) + dg \quad (5)$$

C. Multilevel Cell Capability of RRAM

Another property of RRAM that adds to its resistance modulation capability is the Multi-Level Cells (MLC) [24, 25] which means that by changing the SET and RESET conditions we can achieve different HRS and LRS values for the same RRAM. Fig. 2 explains the origin of multiple LRS and HRS states. In LRS multiple levels can be achieved by changing the value of current compliance during the SET process. A larger value of programming current increases the probability of multiple filament formations which effectively increases the width of the CF and hence lowers the resistance value. On the other hand, multiple HRS can be achieved by changing the RESET voltage. A stronger RESET voltage means wider rupture in the CF that translates into higher resistance. Therefore, apart from modulating resistance between two discrete extremes that is HRS and LRS, the designers can fine-tune the resistance value within each state

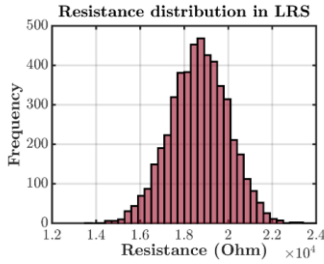

Fig. 3. Resistance distribution in LRS due to oxide thickness variation. The distribution is normal.

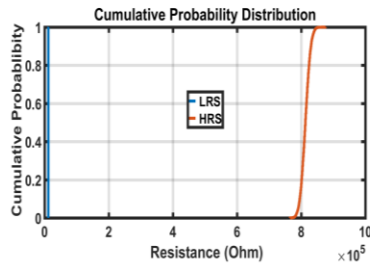

Fig. 4. Probability distribution of RRAM resistance with varying gap length. HRS is more sensitive to gap variation than LRS.

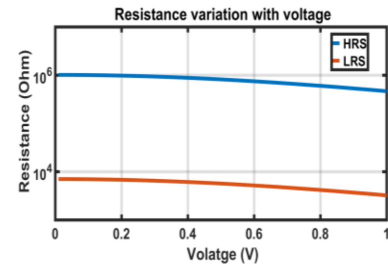

Fig. 5. Resistance variation of RRAM at HRS/LRS with voltage. The hyperbolic I-V relation leads to a non-linear resistance which decreases with voltage.

III. RRAM Analysis for Analog Design

In this section, we study the performance of an isolated RRAM under static and dynamic variation to accurately understand RRAM's potential in analog design and pertinent unique design challenges that may be absent in passive resistors.

A. Oxide Thickness Variation

The proposed simulation framework consists of Monte-Carlo analysis of an RRAM with a mean oxide thickness of 10nm with 20% as 3-sigma variation. An initial gap length of 1.7nm (for HRS) and 0.2nm (for LRS) is assumed. At HRS, no significant variation in the resistance value is observed. This can be explained by the evolution rate of tunneling gap (equation (3)) which weakly depends on the oxide thickness (L). Therefore, the rate of change of gap due to oxide thickness variation is quite less for the low voltage across the RRAM (0.2V for this simulation) to have any impact on the current value and the resistance. On the other hand, the resistance value in LRS is proportional to the oxide thickness (equation (1)) due to metal-like conduction through CF in LRS. Therefore, the resistance value in LRS follows a Gaussian distribution with process variation (Fig. 3). RRAM resistance programmability can be utilized to compensate for the process variation. For example, an appropriate level of compliance current can set the effective CF width to a value that can counteract the oxide thickness variation. An appropriate programming scheme [26] needs to be applied for this purpose.

B. Tunneling Gap Variation

RRAM has intrinsic variability [12, 13] which means that for the same device and same set of conditions, it may have different resistance values. This is due to the stochastic nature of the oxygen vacancy generation and recombination during SET and RESET process [27]. Therefore, the tunneling gap can vary from cycle to cycle and for the same programming condition. Since the I-V relation of RRAM is a strong function of the tunneling gap, the resistance value will vary with the tunneling gap. To study the effect of tunneling gap variation, we perform a Monte-Carlo simulation with a mean gap of 1.3nm (for HRS) and 0.2nm (for LRS), with 5% of the mean as an absolute variation. The cumulative probability distribution function is shown in Fig. 4. Resistance value at HRS varies substantially while the variation is insignificant in LRS. At LRS, the top and bottom electrode will eventually get shorted by the CF which effectively means a zero tunneling gap. Therefore, this small (close to 0) variation in the tunneling gap does not have a well-pronounced effect on the resistance. But, the amplitude of the current exponentially depends on the tunneling gap in HRS (equation (2)) which results in stronger dependence and hence more variation in the resistance value. To summarize, HRS is more affected by tunneling gap variation than LRS. Therefore, LRS is more suitable to design an analog circuit. We use this property to design more reliable RRAM (LRS) based amplifier.

C. Voltage Variation

RRAM current equation has a nonlinear component (at HRS and LRS) and a linear component (at LRS). This essentially means that unlike passive resistor which has a constant resistance with respect to voltage, RRAM has a variable resistance with voltage. This is a challenge for analog design since the resistance will vary with applied small signal voltage. To study this effect, we have swept the voltage from 0 to 1V. Resistance values are captured at different voltages. With the increase in voltage, the resistance decreases. At HRS the variation, $\frac{\Delta R}{R} \sim 8\%$ and at LRS the variation is ~ 6% over the range. This can be explained by the I-V equation below where the current has a hyperbolic dependence on the voltage across the RRAM:

$$R = \frac{\partial V}{\partial I} = \frac{\exp(gap/g_0)}{I_0 \cosh(V/V_0)} \qquad (6)$$

Since the gap in HRS is greater than the gap in LRS, the resistance changes more at HRS than at LRS. This observation leads to two design constraints: (i) If we need RRAM to behave as a linear resistance, the voltage across a single RRAM should be kept very small; (ii) To limit the resistance swing, LRS state of the RRAM should be used in analog designs as much as possible.

D. Temperature Variation

To study the temperature dependence of RRAM resistance, we have swept the temperature from 263K to 363K. A variation of $\frac{\Delta R}{R} \sim 8\%$ is observed over this temperature range. The resistance exhibits a negative-linear correlation (Fig. 6) with temperature which is in agreement with experimental results [28]. When the device is RESET to HRS, the CF is ruptured near the dielectric/electrode interface. The probability (p) of oxygen ions to overcome the potential barrier and create vacancies can be expressed as: $p \approx v \exp\left(-\frac{E}{K_B T}\right)$, Where E is the potential barrier height and T is the temperature [29]. Therefore, increased oxygen vacancy related trap density at high temperature enhances the trap-assisted tunneling. As a

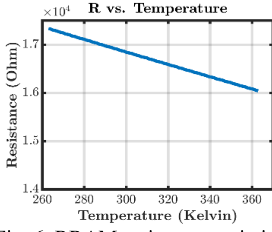

Fig. 6. RRAM resistance variation with temperature.

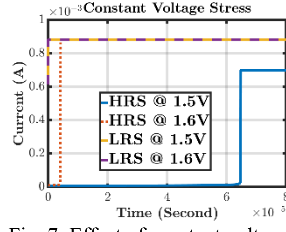

Fig. 7. Effect of constant voltage stress on RRAM.

result, current increases and resistance decreases. (More discussion to follow in Section V (C).)

E. Constant Voltage Stress

RRAM in analog designs may experience constants current through or voltage across it, unlike digital memory application where the RRAM may be written or read sporadically. Therefore, the effect of constant voltage stress on RRAM needs to be studied. We apply a constant stress voltage across an RRAM (at HRS and LRS both) in SET mode and observe the time required for the state to flip. Fig. 7 shows the result. After a certain amount time, HRS RRAM flipped to LRS. In case of RRAM in LRS, there is a slight decrease in resistance over time. This is due to the initiation of more conductive paths or an effective increase of filament radius under a continuous voltage. In both cases, it is observed that higher voltage causes faster change in the state. This provides us with an important insight that the voltage across the RRAM must be as small as possible for reliable operation and LRS is better suited for continuous voltage stress than HRS.

IV. Analog Circuit Design with RRAM

We employ the insights developed from the previous section to design and optimize analog circuits. Predictive Technology Model 65nm transistors [30] are used in the simulations unless otherwise stated.

A. Common Source Amplifier

Base Design: As a case study, we have taken a single stage CS amplifier (Fig. 8b). The (W/L) ratio of the transistor is 15µm/0.5µm and the supply voltage is 3V. The gate of the transistor is fed by 2 $mV_{peak\text{-}peak}$ sine-wave with appropriate DC bias. The amplifier shows a gain of ~34 V/V with ~76 kΩ resistance used as the drain resistance (R_D).

Design using RRAM: One possibility is to use a single RRAM in HRS with matching resistance as a passive resistor and another possibility is to use multiple series-connected RRAMs in LRS. The choice between these options is guided by the desired resiliency of the amplifier to endurance, resistance and inherent gain variation.

Fig. 1(a) shows the output voltage (hence gain) of CS amplifier with the above-mentioned configurations. There is a wide difference between the gains of the amplifier with R and amplifier with RRAM at HRS. The HRS has a nonlinear I-V curve and resistance due to which the output swing (or gain) is decreased. On the other hand, current at LRS is dominated by conduction though metal-like CF. Therefore, resistance at LRS is more linear than HRS. The behavior of amplifier with RRAM at LRS, therefore, closely matches with that of the amplifier with a passive resistor. For our case, 8 series connected RRAMs at LRS achieves the equivalent resistance of ~76 kΩ. To program the RRAMs 3 additional transistors (Fig. 8a) are needed. During programming, V_{DD} is disconnected, WL is asserted, SL is grounded and the gate bias voltage is changed to 0V. Therefore, the current flows from programming supply (BL) through RRAMs to ground and programs the RRAMs. Compared to polysilicon-based resistance that is estimated using MOSIS Scalable CMOS design rules (minimum poly-width in resistor = 5λ and minimum spacing of poly-resistors = 7λ where 2λ is 65nm) [31] and UMC 65nm technology data (sheet resistance of high ohmic resistor ~ 1kΩ/square) [32], 8 RRAMs with an active cell area of 40 × 40 nm^2 each [33] along with three programming transistors (assumed, W/L = 260nm/65nm) consumes ~ 30X less area. The poly resistor layout is assumed to be serpentine with unit resistor cell consisting 9 squares.

Non-linearity in RRAM resistance is a design challenge. Connecting multiple RRAMs in series can aid to mitigate this. As the voltage difference between V_{DD} and output node gets divided among the RRAMs, each RRAM experiences less voltage variation across it and hence the resistance of a single RRAM remains fairly constant as identified in Section III. Operating with series connected LRS RRAMs has another added advantage of inherent resiliency to retention failure. As single RRAM in this series connected scheme will experience much less voltage across it, the gap dynamics will not vary widely and the RRAM will retain its resistance state for a longer period leading to reliable operation.

In case of any retention failure or aging, the resistance tuning aspect can be leveraged to compensate the resistance drift or change. Programming schemes proposed in [26, 34, and 35] can be used. More discussion to follow in Section VI.

Quantitative Analysis

Gain and Linearity: For the same V_{DD}, biasing and input, the amplifier with RRAM shows a gain of ~32 which is slightly less (~8%) than the amplifier with equivalent passive resistance. Though small, RRAM resistance at LRS may still vary with the voltage across it. This variation contributes to the reduced gain. Therefore, using RRAM instead of passive resistance leads to Gain vs. Area trade-off.

Fig. 9 shows the voltage transfer curve of the single amplifier for 3 different configurations. RRAM in LRS and passive resistor configurations exhibit almost similar behavior. However, the transfer curve of the amplifier with RRAM at HRS provides an interesting perspective. The operating region of the curve has less slope (i.e. less gain) but it has a wider input linear range. For passive resistor and RRAM in LRS

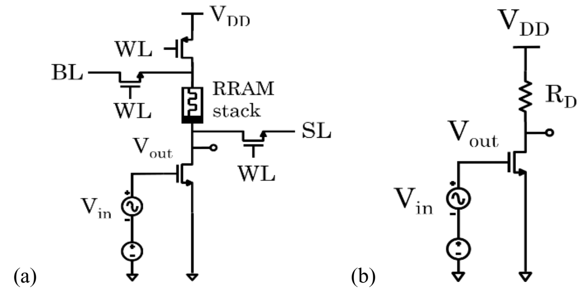

Fig. 8. Single stage common source amplifier with (a) RRAM. Additional transistor is added to enable programming capability and (b) passive resistor.

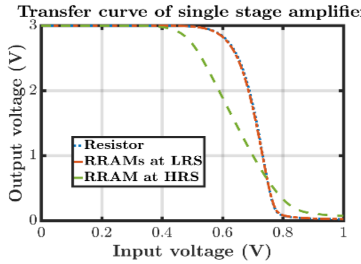

Fig. 9. Voltage transfer curve for single stage amplifier with resistor, RRAMs at LRS and at HRS as drain resistance.

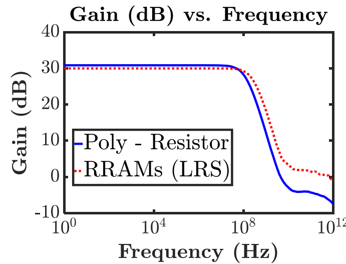

Fig. 10. Gain vs. Bandwidth plot of single stage Common-Source amplifier.

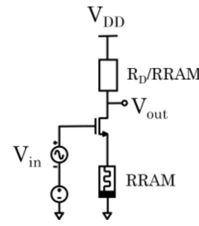

Fig. 11. RRAM degenerated CS amplifier

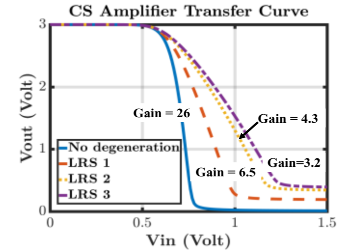

Fig. 12. Voltage transfer curve of the source degenerated CS amplifier.

configuration, the input linear range is roughly 0.65V-0.75V whereas, for RRAM in HRS configuration, the range is roughly 0.45V-0.75V. Therefore, the linear range is increased by ~200%. This improvement in linearity is achieved inherently without any linearization technique (e.g. source degeneration). This is primarily due to the non-linear I-V relation of RRAM. In analog design theory, it is understood that voltage amplifiers can be viewed as a cascade of two nonlinear stages. The input voltage applied to the gate of the transistor generates a super-linear current ($I \sim (V_{gs} - V_t)^2$). When this current flow through the RRAM, owing to sub-linear V-I relation ($V \sim \sinh^{-1}(I)$), it generates a linear voltage drop across the RRAM. Therefore, the two stages work in complementary fashion and second stage cancel outs the nonlinearity introduced by the first stage.

Bandwidth (BW): LRS RRAM based amplifiers show better bandwidth compared to a passive resistor (Fig. 10). As the plate size of RRAM can be very small (e.g. 40 nm × 40 nm), the plate to ground capacitances ($C = \frac{\epsilon_r \epsilon A}{d}$) of RRAM are insignificant and can be ignored for the operating range of frequencies. Moreover, RRAMs are farther from substrates than polysilicon (e.g. in [33], RRAMs are processed in Metal – 1 layer). On the other hand, the size of the passive resistor of comparable resistance is substantially larger than RRAM. Therefore, it has more parasitic capacitance compared to RRAM. Lesser area capacitance of RRAM is an added advantage for bandwidth and speed. From Fig. 7 the 3-dB bandwidth for RRAM based design is ~ 350 MHz compared to ~ 160 MHz bandwidth in resistor-based design (**2.2X higher**). This makes RRAM a candidate for high speed operation.

B. *CS Amplifier with Source Degeneration*

CS amplifier's linearity can be dynamically varied using the resistance tunability. Fig. 11 shows a source degenerated CS amplifier with RRAM. The programming transistors of RRAM are not shown for simplicity. Fig. 12 shows the corresponding transfer curves for the source degenerated CS amplifier. RRAM resistance can be programmed into different values to tune the amount of source degeneration. Therefore, we can achieve different levels of linearity and can dynamically trade-off between linearity and gain using a single configuration.

C. *Differential Amplifier*

Baseline Design: A basic fully differential pair is considered as in Fig. 13. A transistor is added as the tail current source. The input (2 mV peak-peak) is fed into the gates of top transistors. The output is taken out from the drains of top transistors. The V_{DD} is same as single stage amplifier.

Design with RRAM: The argument presented for the CS amplifier is valid for the differential amplifier. The RRAM at LRS configuration of the amplifier shows similar gain characteristics though the gain for RRAM based design is slightly less than the resistor-based design. Fig. 14 shows the output wave swings for two differential amplifier configurations. RRAM based amplifier has a gain of ~23.5 which is ~9.6% less than the gain of resistor-based design which is ~26. However, RRAM based design demonstrates superior bandwidth than a poly-resistor. Fig. 15 shows that the 3-dB bandwidth of RRAM based amplifier is ~ 320 MHz and for poly-resistor-based design, it is ~ 160 MHz. That means RRAM based design has 2X more bandwidth than a resistor-based amplifier.

D. *Source Degeneration using RRAM*

Tavakoli and Sarpeshkar [36] demonstrated that sinh I-V characteristics can be useful to linearize the differential pair. They proposed an 8-transistor circuit to generate an output current that is proportional to the sinh of the input differential voltage across it. We note that RRAM inherently possess a sinh I-V relation. Therefore, this non-linear I-V relation can be exploited to design a more linear differential pair. Compared to [36], the proposed design is compact (single RRAM vs 8 transistors) and simpler. To test the hypothesis, we put an RRAM as a source degeneration element (Fig. 13(b)) and simulated the design. The results are shown in Fig. 16. Differential pair degenerated with RRAM shows better linearity. As evident from the transfer curve, the linear range of operation increases by ~5X (from +/- 0.05V of input to approximately +/-0.25 V).

E. *Constant Transconductance Biasing Circuit*

Fig. 17 shows a constant gm biasing circuit. The reference current is given by the following equation:

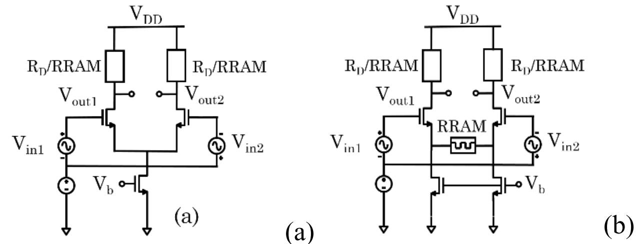

Fig. 13. Fully differential amplifier (a) without source degeneration and (b) with source degeneration using RRAM. Programming transistors are not shown onwards for clarity.

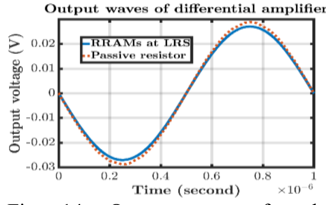

Fig. 14. Output waves for the differential amplifier.

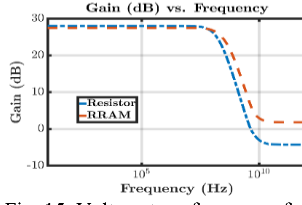

Fig. 15. Voltage transfer curve of differential amplifier.

$$I_{REF} = \frac{1}{8.R^2 \mu_n C_{OX} \left(\frac{W}{L}\right)_{MB1}} \quad (8)$$

The current value depends on the resistance R. RRAM can replace the passive resistor to realize this constant g_m biasing circuit. Table 1 shows the results of the circuit with a passive resistor and with RRAM. Carefully combining three LRS RRAMs in parallel can achieve desired I_{REF} and V_{biasp} (Table 1). However, the main benefit of using RRAM in the network stems from its resistance tunability. Generally, I_{REF} is very sensitive to resistance variance. The reference current is mirrored in other branches in typical analog design and therefore, the I_{REF} has to be precise. This precision of R-value (thus, I_{REF} value) is achieved through trimming. However, trimming networks are large and occupy substantial area in the chip. RRAMs can be programmed to desired resistance value without any trimming circuit. Therefore, with additional

TABLE I

CONSTANT G_M BIAS NETWORK PERFORMANCE COMPARISON

	RRAM	Poly (R = 5.5kΩ)
I_{REF}	13.1µA	13µA
V_{biasp}	633 mV	626 mV

transistors for programming and one-time calibration, RRAM can replace the necessity of trimming circuit to achieve precision reference current.

F. Tunable Active Filter with RRAM

RRAM can be used to design reconfigurable active filters. Fig. 18 shows a common topology of an op-amp based active low-pass RC filter. The cut-off frequency and DC gain of the filter are given by following equations:

$$\omega_C = \frac{1}{R_2 C} \; and \; DC \; gain = -\frac{R_2}{R_1} \quad (9)$$

Therefore, by changing the resistance value of R_2, the cut-off frequency of the filter can be tuned. The circuit in Fig. 18 is simulated with RRAM at R_1 and R_2. Fig. 19 shows the frequency response of the filter with three different values of RRAM resistance R_2 (DC gain is kept at 1 i.e. $R_1 = R_2$). It shows

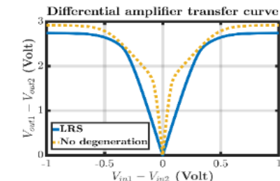

Fig. 16: Volatge transfer curve of degenerated differential amplifier.

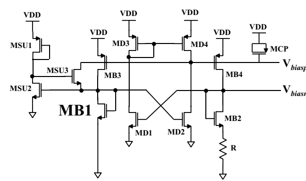

Fig. 17: Constant g_m biasing circuit.

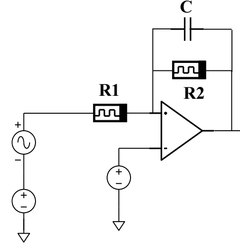

Fig. 18. An active low-pass filter. $R_{1/2}$ are realized with RRAMs (LRS).

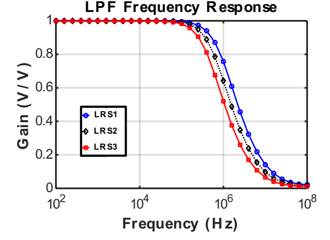

Fig. 19. Frequency response of the filter. LRS – 1/2/3 corresponds to three different configurations of (R_1, R_2) pair.

by tuning the RRAM resistance value, the cut-off frequency of the filter can be reconfigured.

V. Variability Analysis

In Section III, variability analysis for a single RRAM was presented. In this section, the analysis is extended to a full circuit implementation i.e. CS amplifier.

A. Supply Voltage Variation

Supply voltage variation is tested with a VDD sweep from 2.7V to 3.3V (±10%). The effect is shown in Fig. 20(a). The circuit performance is more susceptible to supply drop than supply rise from the nominal value.

B. Tunneling Gap Variation

Monte-Carlo simulation is run for 5000 times with mean tunneling gap of 0.1nm, an absolute variation of 10% of the mean gap and at one sigma level. The result is shown in Fig. 20(b). The distribution is normal with a mean of 31.55 and standard deviation of 0.2457. The low value of the standard deviation means at LRS the circuit performance does not suffer widely due to initial gap variation. At LRS, the tunneling gap is quite negligible or absent. Therefore, the tunneling gap variation has less impact on the gain.

C. Temperature Variation

At LRS, the conduction of RRAM is more metal-like. Therefore, it can be assumed that RRAM resistance at LRS will vary like a conventional resistor with temperature. Experimental verifications [37], [38] corroborate this assumption as well. According to [38] cells with strong ON-

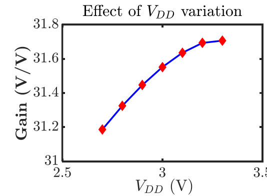

Fig. 20(a): Effect of supply voltage variation.

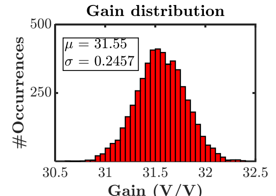

Fig. 20(b): Effect of initial gap variation.

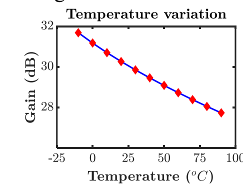

Fig. 20(c): Effect of temperature on amplifier gain.

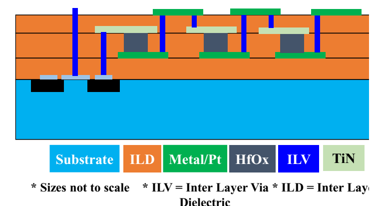

Fig. 21: Possible realization of RRAM based CS amplifier.

TABLE II
Comparative analysis of proposed RRAM based analog circuits

	Circuit / Metrics	Gain	BW in MHz	Power (µW)	Technology	Dynamic trade-off	Linearity
[3]	PGA*	32.34	-	-	Memristor	-	
[4]	PGA	2-11	-	-	Memristor	-	
This work	**Proposed CS amp**	31.6	350	60	RRAM	Gain vs. Linearity	0.3V (HRS)
	Proposed diff amp	23.5	320	120	RRAM	Gain vs. Linearity	±0.25V
	CMOS CS amp	34	160	60	CMOS	Fixed	0.1V
	CMOS Diff amp	26	160	120	CMOS	Fixed	±0.05V

* PGA = Programmable Gain Amplifier

state the readout resistance increases with temperature which suggests the metallic character of the conducting filament. Moreover, empirical results from [37] report the temperature coefficient of the conductive filament to be 4.2×10^{-4} K^{-1}. Considering these facts, we simulate the effect of temperature on the gain of the RRAM based amplifier and report the result in Fig. 20(c). The result shows that the gain drops with an increase in temperature.

VI. Final Remarks

A. Process Integration

To evaluate the potential resistive memories in analog design, process integration challenges has to be understood. RRAM fabrication is CMOS back-end-of-the-line (BEOL) compatible and there are numerous experimental demonstrations where RRAM has been seamlessly integrated into conventional CMOS technology. Fig. 21 shows a possible realization of an RRAM based analog circuit in CMOS. The fabrication process involves techniques like PVD, ALD, PECVD etc. which are well understood and post-silicon fabrication steps have a BEOL compatible thermal budget, not exceeding 400°C. Details of RRAM fabrication can be found in [33], [39]-[42]. Moreover, almost 100% yield has been reported for RRAM in crossbar memory architecture [17]. In analog circuits design rules can be more relaxed for RRAM as packing more memory element in the smallest feature size is not the end goal and therefore, the yield can be even better.

B. Resistance Tuning

Several benefits of RRAM based analog circuits stem from its resistance modulation property. Several programming techniques have been proposed to program RRAM at the desired resistance state [26], [35], [43]. RRAM achieves better resistance accuracy when a train of the programming pulse is used instead of a single pulse [43]. The pulse-trains can be two types: fixed width–variable amplitude or fixed amplitude–variable pulse width. For example, in [35] device conductance state is checked with a read pulse after each programming pulse. If conductance reaches the target with defined tolerance the program stops. If the conductance does not reach the target value, an additional pulse with increasing amplitude or incremental width is applied. Then conductance state is checked again and the flow repeats until the target is achieved. The programming circuitry can be off-chip and may be used for one-time calibration before the first use. It can be interfaced with the analog device through the programming transistors.

VII. Conclusion

We proposed analog circuit design techniques using RRAM. Our study reveals issues with the drop-in replacement of resistor with resistive memory devices and probable mitigations. Furthermore, we show that analog designs such as amplifiers can be benefitted in terms of area, dynamic reconfiguration and trade-off opportunities with the introduction of RRAM in the circuit. We explored possible applications and circuit design examples which can be benefitted from unique properties RRAM, for example improving amplifier linearity through RRAM's inherent sinh I-V, replacing large trimming network with tunable RRAM, reconfiguring analog specification like cut-off frequency of filter etc. All of these can be achieved with available CMOS fabrication process.

References

[1] L. Gao *et al.*, "Digital-to-analog and analog-to-digital conversion with metal oxide memristors for ultra-low power computing," *2013 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Brooklyn, NY, 2013, pp. 19-22.

[2] Y. V. Pershin, E. Sazonov and M. D. Ventra, "Analogue-to-digital and digital-to-analogue conversion with memristive devices," in *Electronics Letters*, vol. 48, no. 2, pp. 73-74, January 19, 2012.

[3] S. Shin, K. Kim and S. M. Kang, "Memristor Applications for Programmable Analog ICs," in *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 266-274, March 2011.

[4] Y. V. Pershin and M. Di Ventra, "Practical Approach to Programmable Analog Circuits with Memristors," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1857-1864, Aug. 2010.

[5] Vladimir V. Rakitin, Alexander V. Rakitin, "Ambipolar memristor-based oscillator," Proc. SPIE 10224, *International Conference on Micro- and Nano-Electronics 2016*, 1022411 (30 December 2016).

[6] K. Yogendra, M. C. Chen, X. Fong and K. Roy, "Domain wall motion-based low power hybrid spin-CMOS 5-bit Flash Analog Data Converter," *Sixteenth International Symposium on Quality Electronic Design*, Santa Clara, CA, 2015, pp. 604-609.

[7] Zhezhi He and Deliang Fan. 2016. A Low Power Current-Mode Flash ADC with Spin Hall Effect based Multi-Threshold Comparator. In Proceedings of the 2016 International Symposium on Low Power Electronics and Design (ISLPED). ACM, New York, NY, USA, 314-319.

[8] Q. Dong, K. Yang, L. Fick, D. Fick, D. Blaauw and D. Sylvester, "Racetrack converter: A low power and compact data converter using racetrack spintronic devices," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 585-588.

[9] Y. K. Upadhyaya, M. K. Gupta, M. Hasan and S. Maheshwari, "High-Density Magnetic Flash ADC Using Domain-Wall Motion and Pre-Charge Sense Amplifiers," in *IEEE Transactions on Magnetics*, vol. 52, no. 6, pp. 1-10, June 2016.

[10] Q. Dong, K. Yang, L. Fick, D. Fick, D. Blaauw and D. Sylvester, "Low-Power and Compact Analog-to-Digital Converter Using Spintronic Racetrack Memory Devices," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 3, pp. 907-918, March 2017.

[11] M. Sharad, C. Augustine and K. Roy, "Boolean and non-Boolean computation with spin devices," *2012 International Electron Devices Meeting*, San Francisco, CA, 2012, pp. 11.6.1-11.6.4.

[12] S. Yu, Y. Wu, Y. Chai, J. Provine and H. S. P. Wong, "Characterization of switching parameters and multilevel capability in HfOx/AlOx bi-layer RRAM devices," *Proceedings of 2011 International Symposium on VLSI Technology, Systems and Applications*, Hsinchu, 2011, pp. 1-2.

[13] A. Fantini *et al.*, "Intrinsic switching variability in HfO2 RRAM," *2013 5th IEEE International Memory Workshop*, Monterey, CA, 2013, pp. 30-33.

[14] J. Park *et al.*, "Investigation of State Stability of Low-Resistance State in Resistive Memory," in *IEEE Electron Device Letters*, vol. 31, no. 5, pp. 485-487, May 2010.

[15] S. Yu, Y. Y. Chen, X. Guan, H.-S. P. Wong, and J. A. Kittl, “A Monte Carlo study of the low resistance state retention of HfOx based resistive switching memory,” *Applied Physics Letters*, vol. 100, no. 4, p. 043507, 2012.

[16] B. Gao *et al*., "Modeling of Retention Failure Behavior in Bipolar Oxide-Based Resistive Switching Memory," in *IEEE Electron Device Letters*, vol. 32, no. 3, pp. 276-278, March 2011.

[17] H. S. P. Wong *et al*., "Metal–Oxide RRAM," in *Proceedings of the IEEE*, vol. 100, no. 6, pp. 1951-1970, June 2012.

[18] S. Yu, R. Jeyasingh, Yi Wu and H. S. Philip Wong, "Understanding the conduction and switching mechanism of metal oxide RRAM through low-frequency noise and AC conductance measurement and analysis," *2011 International Electron Devices Meeting*, Washington, DC, 2011, pp. 12.1.1-12.1.4.

[19] S. Yu, X. Guan, and H.-S. P. Wong, “Conduction mechanism of TiN/HfOx/Pt resistive switching memory: A trap-assisted-tunneling model,” *Applied Physics Letters*, vol. 99, no. 6, p. 063507, Aug. 2011.

[20] P. Y. Chen and S. Yu, "Compact Modeling of RRAM Devices and Its Applications in 1T1R and 1S1R Array Design," in *IEEE Transactions on Electron Devices*, vol. 62, no. 12, pp. 4022-4028, Dec. 2015.

[21] H. Li *et al*., "Variation-aware, reliability-emphasized design and optimization of RRAM using SPICE model," *2015 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, 2015, pp. 1425-1430.

[22] D. Ielmini, "Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth," in *IEEE Transactions on Electron Devices*, vol. 58, no. 12, pp. 4309-4317, Dec. 2011.

[23] J. Mcpherson, J.-Y. Kim, A. Shanware, and H. Mogul, “Thermochemical description of dielectric breakdown in high dielectric constant materials,” *Applied Physics Letters*, vol. 82, no. 13, pp. 2121–2123, 2003

[24] H. Y. Lee *et al*., "Low power and high-speed bipolar switching with a thin reactive Ti buffer layer in robust HfO2 based RRAM," *2008 IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 1-4.

[25] S. Yu, Y. Wu, and H.-S. P. Wong, “Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory,” *Applied Physics Letters*, vol. 98, no. 10, p. 103514, Jul. 2011.

[26] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang and H. S. P. Wong, "A neuromorphic visual system using RRAM synaptic devices with Sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling," *2012 International Electron Devices Meeting*, San Francisco, CA, 2012, pp. 10.4.1-10.4.4.

[27] S. Yu, Ximeng Guan and H. S. P. Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," *2011 International Electron Devices Meeting*, Washington, DC, 2011, pp. 17.3.1-17.3.4.

[28] Z. Fang *et al*., "Temperature Instability of Resistive Switching on HfOx-Based RRAM Devices," in *IEEE Electron Device Letters*, vol. 31, no. 5, pp. 476-478, May 2010.

[29] Charles Kittel, Introduction to Solid State Physics, 8th ed. New York, USA: John Wiley & Sons, Inc. 2004.

[30] Predictive Technology Model. [Online]. Available: http://ptm.asu.edu.

[31] MOSIS Scalable CMOS. [Online]. Available: https://www.mosis.com/files/scmos/scmos.pdf

[32] EUROPRACTICE. [Online]. Available: http://www.europractice-ic.com/technologies_UMC.php?tech_id=65nm.

[33] Y. Y. Chen *et al*., "Balancing SET/RESET Pulse for 10^{10} Endurance in HfO_2/Hf 1T1R Bipolar RRAM," in *IEEE Transactions on Electron Devices*, vol. 59, no. 12, pp. 3243-3249, Dec. 2012.

[34] T. W. Lee and J. H. Nickel, "Memristor Resistance Modulation for Analog Applications," in *IEEE Electron Device Letters*, vol. 33, no. 10, pp. 1456-1458, Oct. 2012.

[35] L. Gao, P. Y. Chen and S. Yu, "Programming Protocol Optimization for Analog Weight Tuning in Resistive Memories," in *IEEE Electron Device Letters*, vol. 36, no. 11, pp. 1157-1159, Nov. 2015.

[36] M. Tavakoli and R. Sarpeshkar, "A sinh resistor and its application to tanh linearization," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 536-543, Feb. 2005.

[37] R. Fang, W. Chen, L. Gao, W. Yu and S. Yu, "Low-Temperature Characteristics of HfO_x-Based Resistive Random Access Memory," in *IEEE Electron Device Letters*, vol. 36, no. 6, pp. 567-569, June 2015.

[38] B. Govoreanu, S. Clima, I. P. Radu, Y. Y. Chen, D. J. Wouters and M. Jurczak, "Complementary Role of Field and Temperature in Triggering ON/OFF Switching Mechanisms in Hf/ HfO_2 Resistive RAM Cells," in *IEEE Transactions on Electron Devices*, vol. 60, no. 8, pp. 2471-2478, Aug. 2013.

[39] M. M. Shulaker *et al*., "Monolithic 3D integration of logic and memory: Carbon nanotube FETs, resistive RAM, and silicon FETs," *2014 IEEE International Electron Devices Meeting*, San Francisco, CA, 2014, pp. 27.4.1-27.4.4.

[40] L. Goux et al., “On the gradual unipolar and bipolar resistive switching of TiN\HfO2\Pt memory systems”, Electrochem. Solid State Letter, vol. 13, pp. G54–G56, 2010.

[41] Y. Y. Chen *et al*., "Endurance/Retention Trade-off on HfO_2/Metal Cap 1T1R Bipolar RRAM," in *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 1114-1121, March 2013.

[42] B. Govoreanu *et al*., "10×10nm^2 Hf/HfOx crossbar resistive RAM with excellent performance, reliability and low-energy operation," *2011 International Electron Devices Meeting*, Washington, DC, 2011, pp. 31.6.1-31.6.4.

[43] Zhao, H.-Y. Chen, S.-C. Wu, Z. Jiang, S. Yu, T.-H. Hou, H.-S. P. Wong, and Y. Nishi, “Multi-level control of conductive nano-filament evolution in HfO2 ReRAM by pulse-train operations,” *Nanoscale*, vol. 6, no. 11, pp. 5698–5702, 2014.

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