An Ultra Low-Power Neuromorphic Bandpass Filter for Autonomous Cars

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***Abstract*—An ultra low power neuromorphic bandpass filter (BPF) for dedicated short range communication system is proposed. The filter is designed for an intermediate frequency receiver for a passband of 75 MHz with 37.5 MHz center frequency. In an effort to improve the filter performance without compromising power consumption; a standard R_m-C BPF structure is incorporated within the modified Izhikevich neuron to design the neuromorphic bandpass filter. Implemented in 45 nm CMOS technology, the proposed bandpass filter consumes 100.8 nW at a supply voltage of 0.5 V. The neuromorphic bandpass filter demonstrates excellent figure-of-merit (FOM) of -181.5 dB for a spurious free dynamic range of 27.1 dBm.**

I. Introduction

In the recent years, autonomous car technology has gained lots of interests among potential users, manufacturers, and government agencies. While in the United States each year almost 38,000 deaths occur in car accidents due to human errors, the autonomous car technology can promise to provide better safety and security of human lives by maintaining an integrated sensor and communication environment. As an integral part of the intelligent transportation services (ITS), a dedicated short range communication (DSRC) protocol has been developed worldwide where a 5.9 GHz ISM band is allocated for communication using DSRC service in the USA [1].

The DSRC service is an important step in making autonomous cars safe by establishing a radio link between an on-board equipment (OBE) and roadside equipment (RSE) within a small communication range from 100 m to 1 km. This will enable a vehicle-to-vehicle or vehicle-to-infrastructure communication to avoid a potential accident situation by alerting the autonomous car system to impending hazards-such as a sudden stop of vehicles in front; the location of nearby OBEs and RSEs; anticipating collision paths during merging; acute curves or slippery patches on the road ahead [2].

Traditionally, the low frequency bandpass filters are designed with transconductance-C (Gm-C) filters, operational transconductance amplifiers (OTA), and a switched capacitor [3–5]. Since the high power requirements of the filters discussed earlier do not meet the CMOS power budget, split current sources and log-domain filter topologies have been considered [6], [7]. For high frequency applications such as radio frequency (RF) receivers, the bandpass filters are designed for the intermediate frequency (IF). In recent years, significant strides are made to develop an integrated CMOS DSRC transceiver for Korea/Japan ETCS at 5.8 GHz [8], [9]. The BPFs in these transreceivers are designed for an IF stage with center frequency of around 37.5 MHz with 75 MHz bandwidth alloted in the spectrum. They are realized by using off-chip passive elements for achieving higher channel attenuation ratio, but at the expense of increase in hardware overhead. A band-select on-chip resonance based cascaded BPF is developed in [10] for DSRC system for center frequencies ranging from 27 MHz to 41 MHz with a total power consumption of 14.8 mW.

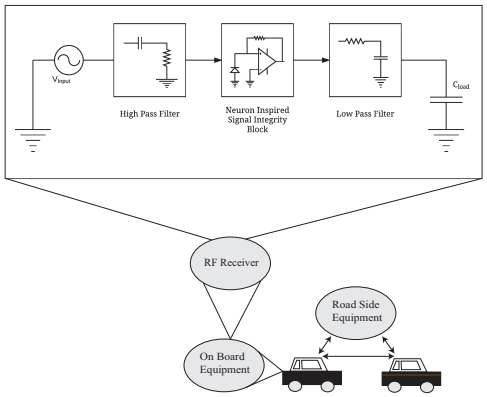

Fig. 1. Symbolic representation of neuron inspired IF band pass filter in an autonomous car.

The paper is organized as follows; section II provides insight on the proposed bandpass filter. The simulation results are discussed in section III. Finally, the paper is concluded in section IV.

II. The Proposed Neuromorphic Bandpass Filter

The symbolic representation of the neuromorphic IF BPF for DSRC system in an autonomous car is shown in Fig. 1. In order to improve the noise performance and the power handling capability of the standard CMOS R_m-C BPF, it is incorporated within a neuron inspired signal integrity block. Figure 2 illustrates the proposed fourth order neuromorphic bandpass filter with a bandwidth of 75 MHz based on the Izhikevich neuron model.

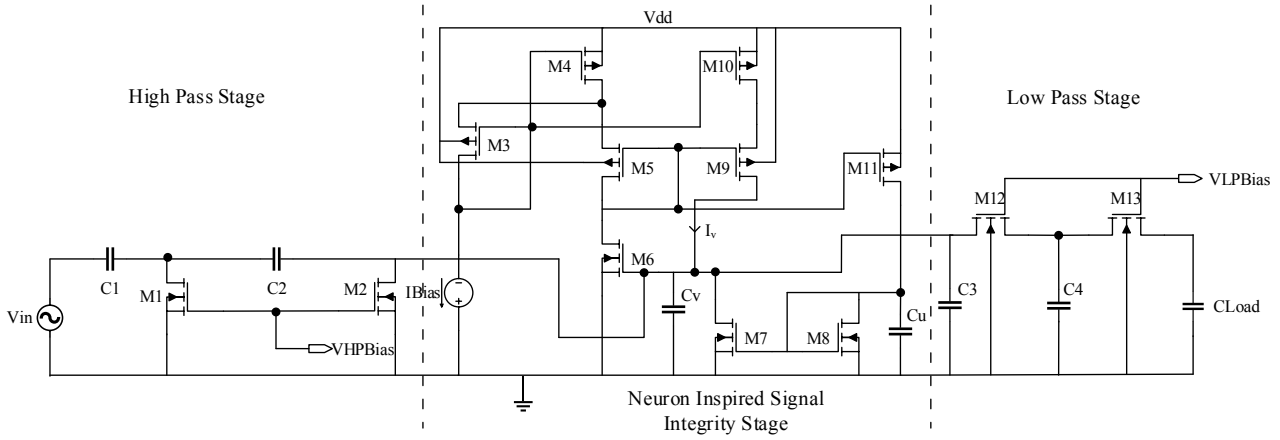

Fig. 2. Circuit diagram of the proposed neuromorphic bandpass filter.

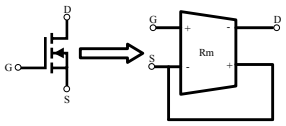

Fig. 3. A MOSFET and its macro model.

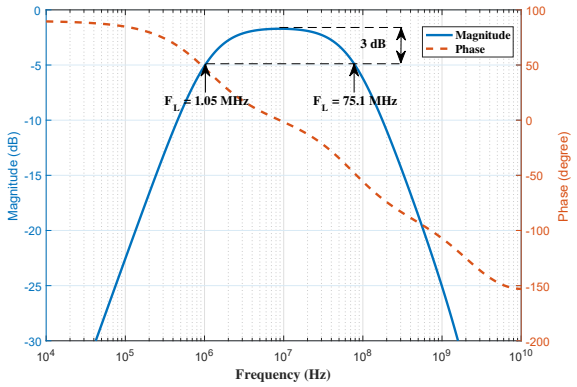

Fig. 4. Magnitude and phase response of the proposed neuromorphic bandpass filter.

A. Proposed Neuromorphic Bandpass Filter Circuit Architecture

Figure 2 shows a 4^{th} order R_m-C BPF topology. The proposed 75 MHz bandwidth BPF is realized using all on-chip components. For realizing a smooth frequency response in a wide band BPF, a higher order cascaded connection is required. Capacitance C1, C2 with MOSFETs M1, M2 and capacitance C3, C4 with MOSFETs M12, M13 are connected in a cascaded manner to generate high-pass and low-pass cutoff frequencies, respectively for the BPF. The simulated magnitude and phase response is shown in Fig. 4. A monotonically decreasing phase response is achieved for the passband.

1) Modeling R_m using a MOSFET: A MOSFET can be modeled as a controlled resistor when V_{DS} is low. A R_m cell connected in a negative feedback manner can be achieved by performing a small signal analysis of the transistor as shown in

TABLE I
COMPARISON OF POWER CONSUMPTION

	CMOS Technology	Power (μW)
This Work	45 nm	0.1
[16]	45 nm	180
[17]	65 nm	48.5×10^3
[18]	65 nm	13.1×10^3
[19]	65 nm	0.9×10^3
[20]	65 nm	28×10^3

Fig. 3. The resistance R_{DS} of the MOSFET depends upon the V_{GS}, i.e. as V_{GS} increases above V_T, R_{DS} decreases and vice versa. This can be intuitively realized by following equation:

$$R_{DS} = \frac{L/W}{\mu_n C_{ox}(V_{GS} - V_T - V_{DS}/2)} \quad (1)$$

where, W and L are the width and length of the MOSFET respectively, $\mu_n C_{ox}$ is a process parameter, V_{GS} is Gate-Source voltage of a MOSFET, V_T is the threshold voltage and V_{DS} is Drain-Source voltage. Hence the R_{DS} value can be altered by changing the gate drive (V_{GS}-V_T) or by changing the W/L ratio of the MOSFET. Thus the BW of the filter can be tuned by changing the operating region of a MOSFETs (M1-M2 and M12-M13) from weak inversion to velocity saturation.

2) Neuron-inspired signal integrity block: Since this structure does not have a high impedance input port, a cascade connection for high order filter realization would require an additional buffer circuit in order to maintain the signal integrity. A Izhikevich neuron inspired signal integrity block is used in this design. Building on the VLSI implementation of the Izhikevich neuron proposed in [12], the proposed design improves the stability of the neuron model by implementing a wide swing cascode current mirror. The output of the high pass stage is used to bias M6 and its size is designed such that it operates in saturation. The current generated by M6 is fed to the wide swing cascode mirror of the membrane circuit and

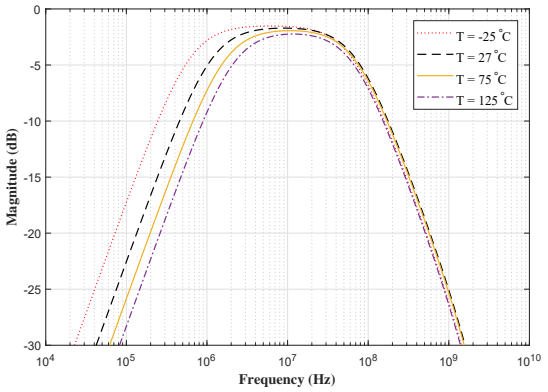

Fig. 5. Magnitude response of the proposed neuromorphic bandpass filter at different operating temperature levels.

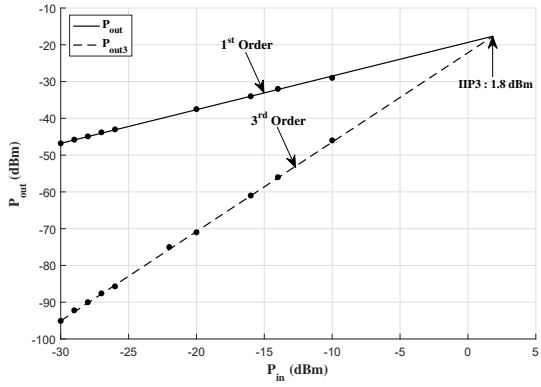

Fig. 6. Extrapolated IIP3 of the filter with two tones of 37.5MHz and 40 MHz at the input.

simple current mirror of the slow variable circuit. The I_{BIAS} in the wide swing current mirror can be set to I_{Dmax} of M6 to ensure the V_{DS} of transistors M4 and M10 force them towards triode region. Since transistor M6 is in saturation, it will fed the current mirrors with a constant current irrespective of small variations at the gate caused by the non linearity in the high pass stage. Hence, the bias current and the size of the transistor M3 can be kept lower in order to save power. This will have no effect on the current densities as the current will be mirrored efficiently even if the V_{min} at the current sink is as low as $2\Delta V$.

The mirrored current (I_v) is used to charge the membrane capacitor C_v as described in section 2A. The size of the C_v is kept smaller for fast charging. Consequently it will discharge fast through transistor M7 even if large M7 is used. The hyper-polarization of C_v can be controlled by biasing M7 with the slow variable circuit. This will assure a stable transfer of the signal from high pass stage to low pass stage, thus improving the noise performance and signal integrity of a traditionally lossy R_m-C bandpass filter.

III. Simulation Results

The circuit proposed in Fig. 2 for a neuromorphic BPF is designed and simulated in a standard 45 nm CMOS technology. The lossy R_m-C filter is incorporated within a modified izhikevich neuron to improve the filter performance without increasing the power consumption. Table I shows the comparison of the neuromorphic filter and stat-of-the art BPF. The proposed on-chip filter for a passband of 75 MHz consumes only 100.8 nW of power for a 0.5 V voltage supply.

In order to verify the stability of the presented BPF, a supply voltage sweep and temperature sweep was performed from 0.5 V to 1 V and from -25^o C to 125^o C respectively. A constant frequency response was observed when supply voltage was varied in the range of 0.5 V to 1 V. The temperature sweep results shown in Fig. 5 records a slight change in lower cutoff frequency. A variation in insertion loss of 1.71 $\pm$ 0.5 dB can be observed. This fluctuation in lower cutoff frequency and insertion loss is due to high sensitivity of 45 nm standard process CMOS transistors towards Process-Voltage-Temperature (PVT) variations.

Figures 6 and 7 demonstrate the results of a two tones input test. For input tones of 35 MHz and 37.5 MHz with P_{in} of -30 dBm, an IIP3 of 1.8 dBm is observed. It is clearly seen in Fig. 7 that the 2^{nd} and 3^{rd} order harmonics of the input tones are suppressed. Based on a Monte-Carlo simulation, see Fig. 8, the average input-referred noise is 130 nV_{rms} with a standard deviation σ of 25.9 nV_{rms}. In addition, another metric to assess the filter's performance is the figure-of-merit (FOM), which is given as [13]:

$$FOM = 10log\left(\frac{P_{cons} * V_{dd}}{N * F_c * SFDR}\right) \quad (2)$$

where, P_{cons} is the power consumption, V_{dd} is the supply voltage, N is the order of the filter, F_c is the center frequency, and SFDR is the spurious free dynamic range. The SFDR of the proposed architecture is 27.1 dBm. An excellent FOM of -181.5 dB was achieved for the proposed neuromorphic BPF. Table II summarizes the comparison between simulated results of the proposed neuromorphic BPF architecture and measured as well as simulated results of recent peer reviewed work for BPF over various performance parameters.

IV. Conclusion

A neuromorphic bandpass filter with 75 MHz passband for IF stage in a DSRC system of an autonomous car is realized. In a standard 45 nm CMOS technology, the proposed neuron inspired R_m-C BPF consumes only 100.8 nW power for a supply voltage of 0.5 V. For a 37.5 MHz center frequency, a passband ripple of 1 dB is observed. Experimental results demonstrates the stability of the system over various parameters. A monte carlo simulation reveals the average input-referred noise is 130 nV_{rms} with a standard deviation of 25.9 nV_{rms}. A figure of merit of -181.5 dB is reported for a dynamic range of 60 dB.

Acknowledgement

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TABLE II
COMPARISON OF FILTER PERFORMANCE PARAMETERS

Parameters	This Work	[16]	[17]	[18]	[19]	[20]
Supply Voltage (V)	0.5	0.75	1.2	1.2	2.5	1.2
F_c (MHz)	38	1000	70	80	4.1-20.4	20-100
IIP3 (dBm)	1.8	-	31.5	2	25	0
BW (MHz)	75	-	22	10	5	24-125
Passband Gain (dB)	-1.71	1	0	2	0	0
Order	4	2	5	4	3	6

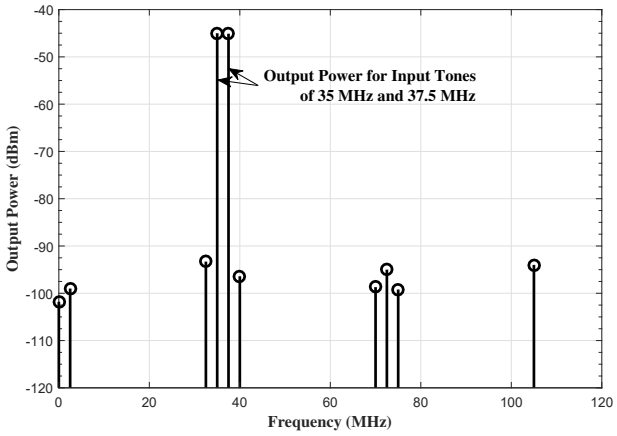

Fig. 7. Output power spectrum for input dual tones of 35 MHz and 37.5 MHz with -30 dBm P_{in}.

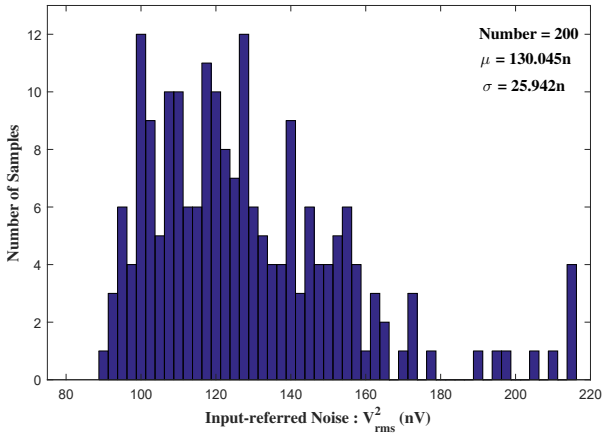

Fig. 8. Monte Carlo simulation for Input-referred Noise.

REFERENCES

[1] *Dedicated Short Range Communications (DSRC) Service* [online]. Available : https://www.fcc.gov/wireless/bureau-divisions/mobility-division/dedicated-short-range-communications-dsrc-service

[2] *DSRC: The Future of Safer Driving* [online]. Available: https://www.its.dot.gov/factsheets/dsrc_factsheet.htm

[3] W. M. Snelgrove, and A. Shoval, "A balanced 0.9 pm CMOS transconductance-C filter tunable over the VHF range," *IEEE J. Solid-state Circuits*, vo1.27, pp.3 14-323, March 1992.

[4] C. Salthouse and R. Sarpeshkar, "A practical micropower programmable bandpass filter for use in bionic ears, " *IEEE Journal of Solid-State Circuits*, vol. 38, no. I, pp. 63-70, Jan. 2003.

[5] P. Corbishley and E. Rodriguez-Villegas, "A nanopower bandpass filter for detection of an acoustic signal in a wearable breathing detector, " *IEEE Transactions on Biomedical Circuits and Systems*, vol. I, no. 3, pp. 163-171, Sept. 2007.

[6] S.-c. Lee, S.-Y. Lee, and C.-H. Chiang, "0. 9 v low-power switchedopamp switched-capacitor bandpass filter for electroneurography acquisition systems, " *Circuits, Devices Systems, IET*, vol. 2, no. 2, pp. 257-263, April 2008.

[7] M. van de Gevel, *et. al.*, "Low-power mos integrated filter with transconductors with spoilt current sources, " *IEEE Journal of Solid-State Circuits*, vol. 32, no. 10, pp. 1576-1581, Oct. 1997.

[8] S. Shin, *et. al.*, "0.18 μm CMOS integrated chipset for 5.8 GHz DSRC systems with 10 dBm output power," in *Proc. IEEE Int. Sym. Circuits Systems*, May 2008, pp. 1958-1961.

[9] Kuduck Kwon *et al.*," A 5.8 GHz Integrated CMOS Dedicated short Range Communication Transceiver for the Korea/Japan Electronic Toll Collection System", *IEEE Trans. on MTT*, Vol.58, No.11, pp.2751-2763, Nov. 2010.

[10] H. W. Lin, J. Y. Lin and M. T. Chuang, "A low-area digitalized channel selection filter for DSRC system," *2014 International Symposium on VLSI Design, Automation and Test*, Hsinchu, 2014, pp. 1-4.

[11] E. M. Izhikevich, "Simple model of spiking neurons," *IEEE Trans. Neural Network*, vol. 14, no. 6, pp. 1569-1572, 2003.

[12] J. H. B. Wijekoon and P. Dudek, "Simple analogue VLSI circuit of a cortical neuron," in *13th IEEE International Conference on Electronics, Circuits and Systems*, 2006, pp. 1344-1347.

[13] C. Sawigun, W. Ngamkham, and W. Serdijn, "A 2. 6nw, 0. 5v, 52db-dr, 4th-order gm-c bpf: Moving closer to the fom's fundamental limit, " in *IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 656-659, May 2012.

[14] L. Ye, *et. al.*, "Highly Power-Efficient Active-RC Filters With Wide Bandwidth-Range Using Low-Gain PushPull Opamps," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 95-107, Jan. 2013.

[15] M. De Matteis, *et. al.*, "A 54dB-DR 1-GHz-bandwidth continuous-time low-pass filter with in-band noise reduction," *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, Beijing, 2013, pp. 1280-1283.

[16] D. Dheer, *et. al.*, "A current-mode biquad filter for Zigbee applications using 45nm $\pm$0.75V CMOS CDTA," *2014 IEEE International Symposium on Signal Processing and Information Technology (ISSPIT)*, Noida, 2014, pp. 131-136.

[17] Ying-Hang Wu, *et.al.*, "A high linearity active-RC BPF with 70MHz center frequency and 22MHz bandwidth in 65nm CMOS," *13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT),* Hangzhou, 2016, pp. 1375-1377.

[18] H. Le-Thai, *et. al.*, "An IF Bandpass Filter Based on a Low Distortion Transconductor," in *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2250-2261, Nov. 2010.

[19] Y. Xu, B. Chi, *et. al.*, "Power-Scalable, Complex Bandpass/Low-Pass Filter With I/Q Imbalance Calibration for a Multimode GNSS Receiver," in *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 59, no. 1, pp. 30-34, Jan. 2012.

[20] I. Madadi, M. Tohidian and R. B. Staszewski, "Analysis and Design of I/Q Charge-Sharing Band-Pass-Filter for Superheterodyne Receivers," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 8, pp. 2114-2121, Aug. 2015.