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Two-Dimensional/Three-Dimensional Schottky Junction Photovoltaic Devices Realized by the Direct CVD Growth of vdW 2D $PtSe_2$ Layers on Silicon

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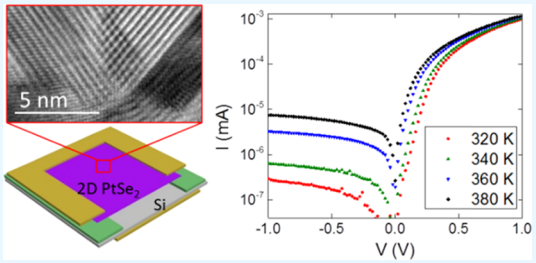
ABSTRACT: Two-dimensional (2D) platinum diselenide ($PtSe_2$) layers are a new class of near-atom-thick 2D crystals in a van der Waals-assembled structure similar to previously explored many other 2D transition-metal dichalcogenides (2D TMDs). They exhibit distinct advantages over conventional 2D TMDs for electronics and optoelectronics applications such as metallic-to-semiconducting transition, decently high carrier mobility, and low growth temperature. Despite such superiority, much of their electrical properties have remained mostly unexplored, leaving their full technological potential far from being realized. Herein, we report 2D/three-dimensional Schottky junction devices based on vertically aligned metallic 2D $PtSe_2$ layers integrated on Si wafers. We directly grew 2D $PtSe_2$ layers of controlled orientation and carrier transport characteristics via a low-temperature chemical vapor deposition process and investigated 2D $PtSe_2$/Si Schottky junction properties. We unveiled a comprehensive set of material parameters, which decisively confirm the presence of excellent Schottky junctions, i.e., high-current rectification, small ideality factor, and temperature-dependent variation of Schottky barrier heights. Moreover, we observed strong photovoltaic effects in the 2D $PtSe_2$/Si Schottky junction devices and extended them to realize flexible photovoltaic devices. This study is believed to significantly broaden the versatility of 2D $PtSe_2$ layers in practical and futuristic electronic devices.



KEYWORDS: *2D layers, 2D $PtSe_2$, 2D heterojunction, 2D/3D mixed dimensionality, 2D photovoltaics*

INTRODUCTION

Two-dimensional (2D) transition-metal dichalcogenides (TMDs) are a group of compounds in the form of MX_2, (M: transition metals, X: chalcogens) assembled by weak van der Waals (vdW) bonding exhibiting exotic optical and electrical properties. Among them, molybdenum- (Mo) and tungsten (W)-based disulfides (MoS_2 and WS_2) or diselenides ($MoSe_2$ and WSe_2) have gained significant interest in the recent developments of 2D TMDs.[1−7] Generally semiconducting in nature, 2D TMDs exhibit enhanced light−matter interaction and band-gap tunability with varying 2D layer numbers projecting exciting applications in electronics and optoelectronics.[8−10] Moreover, they present extraordinary mechanical flexibility in comparison to traditional thin-film inorganic semiconductors, rendering vast opportunities toward devising futuristic devices of unconventional forms.[10,11] Despite such advantages, some critical limitations concerning their material properties and preparation methods hinder their widespread utilization for practical technologies. For instance, their carrier mobilities are inferior to those of traditional semiconductors (e.g., silicon or III−V compounds),[4,8,9] which further degrade when they are synthetically grown via scalable routes such as chemical vapor deposition (CVD).[12,13] Recently, a new type of 2D crystals based on noble metals such as platinum (Pt) has been discovered, which includes $PtSe_2$, PtS_2, and $PtTe_2$.[14−16] Among them, 2D $PtSe_2$ is particularly gaining increasing attention due to distinguishable property advantages over Mo- or W-based 2D TMDs. First, its theoretically predicted carrier mobility at room temperature is >1000 $cm^2/(Vs)$,[17,18] which is much higher over 2D MoS_2[19] and is even comparable to black phosphorus (BP).[18,20,21] Unlike BP, which is prone to very rapid air oxidation and its associated property degradation, 2D $PtSe_2$ is highly stable in ambient conditions.[18,22] More interestingly, it presents a size-dependent transition of carrier transport properties with a dimensional reduction from bulk to monolayer; i.e., 2D $PtSe_2$ of large layer number exhibits strong metallic carrier transport,[15,20,23] which transitions to semiconducting as it gets close to mono- or a few layers. Recently, developed CVD strategies employing the thermal selenization of elemental Pt

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have yielded the growth of 2D $PtSe_2$ layers at 400 °C,[24−26] much lower than what has been demanded for the growth of Mo- or W-based 2D TMDs.[2,27,28] Despite these proven property and manufacturing advantages uniquely inherent to 2D $PtSe_2$ layers, much of their electrical properties have remained largely unexplored, leaving their full technological potential far from being realized. For example, the strong metallic nature of 2D $PtSe_2$ layers projects metal/semiconductor Schottky junction based on "mixed-dimensional" vdW heterostructures[29] when they are interfaced with three-dimensional (3D) semiconductors. The most well-established form of 2D/3D vdW heterostructure-based Schottky junctions can be found in graphene/semiconductor heterojunctions such as mechanically integrated graphene on top of silicon (Si). Although these graphene/Si Schottky junctions are recently gaining significant interest in a variety of electronic applications such as photovoltaic devices,[30,31] their preparation requires the mechanical separation of high-temperature CVD-grown graphene from growth substrates (e.g., copper (Cu)) and its subsequent transfer to Si wafers.[32−34] Accordingly, the process stands a high chance of introducing unwanted contamination throughout the chemical/mechanical treatment of graphene for delamination and integration.

In this article, we demonstrate 2D/3D vdW heterostructure-based Schottky junctions of mixed dimensionality by combining 2D $PtSe_2$ layers with 3D Si substrates. We directly grew metallic 2D $PtSe_2$ layers on lightly doped Si wafers at 400 °C and investigated Schottky junction properties. We verified a comprehensive set of material parameters, which define excellent Schottky junction characteristics, i.e., small ideality factor, large current rectification, and temperature-dependent variation of Schottky barrier heights. Moreover, we observed strong photovoltaic effects in these 2D $PtSe_2$/3D Si Schottky junction devices.

RESULTS AND DISCUSSION

Figure 1 describes the schematic of a 2D $PtSe_2$/3D Si Schottky junction device and its associated fabrication process steps. Figure 1a illustrates that the device is composed of 2D $PtSe_2$ layers intimately interfaced with a patterned Si wafer contacted with gold (Au) electrodes. Two-dimensional $PtSe_2$ layers are directly grown on Si in a vertical orientation via the CVD selenization of Pt as previously reported.[35] Figure 1b shows the step-by-step procedure to fabricate a 2D $PtSe_2$/Si Schottky junction device. A lightly doped Si wafer is selectively deposited with silicon dioxide (SiO_2) through a shadow mask by electron beam evaporation (deposition rate: ∼0.5 Å/s), which defines an open Si area of 0.25 cm^2. Pt film of controlled thickness is deposited by electron beam evaporation (deposition rate: ∼0.1 Å/s) through another shadow mask, resulting in both Pt/Si (active area) and Pt/SiO_2 (electrode area) interfaces. The prepared Pt-deposited Si wafer is placed in the center of a quartz tube CVD furnace with a preloaded alumina boat containing selenium powders at the furnace upstream side. The CVD furnace is pumped down to a base pressure of ∼1 mTorr, followed by purging with argon (Ar) gas to remove any residual impurities inside the quartz tube. Subsequently, it is heated up to 400 °C in 50 min for a dwell time of 50 min under a continuous flow of Ar gas. After the CVD reaction, the furnace is naturally cooled down to room temperature, and the conversion of Pt to 2D $PtSe_2$ layers is confirmed by a noticeable color change in the Pt-deposited area. Finally, the top and bottom Au electrodes are deposited

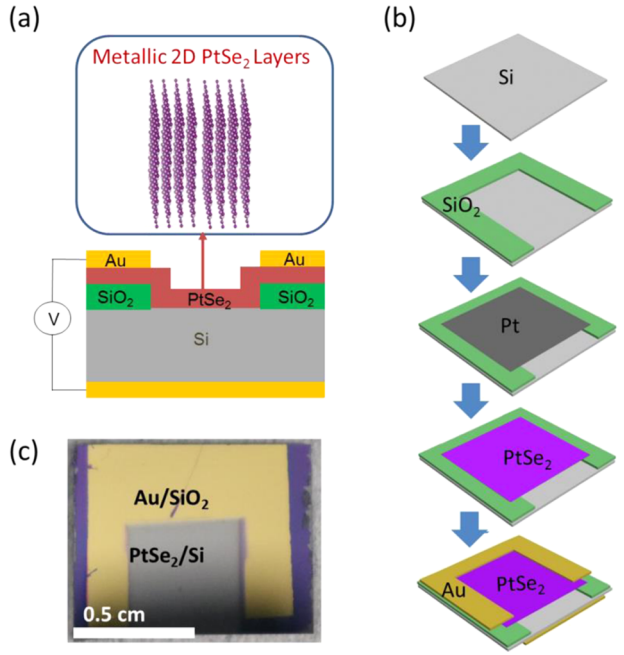

Figure 1. Fabrication of 2D $PtSe_2$/Si Schottky devices. (a) Schematic of a 2D $PtSe_2$/Si Schottky device based on vertically aligned 2D $PtSe_2$ layers. (b) Illustration of step-by-step procedures to fabricate a 2D $PtSe_2$/Si Schottky device. (c) Representative image of a completed 2D $PtSe_2$/Si Schottky device.

on the top (2D $PtSe_2$/SiO_2) and the bottom (bare Si) sides of the wafer, respectively. Figure 1c shows a photograph image of a complete 2D $PtSe_2$/Si Schottky junction device. It is worth mentioning that the low growth temperature of 400 °C for 2D $PtSe_2$ layers is comparable to the thermal budget back-end-of-line temperature adopted in complementary metal-oxide semiconductor (CMOS) processes,[36] indicating potential advantages of CMOS-compatible large-scale manufacturing.

Microstructures and atomic-bonding natures of the 2D $PtSe_2$ layers directly grown on Si wafers were characterized by transmission electron microscopy (TEM) and Raman spectroscopy. We have previously identified that two distinguishable 2D layer orientations of horizontal and vertical can be achieved by CVD-selenizing Pt films of controlled thickness;[35] horizontally aligned 2D $PtSe_2$ layers are grown by the CVD selenization of thin Pt (typically <1 nm), while vertically aligned 2D layers are achieved with thick Pt (typically >4 nm). In this work, we have deliberately grown vertically aligned 2D $PtSe_2$ layers only as they present strong metallic transports suitable for Schottky junction formation—details are to be confirmed in the next section. Figure 2a,b shows low-magnification and high-resolution scanning TEM (HR-STEM) images of vertically aligned 2D $PtSe_2$ layers, respectively. The HR-STEM image in Figure 2b reveals that vertically aligned 2D $PtSe_2$ layers expose their 2D layer edges on the surface consistent with previous studies,[35] indicating the good morphological controllability of our CVD process. Figure 2c shows the Raman spectra of vertically aligned 2D $PtSe_2$ layers exhibiting two characteristic peaks corresponding to in-plane E_g and out-of-plane A_{1g} vibration modes.[25] It is noted that vertically aligned 2D $PtSe_2$ layers exhibit E_g and A_{1g} peaks of comparable intensity, indicating a significant enhancement of out-of-plane vibration, similarly observed with vertically aligned 2D MoS_2 layers.[27] Figure 2d shows a cross-sectional

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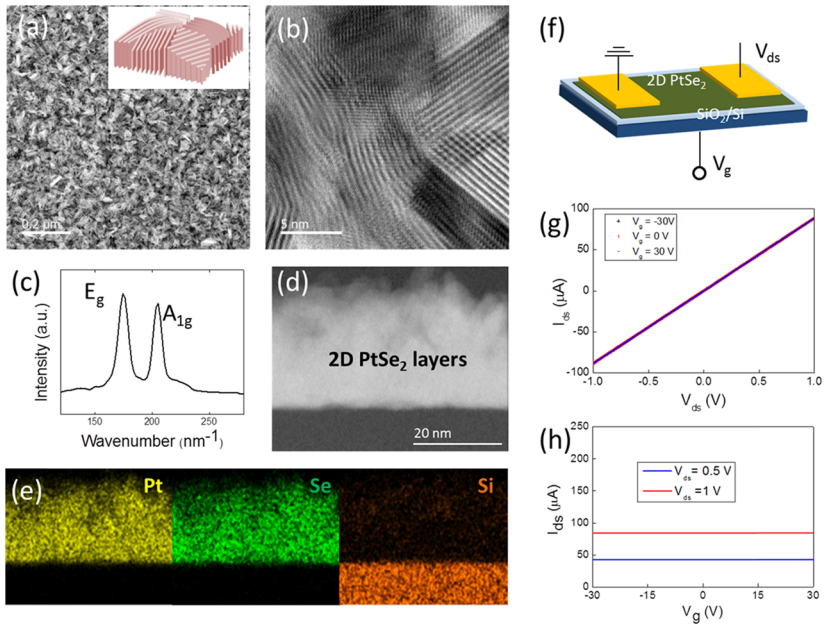

Figure 2. Structural, chemical, and electrical characterizations of vertically aligned 2D $PtSe_2$ layers. (a–e) Structural and chemical characterizations: (a, b) TEM characterization of vertically aligned 2D $PtSe_2$ layers in (a) low-magnification and (b) high-magnification views. (c) Raman spectroscopy characterization. (d) Cross-sectional STEM image of vertically aligned 2D $PtSe_2$ layers. (e) STEM–EDS elemental mapping images corresponding to (d). (f–h) Electrical characterization. (f) Schematic of a back-gated FET device based on vertically aligned 2D $PtSe_2$ layers. (g) I_{ds}–V_{ds} FET transfer characteristics. (h) I_{ds}–V_g FET transfer characteristics.

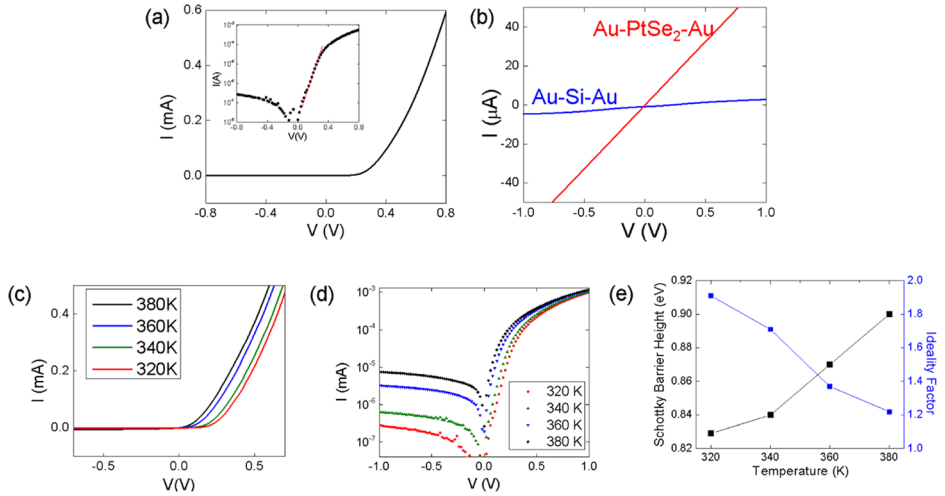

Figure 3. Characterization of Schottky junction characteristics in 2D $PtSe_2$/Si devices. (a) I–V characteristics of a 2D $PtSe_2$/Si Schottky junction device. The inset presents the corresponding semilog plot. (b) I–V characteristics from only-2D $PtSe_2$ layers and only-Si wafers without 2D $PtSe_2$/Si junctions obtained with Au contacts. (c) I–V characteristics with varying temperature in a range of 320–380 K. (d) Semilog plots corresponding to (c). (e) Temperature-dependent Schottky barrier height and ideality factor.

STEM image of vertically aligned 2D $PtSe_2$ layers on a growth substrate, indicating that they are ~30 nm thick. Figure 2e shows the corresponding energy-dispersive X-ray spectroscopy (EDS) elemental mapping images, revealing the spatial distribution of Pt, Se, and Si. Having carried out the structural and chemical analyses of vertically aligned 2D $PtSe_2$ layers, we then investigated their electrical properties to assess their suitability for Schottky junction formation. We fabricated field-effect transistors (FETs) employing 2D $PtSe_2$ layers as active channels and identified their carrier transport types by characterizing FET back-gate responses, as illustrated in Figure 2f. Figure 2g,h shows the FET transfer characteristics of drain–source current vs. voltage (I_{ds}–V_{ds}) with varying gate voltage (V_g) and I_{ds} as a function of V_g (I_{ds}–V_g) with varying V_{ds} obtained from vertically aligned 2D $PtSe_2$ layers, respectively. We note that the vertically aligned 2D $PtSe_2$ layers do not exhibit any FET gate responses, indicating they are highly metallic; i.e., transfer characteristics of I_{ds}–V_{ds} completely overlap irrespective of V_g (Figure 2g) and I_{ds} does not change as a function of V_g (Figure 2h), consistent with our previous studies.[35]

Figure 3 presents the electrical characterization results of 2D $PtSe_2$/Si Schottky junction devices. Figure 3a shows the two-terminal current–voltage (I–V) characteristics of a 2D $PtSe_2$/Si Schottky junction device measured with Au contacts, as shown in Figure 1a. The device exhibits asymmetric rectifying

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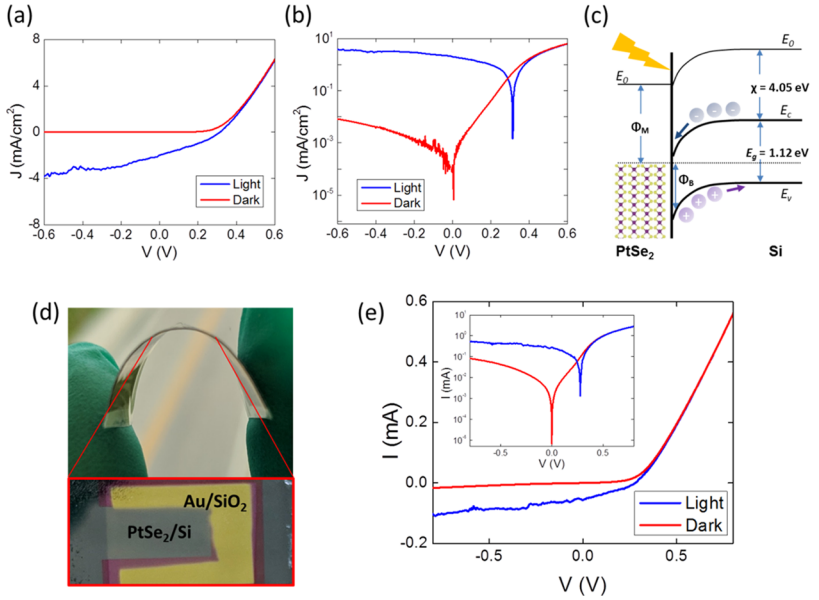

Figure 4. Photovoltaic characteristics of 2D $PtSe_2$/Si devices. (a, b) $J-V$ characteristics of a 2D $PtSe_2$/Si Schottky junction device in dark (red) and under illumination (blue) in (a) linear and (b) semilog scales. (c) Representative band diagram of a 2D $PtSe_2$/Si Schottky junction under zero bias. (d) Photo image of a flexible 2D $PtSe_2$/Si Schottky junction device. (e) $I-V$ characteristics of the device in (d) in dark (red) and under illumination (blue). The inset presents the corresponding characteristics on a semilog scale.

$I-V$ characteristics with a high rectification ratio of $>10^3$ as manifested in the corresponding semilog plot in the inset. Moreover, from the linear tangential (red slope) to the semilog plot belonging to a forward bias regime, a diode ideality factor, n, can be extracted and it is found to be ~1.9. Details for the ideality factor extraction are presented in the next section. The deviation of n from unity indicates that the device performance is presently impaired by recombination of majority carriers, which is most likely attributed to unoptimized device process conditions. To confirm that the observed current rectification indeed reflects Schottky junction characteristics, we separately characterized the $I-V$ characteristics of only-2D $PtSe_2$ layers and only-Si wafers without 2D $PtSe_2$/Si junctions. Figure 3b reveals that both 2D $PtSe_2$ layers and Si wafers exhibit highly symmetric Ohmic transport characteristic with Au contacts, which decisively confirms that the observed rectification originates from the 2D $PtSe_2$/Si junction. To better understand the underlying transport mechanism of 2D $PtSe_2$/Si Schottky junction devices, we employed temperature-variant $I-V$ measurements. Figure 3c presents the variation of $I-V$ characteristics under varying temperature, revealing an increase of current in the forward bias regime with increasing temperature. Figure 3d shows the semilog plots of the corresponding $I-V$ characteristics with varying temperature. In addition to the increase of current in the forward bias regime, it is observed that there is a significant increase (>50 times) of current in the reverse bias regime as temperature increases from 320 to 380 K. Such a temperature-dependent increase of current indicates the thermal excitation of electrons within semiconducting Si, reflecting an increase of carrier concentration in its conduction band..[37,38] From these temperature-dependent $I-V$ plots, we further extract important material parameters, which define the performances of the Schottky junction devices; i.e., Schottky barrier height, Φ_B, and ideality factor, n. According to thermionic emission theory,[39] the current, I, through a Schottky diode is expressed as

$$I = I_0 \exp\left(\frac{q(V-IR_s)}{nKT}\right) \quad (1)$$

Here, I_o is the reverse saturation current, which can be modeled as

$$I_0 = AA^{**}T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \quad (2)$$

Here, q is the charge of an electron, A^{**} is the Richardson constant for Si, A is the active diode surface area, T is the absolute temperature, k is the Boltzmann constant, R_s is the series resistance, and V is the voltage applied across the diode. Moreover, the diode equation can be re-expressed as[40]

$$\frac{dV}{d(\ln J)} = IR_s + n\left(\frac{kT}{q}\right) \quad (3)$$

where $J = I/A$, Then

$$IR_s + n\Phi_B = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^{**}T^2}\right) \quad (4)$$

Figure 3e presents the variation of Φ_B and n as a function of temperature extracted from the above equation, revealing that Φ_B increases with increasing temperature. The observation is consistent with previous studies on similarly structured 2D/3D Schottky junction devices such as graphene/Si,[41] indicating that current density is dominated by thermal excitation rather than Φ_B. Meanwhile, n decreases with increasing temperature, indicating diminished carrier recombination possibly due to the thermal annihilation of structural defects at 2D $PtSe_2$/Si interfaces. Moreover, the room-temperature series resistance was determined to be ~529 Ω extracted from eq 3, which is consistent with previous studies.[25,42]

We investigated the photovoltaic properties of 2D $PtSe_2$/Si Schottky junction devices by measuring their photoresponsiveness. Figure 4a demonstrates the current density–voltage ($J-$

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V) characteristics of a 2D $PtSe_2$/Si junction device in dark (red) and under illumination (blue). Upon illumination with a 400 W/m^2 illumination source, the device exhibits a significant photovoltaic effect as manifested by a generation of reverse current density. Figure 4b shows the semilog plot of the corresponding J–V characteristics better demonstrating photovoltaic device parameters, i.e., open-circuit voltage V_{oc} and short-circuit current density J_{sc}. By analyzing both Figure 4a,b, we extract $V_{oc} \sim 0.35$ V, fill factor (FF) of ~26%, and $J_{sc} \sim 4$ mA/cm^2, which leads to a power conversion efficiency (PCE) of ~1%. Figure 4c describes a diagram of the energy band bending formed at the 2D $PtSe_2$/Si Schottky junction, which justifies that the generation of photoexcited carriers is responsible for the observed photovoltaic effect under zero bias. The band-bending diagram is constructed based on the room-temperature Φ_B, and the electron affinity (χ) and band gap (E_g) of Si known from the literature.[43] E_c and E_v are the conduction band edge and the valence band edge of Si, respectively. We note that the operational principle of 2D $PtSe_2$/Si Schottky junction photovoltaics is, in principle, similar to those of other metallic 2D layers/Si-based systems. The most extensively studied one is graphene/Si heterojunction devices whose initial PCE were ~1.5% in 2010,[33] comparable to that of 2D $PtSe_2$/Si. Since then, significant efforts have been made to further improve the PCE of graphene/Si devices by engineering their intrinsic electronic/physical structures; these efforts include adjusting band offsets and heterojunction interfaces, as well as incorporating light-trapping structures.[44] P-type doping of graphene can increase FF by reducing its sheet resistance, as well as increasing its work function (thus, Schottky barrier), as previously reported.[32,45] Additionally, light-trapping materials and passivation layers have been incorporated to reduce light reflection from Si surface, as well as to improve graphene/Si interfacial morphology, respectively.[46,47] The highest PCE of graphene/Si Schottky junction photovoltaics is now up to 16.2%,[48] reflecting a drastic improvement over the last several years. Considering the similarity of their operational principle, we project that the photovoltaic performances of 2D $PtSe_2$/Si Schottky junction devices can also be significantly improved by employing those engineering schemes developed for graphene/Si systems. The fabrication of photovoltaic Schottky junctions via a direct growth of metallic 2D $PtSe_2$ layers on Si can be further extended to realize 2D $PtSe_2$/Si flexible photovoltaic devices. 2D $PtSe_2$ layers were directly grown on thin Si wafers (thickness <50 μm), which were prepared by potassium hydroxide (KOH) etch followed by the device fabrication procedure described in Figure 1b. Details for the KOH etching of Si are presented in the Method section. Figure 4d shows a camera image of a 2D $PtSe_2$/Si flexible device under mechanical bending, as well as its device components described in the inset. Figure 4e presents the I–V characteristics of the same device without bending in dark (red) and under illumination (blue), as well as the corresponding semilog plot in the inset. The device exhibits a significant photovoltaic effect with $V_{oc} \sim 0.28$ V, $I_{sc} \sim 0.282$ mA/cm^2, and FF ~ 28.75%.

We further evaluated the photovoltaic performances of 2D $PtSe_2$/Si photovoltaic devices under mechanical deformation. A flexible 2D $PtSe_2$/Si photovoltaic device was tested under a systematic application of controlled bending; it first underwent 100 bending cycles at a bending radius of $R1$ = 9.43 mm and subsequently underwent another 100 bending cycles at a bending radius of $R2$ = 5.95 mm (Figure 5a–f). Characteristics of current density vs. voltage (J–V) were obtained after 0th, 10th, and 100th bending cycles at each radius. Figure 5a shows an image of the device at a bending radius, $R1$. Figure 5b,c represents J–V curves obtained before and after the first 100 bending cycles at $R1$, respectively, revealing good retention of significant photovoltaic effects. Figure 5d shows an image of the same device at a bending radius, $R2$, after the bending shown in Figure 5b,c. Figure 5e,f represents J–V curves obtained before and after the first 100 bending cycles at $R2$, respectively. We extract J_{sc} and V_{oc} for each bending radius and present them as a function of bending cycles in Figure 5g,h, respectively. We note that V_{oc} remains nearly constant, while J_{sc} slightly decreases with increasing bending cycles possibly due to a pronounced generation of charge recombination sites within 2D $PtSe_2$ layers. The measurements were carried out under an AM 1.5 solar spectral irradiance with an intensity of 245 W/m^2.

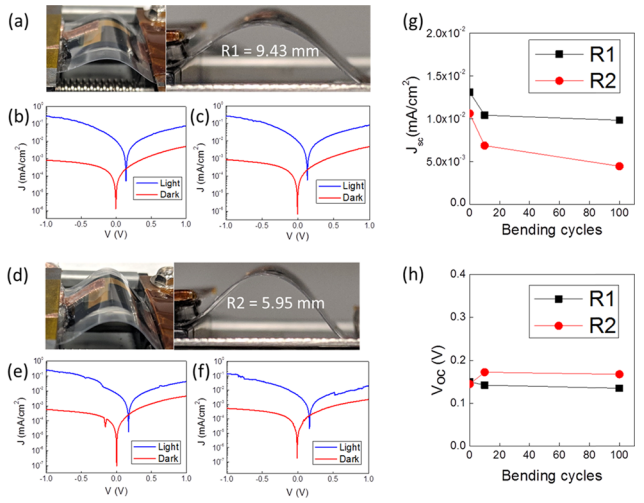

Figure 5. Flexible photovoltaic 2D $PtSe_2$/Si devices. (a–c) Photovoltaic responses before/after repeated bending at a bending radius of $R1$ = 9.43 mm. (a) Corresponding image. (b) Photovoltaic characteristics before bending. (c) Photovoltaic characteristics after 100 times bending at $R1$. (d–f) Photovoltaic responses before/after repeated bending at a bending radius of $R2$ = 5.95 mm. (d) Corresponding image. (e) Photovoltaic characteristics before bending. (f) Photovoltaic characteristics after 100 times bending at $R2$. (g) J_{sc} with varying bending cycles. (h) V_{oc} with varying bending cycles.

Finally, we provide a table to overview previous studies on 2D $PtSe_2$ layer-based heterojunctions, emphasizing novel aspects of this study. Table 1 summarizes recent progresses in the development of 2D $PtSe_2$ layer-based heterojunction materials and devices, as well as their associated fabrication approaches. The table highlights that studies on 2D $PtSe_2$/Si Schottky junction for flexible photovoltaics have not been previously explored.

CONCLUSIONS

In summary, we have directly grown 2D $PtSe_2$ layers of controlled morphological orientation and carrier transport on Si wafers and fabricated 2D $PtSe_2$/Si heterojunction devices. With vertically aligned 2D $PtSe_2$ layers of metallic transports interfaced with Si, we have identified pronounced Schottky junction characteristics such as high-current rectification ratio, temperature-dependent barrier height, and diode ideality

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Table 1. Overview of Recent Studies on 2D $PtSe_2$ Layer-Based Heterojunctions

material	application	method	heterojunction type	ref
$PtSe_2$/Si	photodetection/photovoltaics	CVD growth and mechanical transfer	2D/3D	25
$PtSe_2$/Si	wide spectral photoresponse	CVD growth and mechanical transfer	2D/3D	50
$PtSe_2$/Si	broad-band photodetection	direct CVD growth	2D/3D	26
$PtSe_2$/Si nanowire	broad-band photodetection	CVD growth and mechanical transfer	2D/1D	42
$PtSe_2$/CdTe	broad-band photodetection	CVD growth and mechanical transfer	2D/3D	51
$PtSe_2$/GaAs	broad-band photodetection	CVD growth and mechanical transfer	2D/3D	52
$PtSe_2$/Perovskite	broad-band photodetection	CVD growth and solution drop-casting	2D/3D	53
$PtSe_2$/GaN	deep UV photodetection	direct CVD growth	2D/3D	54
$PtSe_2$/Ge	photovoltaics/photodetection	CVD growth and mechanical transfer	2D/3D	55
$PtSe_2$/MoS_2	p−n junction devices	CVD growth and mechanical transfer	2D/2D	56
$PtSe_2$/PtS_2	broad-band photodetection	direct CVD growth	2D/2D	57
$PtSe_2$/Si	flexible photovoltaics	direct CVD growth	2D/3D	this work

factors. Such intrinsic Schottky junction characteristics lead to significant photovoltaic effects upon light illumination, suggesting a technological versatility and promise of these 2D/3D electronic junctions.

METHOD

Flexible 2D $PtSe_2$/Si Device Fabrication. Si wafers (initial thickness of ∼180 μm) were submerged into a 30% wt KOH solution at 90 °C until their thickness reached down to ∼20 μm, following the established KOH-etching recipe.[49] The remaining fabrication procedures including SiO_2 deposition and 2D $PtSe_2$ layer growth were carried out as instructed in Figure 1b.

TEM and Raman Characterization. Microstructure analysis of 2D $PtSe_2$ layers was performed with a JEOL ARM 200 F Cs-corrected TEM at an operation voltage of 200 kV. For plane-view TEM sample preparation, BOE was directly applied to 2D $PtSe_2$ layer-grown SiO_2/Si wafers, and the delaminated 2D $PtSe_2$ layers were directly transferred onto copper TEM grids by mechanical scooping. For Raman spectroscopy characterization, a Renishaw RM 1000B system with a laser source of 514 nm wavelength was used.

Room-Temperature Electrical and Photovoltaic Characterizations. All electrical measurements were performed with a home-built probe station using a HP 4156 A semiconductor parameter analyzer. Photovoltaic measurements were carried out using an AM 1.5 G solar simulator (G2V optics) under 400 W/m^2 intensity. For the bending cyclic tests, flexible 2D $PtSe_2$/Si photovoltaic devices were laminated onto self-sealing polyethylene terephthalate sheets (25 μm thickness). Conductive copper tapes were attached to the front/back contacts of the devices for electrical measurements.

Variant Temperature Electrical Measurement. For temperature-dependent electrical measurements, devices were probed under vacuum inside a Janis research ST-500-UHT micromanipulated probe station, and the temperature was varied with a Lakeshore 336 cryogenic temperature controller. Electrical measurements were carried out with a Keysight B1500A semiconductor device analyzer.

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Author Contributions

Y.J. conceived the project and directed it; M.S.S. performed the material synthesis, device fabrication, and electrical and photovoltaic characterizations under the guidance of Y.J.; H.-S.C. performed the TEM characterization and analysis; D.D. performed the temperature-variant electrical characterization with M.S.S. under the guidance of T.R.; S.D. assisted with the fabrication of flexible devices under the guidance of Y.J. and T.R.; and M.S.S. and Y.J. wrote the manuscript with inputs from all authors.

Notes

The authors declare no competing financial interest.

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