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Quantitative, Dynamic TaO_x Memristor/Resistive Random Access Memory Model

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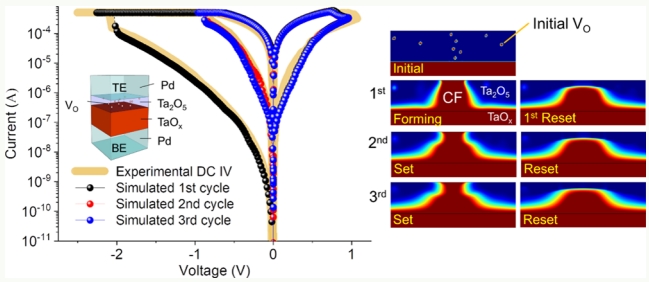
ABSTRACT: Oxide-based memristors are two-terminal devices whose resistance can be modulated by the history of applied stimulation. Memristors have been extensively studied as memory (as resistive random access memory) and synaptic devices for neuromorphic computing applications. Understanding the internal dynamics of memristors is essential for continued device optimization and large-scale implementation. However, a model that can quantitatively describe the dynamic resistive switching (RS, e.g., set/reset cycling) behavior in a self-consistent manner, starting from the initial forming process, is still missing. In this work, we present a Ta_2O_5/TaO_x device model that can reliably predict all key RS properties during forming and repeated set and reset cycles. Our model revealed that the forming process originates from electric field focusing and localized heating effects from the initial nonuniform oxygen vacancy (V_O) defect distribution. A broad range of device behaviors, including cycling of the V_O distribution during set/reset cycles, multilevel storage, and two different filament growth processes, can be quantitatively captured by the model. In particular, a bulk-type doping effect with low programming current was found to produce linear conductance changes with a large dynamic range that can be highly desirable for neuromorphic computing applications. The simulation results were also compared with experimental dc and pulse measurements in 1R and 1T1R structures and showed excellent agreements.



KEYWORDS: *memristor, Ta_2O_5, oxygen vacancy, forming, cycling, 1T1R*

1. INTRODUCTION

Nanoscale memristor devices have been widely considered as a promising candidate for neuromorphic and other memory-centric applications[1−3] because of their simple structure and superior performance metrics, including endurance, switching speed, and exceptional scalability.[4−6] Moreover, memristors can be used to both store data in their analog conductance states and process data at the same physical locations, allowing power-efficient computing both in-memory and in parallel,[7−18] inducing recent implementations of convolutional neural networks and other machine learning models for image and natural language processing tasks. The principle of resistive switching (RS) in oxide-based memristors has been explained by V_O migration in the oxide layer through ion drift and diffusion, where V_Os act as dopants and modulate local electrical and thermal conductivities.[19−24] After the set process, high V_O concentration (n_D) regions can act as conducting filaments (CFs) and provide high conductance channels in the switching layer.

A number of device models have been proposed to describe the RS dynamics such as the formation/rupture of CFs.[25−31] However, these models typically start from assumptions that a filament is already (partly) formed and cannot, in general, reliably reproduce multiple RS cycles. Additionally, most models do not provide a mechanism to control the programming current during filament formation, which is critical during practical device applications. These challenges can be largely attributed to the complex physics required in the models.

In this work, we present a comprehensive physical model for TaO_x-based memristor that can accurately capture practical device operations, starting from the initial state, by self-consistently solving[20,29] the electric field (E), temperature (T), and V_O concentration (n_D) dynamic evolutions in realistic device structures. The maximum programming current during filament formation, that is, the compliance current (I_{CC}), is also introduced in the model through a current modulation layer. Our model clearly revealed that the forming process is a result of the initial nonuniform oxygen vacancy (V_O) defect distribution and initiated by electric field focusing and localized thermal effects. By carefully considering the conduction mechanisms and the temperature effects, the model can successfully predict repeated set/reset cycles, whereas previous models[28] would fail after a few set/reset cycles. Additionally, we observed different

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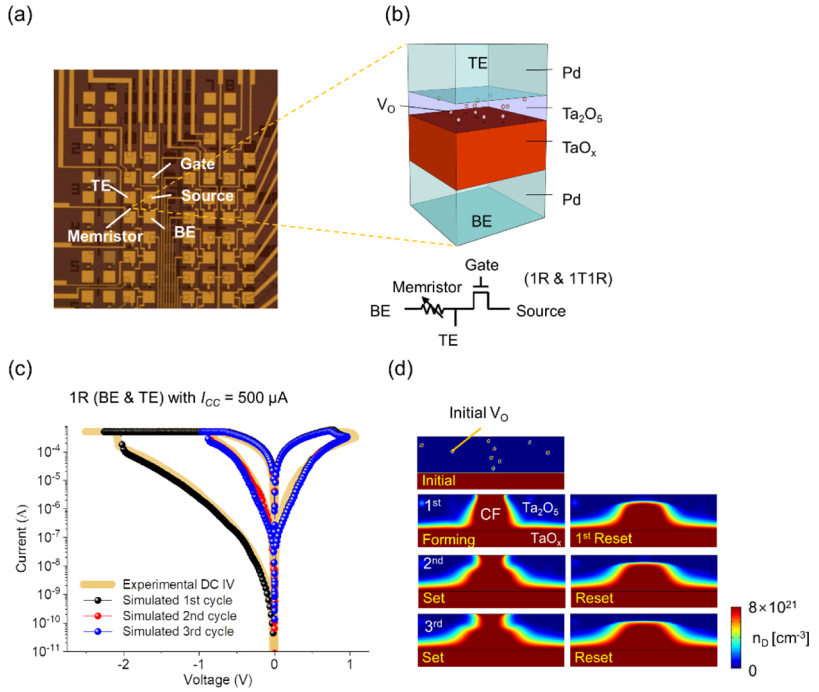

Figure 1. Tantalum oxide memristor during forming and set/reset cycling. (a) Top view of the integrated memristor (1R and 1T1R) on the CMOS chip. (b) Schematic of the Pd/Ta_2O_5/TaO_x/Pd bilayer device and the 1T1R circuit. (c) Measured and simulated dc I–V characteristics of the memristor device with 500 μA I_{CC}, showing the forming and consecutive set and reset switching cycles. (d) 2D maps of n_D obtained in the model for initial, forming, first reset, and subsequent set and reset states. After forming and first reset, CF formation/rupture can be reliably repeated in subsequent cycles.

RS mechanisms during the set process, depending on the programming current level. With a low programming current, a bulk-type doping phenomenon was observed. This effect can lead to linear analog conductance modulation with a large dynamic range, which is beneficial to low-power neuromorphic computing applications. On the other hand, filament width growth becomes dominant at high programming current levels, resulting in high conductance values and a leaky high-resistance state (HRS) and a small dynamic range. These results were further verified by experimental studies using a 1T1R device structure, where the maximum programming current was controlled by the gate voltage (V_G) to allow systematical tuning of the conductance level and the V_O configuration.

2. RESULTS AND DISCUSSION

2.1. Device Integration and Physical Model. A standard bilayer Ta_2O_5/TaO_x device structure is chosen as the model system. The device consists of a high-resistance Ta_2O_5 layer on top of a more conductive TaO_x layer,[32] sandwiched by a Pd-based top electrode (TE) and a bottom electrode (BE). The device is directly fabricated on top of a CMOS chip and is integrated with an on-chip transistor (1T) to form 1R or 1T1R structures (see Methods), as shown in Figure 1a,b.

RS in the Ta_2O_5/TaO_x device has been generally explained by the V_O redistribution and V_O exchange between the high-resistance Ta_2O_5 layer and the low-resistance TaO_x layer.[28,33] Specifically, a negative voltage applied to the TE attracts V_Os from the TaO_x layer, which acts as a V_O reservoir, into the Ta_2O_5 layer and forms a CF connecting the TE and the conductive TaO_x layer. This process switches the device to the low-resistance state and is termed the set process. When a positive voltage is applied to the TE, it repels V_Os from the Ta_2O_5 layer and breaks the filament, thus switching the device back to the HRS in the so-called reset process, as shown in Figure 1c.

Our model aims to achieve quantitative agreements with experimental results, starting from the initial state. To start with, we assume a uniform V_O concentration of $n_D = 1 \times 10^{22}$ cm^{-3} and conductivity of 10^5 S/m in the conductive TaO_x layer, based on results from density functional theory calculations[34] and experimentally measured conductivity values of TaO_x films[35] and only a small number of V_Os that are randomly distributed in the Ta_2O_5 layer (Figure 1b,d). The size of the V_O defects in the Ta_2O_5 layer is assumed to be 3 Å,[34] and the V_O defects are assumed to have the same local conductivity of 10^5 S/m as the TaO_x layer, whereas the stoichiometric Ta_2O_5 film is assumed to have a very low n_D level (1×10^{16} cm^{-3}) and is highly resistive. In the proposed model, the electrical conductivity (σ) in the oxide is assumed to depend on the V_O concentration (n_D), temperature (T), and electrical field (E) and is given by

$$\sigma_{Ta_2O_{5-x}} = \sigma_0(n_D)\exp(-E_{ac}(n_D)/kT) + \sigma_{PF}(E, T) \quad (1)$$

where σ_0 is a prefactor, E_{ac} is the activation energy for electron conduction, and $\sigma_{PF}(E,T)$ represents the Poole–Frenkel (PF) conduction term ($\sigma_{PF}(E, T) = \exp(293/T\cdot(\alpha\sqrt{E} + \beta))$. Considering the ion drift/diffusion in the oxide layer, n_D can be determined by

$$\partial n_D/\partial t = \nabla\cdot(D\nabla n_D - vn_D + DSn_D\nabla T) \quad (2)$$

where $D\nabla n_D$ and vn_D are the Fick diffusion flux and the drift flux terms, respectively.[28] The $DSn_D\nabla T$ term corresponds to the Soret diffusion flux, where S is the Soret coefficient ($S = -E_a/kT^2$). Soret diffusion is the movement of particles along a temperature gradient because of the different diffusion constants at different temperatures. In this simulation, it describes the tendency for V_Os to move toward the hotter region (i.e., the

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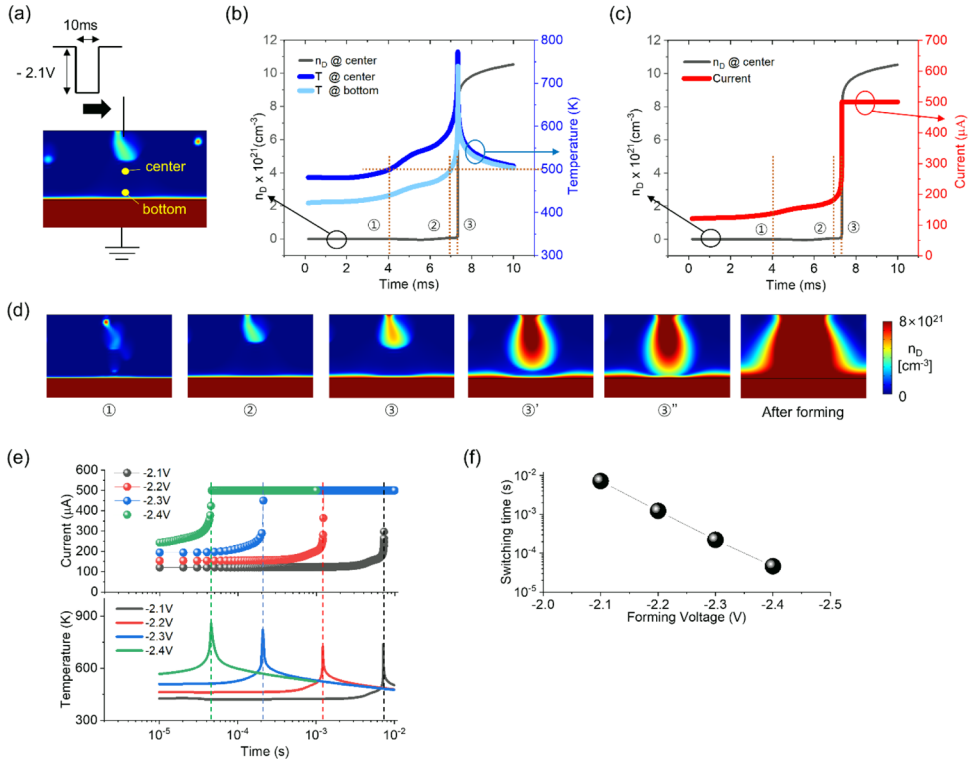

Figure 2. Forming process. (a) Schematic of the device during pulse forming. (b) n_D and T evolutions in the bottom and center regions marked in (a). (c) Current and n_D evolution during the forming transition. (d) Evolution of the internal V_O configuration at different stages during forming. (e) Current and temperature evolutions in the bottom region at different forming voltages. (f) Forming speed vs forming voltage.

filament region) in a temperature gradient (due to the higher diffusivity of oxygen ions at higher temperatures), which helps the formation of a stable CF by V_Os even at high temperatures. The diffusion coefficient (D) is given by

$$D = 1/2 \cdot a^2 f \exp(-E_a/kT) \tag{3}$$

and the drift velocity (v) is given by

$$v = af \exp(-E_a/kT)\sinh(qaE/2kT) \tag{4}$$

where f is the escape-attempt frequency (10^{12} Hz),[28] a is the effective hopping distance (0.32 nm), and E_a is the activation energy for V_O migration (0.85 eV).

Equation 2 can be self-consistently solved along with eq 5, the continuity equation for electrical conduction, and eq 6, the Fourier equation for Joule heating, following the approach proposed by Ielmini et al.[29]

$$\nabla \cdot \sigma \nabla \Psi = 0 \tag{5}$$

$$\rho C_p \frac{\partial T}{\partial t} - \nabla \cdot k_{th} \nabla T = J \cdot E \tag{6}$$

where σ is the electrical conductivity and Ψ is the electric potential.

The equations are solved in a numerical solver (COMSOL) to calculate n_D, Ψ, and T. To simulate realistic devices, we also introduce a current modulation layer that can control the programming current, as shown in Supporting Information Figure S1. The definitions of the parameters used in the model are summarized in Supporting Information Table S1 and Figure S2. The details for the proposed model are also discussed in the Supporting Information.

2.2. Forming Process. Figure 1c shows the measured and the simulated dc $I-V$ characteristics during the forming, set, and reset processes with 500 μA of I_{CC} (Supporting Information Figure S3a). A very good match of the simulation results with the measured data can be found. The forming and set transitions occur at negative voltages, around −2.04 and −0.9 V, respectively, whereas the reset transition starts around 0.8 V for this model device. Figure 1d plots the two-dimensional (2-D) maps of n_D for three consecutive switching cycles, showing the creation and elimination of the V_O depletion gap during repeated cycling. Note that the model can run in a self-contained manner (e.g., no adjustment of parameters) from the initial state and through repeated cycling without degradation (Supporting Information Movies S1−S4).

Before the forming transition, the current level is very low because of the highly resistive Ta_2O_5 layer, where the current conduction mechanism is dominated by PF emission. In local regions within the Ta_2O_5 layer with a few closely spaced V_O defects (Figure 1d), the PF current is larger because of the electric field focusing effect that further leads to localized heat generation. The higher local electric field and elevated temperature (>500 K) due to Joule heating eventually cause the original V_Os in the Ta_2O_5 layer to migrate toward the TE during the first stage of forming (Supporting Information Figure S4). This process leads to a small filament to be formed from these original V_Os in the oxide film. However, during this stage V_O migration from the V_O reservoir is negligible because the temperature at the interface between the Ta_2O_5 layer and the TaO_x layer is still too low (<500 K) to trigger strong V_O drift/diffusion from the V_O reservoir (Supporting Information Figure S4b). This effect is more clearly observed in pulse simulations by applying a short pulse with a fixed amplitude to the virgin device (Figure 2a). Negligible changes in conductance are observed in stages ①−② (Figure 2b,c) when the temperature at the Ta_2O_5/

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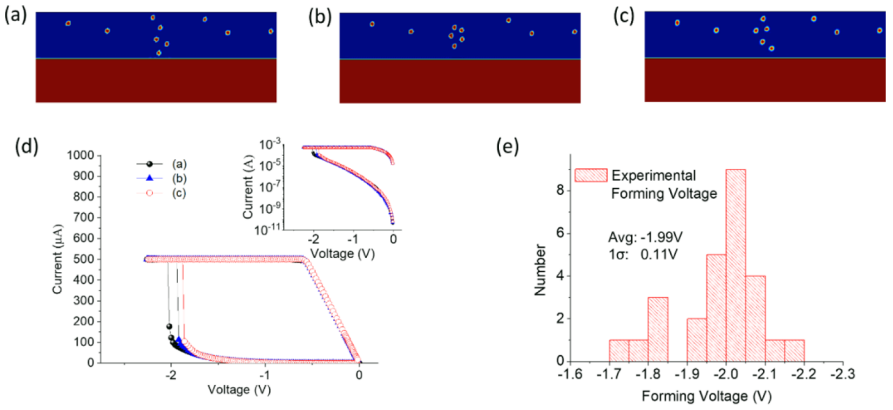

Figure 3. Variation of the forming voltage originating from different initial states. (a–c) Different initial states with the same number of V_Os in the switching layer. (d) Simulated forming I–V characteristics with different initial states in (a–c). (e) Experimentally measured forming voltage distribution from 27 samples fabricated on the same chip.

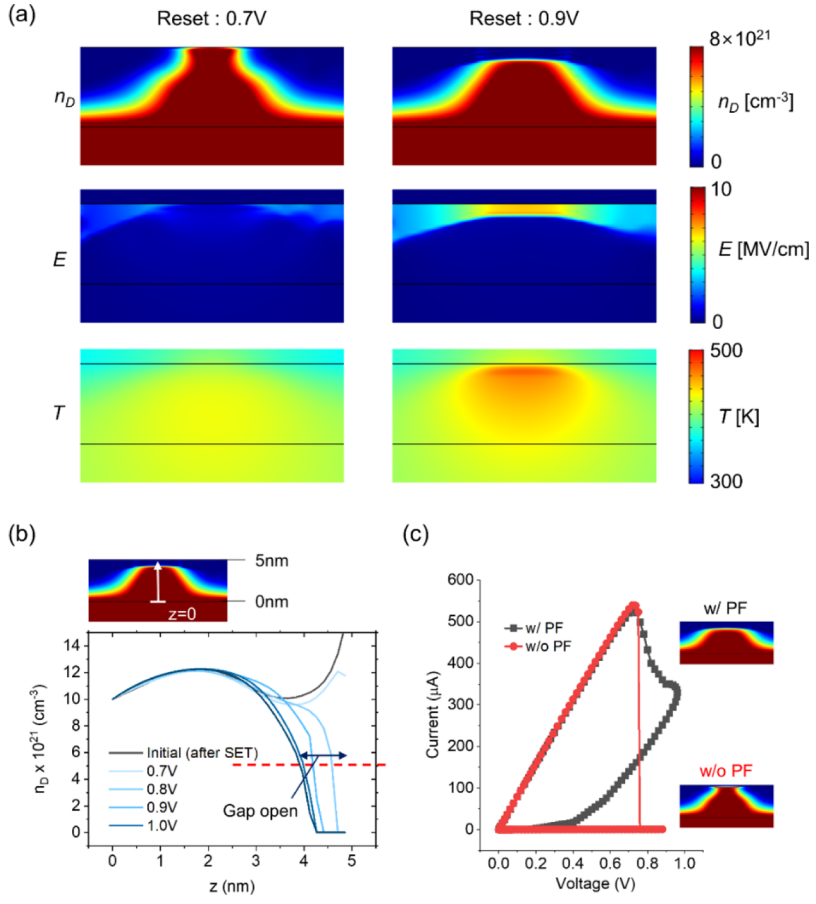

Figure 4. Simulated dc reset process. The voltage sweep rate is 2 V/s. (a) 2D maps of V_O concentration (n_D), electric field (E), and temperature (T) in the device during the reset process at different voltages. (b) 1D profile of n_D along the vertical direction during reset with different reset voltages. (c) Reset with and without the PF effect in the depletion gap. A very narrow gap and failed cycling are obtained without PF.

TaO_x interface is still low, even though the original V_Os in the Ta_2O_5 layer have already migrated to the TE (Figure 2d ①–②). Once the temperature at the Ta_2O_5/TaO_x interface reaches a critical temperature ~500 K (stage ③), the influx of V_Os from the V_O reservoir increases exponentially because of strong V_O drift/diffusion aided by the elevated temperature. Eventually, the extra V_Os supplied from the V_O reservoir form the CF connecting the TE to the conductive TaO_x layer and resulting in the abrupt conductance increase (stages ③–③″, Figure 2c,d). As a result, the switching speed of the forming process strongly depends on the temperature of the Ta_2O_5/TaO_x interface, which in turn is a function of the applied voltage. When a more negative voltage is applied during the forming process, the temperature at the Ta_2O_5/TaO_x interface increases more rapidly and results in faster switching (Figure 2e,f). Such an exponential dependence of forming time versus voltage is commonly observed experimentally.

It should be noted that this transition is driven by a positive feedback process, where a high CF temperature leads to a rapid CF growth, which in turn increases the CF temperature because

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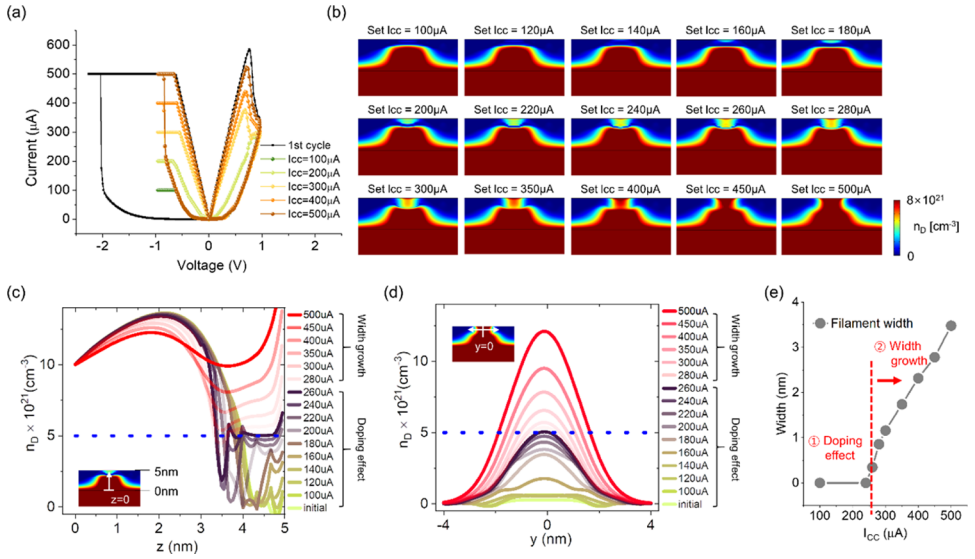

Figure 5. Two different filament growth mechanisms during set with different I_{CC}s. (a) Simulated set and reset dc $I-V$ characteristics and (b) 2D maps of V_O concentration (n_D) at different I_{CC}s. The measurements start after forming with 500 μA I_{CC} and the first reset. Bulk-type doping effect dominates in the low I_{CC} (<260 μA) cases, whereas lateral filament growth can be observed in the high I_{CC} (280−500 μA) cases. (c) Vertical 1D n_D profiles after set for different I_{CC}s. The $z = 0$ position is the Ta_2O_5/TaO_x interface. (d) Horizontal 1D n_D profiles after set for different I_{CC}s. The $y = 0$ position is the center of the filament. (e) Filament width as a function of I_{CC}.

of increased Joule heating effects. After the initial CF growth, prolonged positive feedback during the CF formation should be avoided to improve device reliability, normally by limiting the maximum programming current. Otherwise, permanent damage to the dielectric might occur, and the device cannot be reset again. To model the current compliance effect, we introduced a current modulation layer in the model to control the programming current (Supporting Information Figure S3) during CF formation. Our model clearly shows that once the current level reaches I_{CC} during forming, that is, 500 μA in this example, the CF temperature starts to decrease and the positive feedback stops, which suppresses further V_O drift/diffusion (Figure 2b,c). This leads to controlled and reliable filament formation in the oxide layer (Figures 1d and 2d).

Importantly, the proposed model also clearly reveals that the device-to-device variation of the forming voltage can be traced to the different initial V_O defect profiles in the switching layer (Figure 3a−c). By simply changing the initial V_O defect locations while keeping the number of V_Os constant in the switching layer, our simulation produces different forming voltages for different devices (Figure 3d). These results are consistent with experimental results, where devices even fabricated on the same chip show different forming voltages from −1.7 to −2.2 V [average: −1.99 V; normal distribution (1σ): 0.11 V], as shown in Figure 3e. These findings clearly highlight that even though a relatively uniform film is deposited, precise control of the forming voltage can be challenging because of the stochastic V_O distributions. Precise control of the defect locations, for example, through engineered electrode structures or ion blocking barriers,[36,37] may be necessary if tight distribution of the forming voltage is required.

2.3. Reset and Set Cycling. During the first reset after the initial forming process, our model shows that the CF rupture occurs near the TE, caused by internal V_O redistribution driven by a combination of electric field and thermal effects (Figure 4a). Similar to the forming process, the reset process strongly depends on the local temperature. As the CF is usually formed as a cone shape with a narrow width near the TE (as verified by our simulation shown in Figure 1d), this region experiences a more pronounced temperature rise because of Joule heating, as shown in Figure 4a, and the elevated temperature activates the V_O drift/diffusion at this location. Once the V_Os in this region gain enough thermal energy at the sufficient reset voltage (e.g., 0.9 V), they will be repelled from the TE region by the applied electric field and create a V_O depletion gap between the TE and the CF, resulting in a decrease of the device conductance.

Figure 4b shows the one-dimensional (1D) profile of n_D along the vertical (z) direction during reset with different reset voltages. These results verify that the gap region can be further increased by a larger reset voltage, resulting in further increase of the device resistance. Additionally, we found that it is important to maintain a sufficiently elevated temperature in the filament region during reset to achieve reliable switching behavior. In our model, the PF conduction allows sufficient current to continue to flow through the V_O depletion region during reset and prevents the CF temperature from dropping abruptly soon after the gap is created. Figure 4c shows the reset simulation results with and without the PF conduction term. When the PF conduction term is removed from the model (i.e., removing the $\sigma_{PF}(E,T)$ term from eq 1), the temperature quickly drops as soon as the depletion gap appears, and subsequent V_O drift/diffusion processes essentially stop. As a result, this process fails to produce a sufficiently large V_O depletion gap and leads to cycling failure, as shown in Figure 4c.

After the forming process with 500 μA I_{CC} and the first reset process, the set process is simulated in a self-contained manner, with different levels of set programming currents (I_{CC}s) controlled by the current modulation layer. The set/reset cycling can be reliably repeated through our simulations. Additionally, as shown in Figure 5a,b, both the dc $I-V$ characteristics and the CF shapes are governed by I_{CC} during the set transition. Importantly, we observed two different filament growth mechanisms based on the I_{CC} level: a bulk-type doping mechanism and a filament width growth mechanism. At low set I_{CC} (100−260 μA), n_D is gradually increased in the gap region, that is, representing a bulk-type doping effect in the gap

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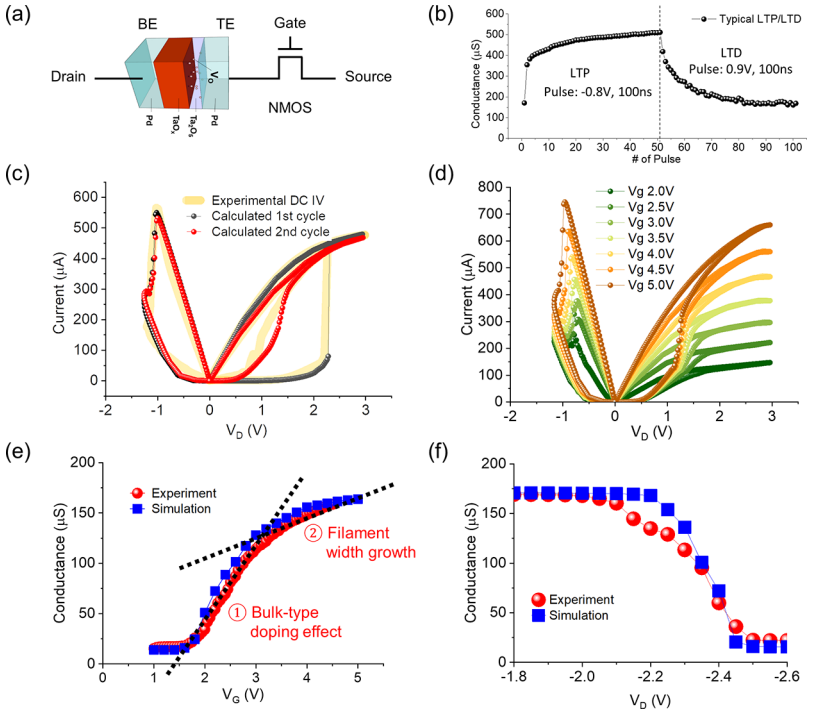

Figure 6. Experimental and simulated 1T1R characteristics with different gate voltages (V_G). (a) 1T1R schematic. (b) Typical LTP/LTD behaviors in the same device structure by applying identical set and reset pulse trains without I_{CC}. (c) Measured and simulated 1T1R dc I–V curves with V_G = 4 V during forming and set. (d) Simulated set and reset curves with different V_G. (e) Measured and simulated LTP behaviors with incremental V_G with 3 V and 10 μs V_D pulses. Different slopes and dynamic ranges can be clearly observed. (f) Measured and simulated LTD behaviors with different V_Ds with 1 μs pulse.

region, but the n_D level does not reach the metallic conduction level (5×10^{21} cm^{-3}) where E_{ac} becomes ~0 (Supporting Information Figure S2a); so this process corresponds to the conductance increase prior to CF completion. With high set I_{CC} (280–500 μA), the filament is formed in regions with $n_D > 5 \times 10^{21}$ cm^{-3}, and lateral filament growth can be observed with continued set programming. This process corresponds to CF expansion.

These effects are also clearly observed in the 1D n_D profile plots along the vertical (z) and horizontal (y) directions for different I_{CC}s, as shown in Figure 5c,d. The V_Os are first accumulated near the TE and migrate to fill the gap region (Figure 5c), similar to the forming process. After n_D reaches the metallic n_D level ($n_D = 5 \times 10^{21}$ cm^{-3}), further increase of I_{CC} leads to both increase in n_D and lateral expansion of the CF (Figure 5d). In this regime, the width of the metallic CF is linearly broadened as I_{CC} is increased (Figure 5e). The filament width modulation mode, however, yields a small dynamic range because the device conductance is already high after the initial CF formation, whereas a much higher dynamic range is observed in the doping region, as we will discuss in more detail in the next section.

Our analysis shows that different forming I_{CC} leads to different filament shapes. For instance, decrease of I_{CC} (300 μA) during forming results in a small filament size, producing a more resistive HRS after reset, compared with the case with the same reset voltage but formed with 500 μA I_{CC} (Supporting Information Figure S5a–d), whereas increasing I_{CC} (800 μA) during forming leads to a large filament size with a more conductive HRS after reset (Supporting Information Figure S5e–h). The filament shapes with different set I_{CC}s (100–500 μA) after 300 μA I_{CC} forming and first reset are also analyzed and compared to the cases with 500 μA forming I_{CC} (Supporting Information Figure S6). Interestingly, even with the same set I_{CC}, the filament shapes and conductance levels are not the same for the two forming conditions (I_{CC} = 300 and 500 μA), which is another evidence that the conductance of a memristor depends on the history of external stimulation.[19,38] Furthermore, the long-term potentiation (LTP) behavior with incremental set I_{CC}s under different forming conditions (300 vs 500 μA) was investigated. It was found that forming with a lower I_{CC} provides a larger dynamic range (on/off ratio), although the conductance update slope becomes sharper, which makes it more challenging to fine-tune the conductance/weight (Supporting Information Figure S7).

This observation explains the discrepancy of filament shapes between the forming and set states even with the same I_{CC} (Figure 1d). Specifically, the forming transition starts from the initial state and requires larger voltage and higher temperature to create a filament, whereas the set process starts on the conditions where the filament is already created and partially ruptured. The different initial states lead to different electric field and temperature profiles during forming and set and produce different filament shapes in the end, as shown in Figure 1d and Supporting Information Figures S5 and S6. On the other hand, during set/reset cycling, the same filament growth/rupture conditions can be maintained, leading to reliable set/reset cycles as shown in Figure 1d.

Pulse simulations were performed to examine the set and reset switching characteristics over time with different voltages (Supporting Information Figure S8a–e). Similar to forming, a larger set/reset voltage pulse leads to higher internal temperature, resulting in faster set/reset switching. We also modeled other conditions, including different Ta_2O_5 thicknesses, device

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area, and ambient temperature, to examine the effects of these parameters on the switching characteristics. The forming voltage strongly depends on the Ta_2O_5 thickness, whereas set and reset switching behaviors are not affected by the film thickness, as shown in Supporting Information Figure S9. The forming/set/reset voltages do not depend on the device area (20, 40, and 100 nm) because the filament is formed locally; however, the subthreshold current during forming reduces as the device area is reduced, as shown in Supporting Information Figure S10. With higher ambient temperature, we found that the forming voltage can be decreased because of high drift and diffusion coefficients, as shown in Supporting Information Figure S11a. Similarly, set and reset voltages can be decreased when the ambient temperature is increased, as shown in Supporting Information Figure S11b,c.

Our model is largely analytical and based on solving the three partial differential equations, which assume that the oxygen vacancy concentration is continuous and its modulation is gradual. This approach allows us to simulate full-scale, realistic physical device structures and capture key device parameters in reasonable time, but does not consider the stochastic, discrete oxygen vacancy migration effects that are captured by models such as kinetic Monte Carlo (KMC).[39] Future advances in simulation techniques that can improve the simulation time of the KMC methods will be necessary to allow full-scale device simulations that fully incorporate the stochastic switching effects.

2.4. 1T1R Experiments and Simulation. In 1T1R devices, the transistor, controlled by the gate voltage (V_G), can effectively modulate the maximum current and suppress the off current level, thus allowing more precise control of the memristor conductance. In particular, current overshoot due to discharging current from parasitic capacitances can be effectively suppressed,[40,41] allowing more reliable forming and set processes. The transistor also serves as an excellent selector that suppresses sneak currents in an array. As a result, the 1T1R structure is widely used for practical implementation of large memristor arrays,[9,13,14,42] especially for inference applications and edge computing[43,44] where data processing occurs close to the point of data creation.

We used n-type enhancement-mode transistors to implement the 1T1R devices (Figure 6a and Supporting Information Figure S3b). The CMOS chip with standalone transistors is fabricated in a commercial fab, and TaO_x-based memristor devices are integrated on the drain side of the transistor afterward (Figure 6a and Supporting Information Figure S12). The transistor $I-V$ model is successfully implemented in the current modulation layer in our model (Supporting Information Figure S3b). In the integrated 1T1R structure, the BE of the bilayer memristor is connected to the drain of the transistor to apply effective negative forming and set voltages to the memristor (Supporting Information Figure S12b).

Similar to the 1R case with I_{CC}, the simulation starts from the initial state where V_Os are nonuniformly distributed in the switching layer. The model can accurately capture the forming, reset, and set switching characteristics. Figure 6c shows that during forming and set switching, the maximum current is limited by the transistor saturation current, for example, $I_{CC} \approx 470\ \mu A$ at $V_G = 4$ V and $V_D = 3$ V. During forming and set transitions, the strong positive feedback process between Joule heating and filament formation is stopped when the memristor current reaches the transistor saturation current, leading to reversible and stable CF formation in the switching layer. In the reset process, the transistor is fully turned ON to minimize the series resistance effect. Because only a positive bias is available for NMOS to switch the memristor in the 1T1R form, we applied the positive bias to the source (0−1.2 V) of the original transistor structure, leading to a negative voltage at the drain (Figure 6c). The simulated consecutive dc $I-V$ switching cycles match well with the measured results. Here, the forming, set, and reset voltages are slightly increased compared to those of the 1R device because of the series transistor resistance.

The conductance level of the 1T1R device can be precisely controlled by changing the gate voltage V_G during set. This typically results in better tuning of the conductance values than applying identical pulses without I_{CC} (Figure 6b). Results of different set conditions after forming with $V_G = 4$ V and the first reset are shown in Figure 6d. Modulation of V_G from 2 to 5 V during set clearly shows the ability to control the conductance levels in the 1T1R device. The model also captures the pulsed LTP and long-term depression (LTD) behaviors in the 1T1R device, consistent with experimental results. For LTP, 3 V and 10 μs V_D pulses were applied to the drain with varying V_G. Even in the pulse condition, bulk-type doping and lateral filament growth regions (Figure 6e) are clearly identified, with different slopes and dynamic ranges with increasing V_G. Similar to the effects of I_{CC} in the 1R structure, a low V_G (1.5−3 V) leads to a bulk-type doping effect with a large dynamic range, whereas a large V_G (3−5 V) leads to the filament width growth effect with a small dynamic range. Here, the read condition was $V_D = 0.3$ V and $V_G = 5$ V. Note that the conductance of the 1T1R device cannot be modulated by V_G lower than 1.5 V both in simulation and in experiment, where the current level is not large enough to initiate V_O migration, as shown in Figure 6e.

Analog LTD behaviors can also be achieved by modulating V_D (Figure 6f), with excellent agreements of the modeling and experimental results. Note that LTD may be harder to control compared to LTP in the 1T1R system because of the changing V_{GS} during reset transition because the device resistance is connected to the effective source side of the transistor and varies during reset. Fortunately, online learning based on LTP only can be effectively implemented by using a pair of memristor devices.[45] For inference applications that do not require online learning, it is also sufficient to achieve precise conductance programming through the program-and-verify scheme,[13,42] where the initial HRS state can be achieved by applying a large positive voltage to the source (e.g., $-V_D$ in Figure 6f). This approach allows the weights to be precisely reprogrammed during the infrequent model updates.

3. CONCLUSIONS

In this study, a Ta_2O_5/TaO_x device model that can self-consistently and quantitatively describe the dynamic RS processes including forming and set/reset cycles is successfully developed. Excellent agreements with experimental dc and pulse measurements in 1R and 1T1R devices were obtained. Forming was observed to originate from the initial nonuniform defect distribution, and electric field focusing and localized thermal effects were found to strongly affect the filament formation process (Supporting Information Figure S13). By controlling I_{CC}, the V_O configuration can be systematically tuned during CF growth, resulting in different RS behaviors. Two different filament growth modes were observed, leading to different conductance modulation slopes and dynamic ranges. In particular, a low programming current induces bulk-type doping effects, resulting in linear conductance/weight updates and a

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large dynamic range. The model and observations will help continued device optimizations and applications in memory and low-power neuromorphic computing applications.

4. METHODS

4.1. Device Fabrication. The TaO_x-based memristor used in this work was directly fabricated on top of the CMOS circuit. First, SiO_2 with 100 nm thickness was deposited on the CMOS chip, followed by a reactive ion-etching process to open the CMOS landing pads (gate, drain, source, and bulk). Then, Pd BEs with 40 nm thickness were defined on SiO_2 by photolithography and e-beam evaporation of the Pd metal, followed by a lift-off process. A 30 nm TaO_x layer was deposited by dc reactive sputtering of a Ta metal target in an Ar/O_2 environment at room temperature, followed by the deposition of the 5 nm Ta_2O_5 switching layer through sputtering a Ta_2O_5 ceramic target in the same chamber without O_2. Afterward, the TE was fabricated, followed by a reactive ion-etching process in SF_6/Ar to expose the contact regions of the BEs. Finally, metallization processes were performed by photolithography to connect the electrodes (BE and TE) with the CMOS landing pads, as shown in Supporting Information Figure S12. The TaO_x memristor device is located on the drain side, and the BE becomes the drain in the 1T1R system to control the transistor saturation current along with V_G during forming/set. For flexibility, devices can be measured in either the 1T1R structure or the 1R (without transistor) structure using an additional pad.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.9b00792.

Device structure for simulation, parameters and constant values used in the model, I_{CC} and transistor model in the current modulation layer, simulated forming, set, and reset processes under different conditions, and LTP behavior with different forming I_{CC} (PDF)

Forming process through dc sweep (AVI)

First reset process through dc sweep (AVI)

Set process through dc sweep (AVI)

Reset process through dc sweep (AVI)

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Notes

The authors declare no competing financial interest.

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