Towards a Low-SWaP 1024-Beam Digital Array: A 32-Beam Subsystem at 5.8 GHz

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***Abstract*— Millimeter-wave communications require multibeam beamforming to utilize wireless channels that suffer from obstructions, path loss, and multipath effects. Digital multibeam beamforming has maximum degrees of freedom compared to analog-phased arrays. However, circuit complexity and power consumption are important constraints for digital multibeam systems. A low-complexity digital computing architecture is proposed for a multiplication-free 32-point linear transform that approximates multiple simultaneous radio frequency (RF) beams similar to a discrete Fourier transform (DFT). Arithmetic complexity due to multiplication is reduced from the fast Fourier transform (FFT) complexity of $\mathcal{O}(N \log N)$ for DFT realizations, down to zero, thus yielding a 46% and 55% reduction in chip area and dynamic power consumption, respectively, for the $N = 32$ case considered. This article describes the proposed 32-point DFT approximation targeting 1024 beams using a 2-D array and shows the multiplierless approximation and its mapping to a 32-beam subsystem consisting of 5.8 GHz antennas that can be used for generating 1024 digital beams without multiplications. Real-time beam computation is achieved using a Xilinx field-programmable gate array (FPGA) at 120 MHz bandwidth per beam. Theoretical beam performance is compared with measured RF patterns from both a fixed-point FFT and the proposed multiplier-free algorithm and is in good agreement.**

***Index Terms*— Approximate beamforming, digital arrays, multibeams.**

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I. Introduction

THE efficient formation of far-field antenna patterns simultaneously across a multitude of directions is crucially important for wireless communications, radio astronomy, imaging, radar, and electronic warfare. Multibeam beamforming has been usually achieved in the microwave domain using analog techniques (e.g., Rotman lenses [1] and Butler/Nolan matrices [2], [3]). Emerging mmW systems are considering hybrid multibeam beamforming due to its power efficiency and excellent performance for a reasonably small number of antenna elements and user streams [4], [5]. Although digital beamforming requires the control of each individual antenna element in an antenna array, it is promising for the future technologies due to its several inherent advantages, which include [6]: 1) maximum flexibility/reconfigurabilty; 2) easy system updates and support for new beamforming algorithms as they emerge; 3) precise control of both the gain and phase of individual antenna elements thus giving better control of the beams; 4) maximum degrees of freedom from a given array; and 5) reduced maintenance and calibration requirements.

Elementwise digital beamforming requires a dedicated receiver (or transmitter, in transmit mode) for each antenna element, which is usually a uniformly spaced linear or rectangular array of antennas. Multibeams can be generated by expanding the concept of a phased-array to multiple simultaneous directions using the fact that each direction of propagation of a carrier wave is associated with two spatial frequencies $(\omega_x, \omega_y) \in \mathbb{R}^2$ across the two orthogonal coordinate axes of a rectangular array aperture. Multiple beam digital beamforming is desired at the lowest possible energy consumption for a given bandwidth, supply voltage, and technology node, which lead to domain-specific architectures that are optimized for low complexity and power consumption.

Here, we propose approximate computing-based algorithms and computing architectures that achieve quasi-orthogonal RF beams without using any digital multiplier circuits. The multiplierless nature of the digital computing architectures allows low chip area/size, weight, and power consumption (SWaP)

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and avoids the need for digital multipliers that have high circuit complexity (transistor count) and power consumption. This is likely to become more critical as wireless systems move to subterahertz frequencies and much wider channel bandwidths than used currently [7]. Algorithms that are multiplierless thus lead to substantially reduced SWaP in real-time digital silicon implementations [7], [8].

Multibeam beamforming on linear/rectangular apertures is important for exploiting multi-directional channels in massive-multi-in multi-out (MIMO) systems, for example, in 5G mmW wireless networks. Such systems rely on the combination of beamforming with MIMO theory [4], [5], [7], [9]–[11] and as frequencies move to terahertz ranges, the need for providing thousands of simultaneous beams will emerge due to the small size of the wavelength and physical antenna aperture. Recent work has described different phased array architectures targeting 5G applications [12]–[18]. However, most of the literature has been concentrated either on hybrid beamforming systems or fully analog architectures due to the prohibitive processing complexity of fully digital beamforming. Other important applications for microwave and mmW digital multibeam beamformers include emerging defense applications such as space-based low earth orbit communications, mesh networks between microsatellites, space-based Internet distribution to densely populated areas, and multi-domain mosaic warfare where reliable high-speed wireless connectivity is needed across multiple platforms (air, space, land, and sea), as well as for emerging terahertz imaging systems [7]. The demands of high-capacity wireless networks for such applications can be significantly more difficult to meet compared to commercial 5G standards since modern military platforms can travel at hypersonic speeds across hundreds of kilometers. Such demanding wireless channel conditions necessitate beamforming gain across wide bandwidths and narrow angles of propagation (i.e., sharp beams) to both thwart detection and also benefit from beamforming gain. Furthermore, 5G networks will eventually require digital beamforming to reduce the overhead associated with the current 3GPP beam search time in the 5G game structure—great reduction in beam pointing can be obtained by simultaneously searching the environment for the best pointing angle, but this is not yet supported in the 5G 3GPP standard [19].

Some recent work has focused on achieving elementwise fully digital beamforming. The work in [20] presents a low-power eight-element digital beamforming prototype based on bit-stream processing. The design uses a low-resolution $\Delta\Sigma$ architecture that replaces multipliers with multiplexers. This multiplexer-based architecture achieves lower power and smaller area than conventional digital beamformers, but the design is limited to a 20 MHz bandwidth with only two simultaneous output beams. Another recent paper [21] reports a 16-element four-beam digital beamformer targeting large-scale MIMO for 5G communication systems. It uses a similar multiplexer-based approach as in [20] with an interleaved architecture to support a 100 MHz bandwidth. The work in [22] and [23] also reports experimental verification of fully digital multibeam beamforming schemes targeting MIMO-based 5G implementations.

Miura *et al.* [24] present a spatial discrete Fourier transform (DFT)-based digital multibeam beamforming implementation scheme for satellite communications. The earlier work in [25] describes a low-complexity algorithm using the spatial DFT-based approach for generating 16 simultaneous beams using a uniform linear array (ULA). The work in [25] uses a 16-point DFT approximation to generate the simultaneous beams and presents the measured beams of its fully digital implementation targeting 5G MIMO applications. This article describes a novel low-complexity algorithm for realizing a massive number of simultaneous sharp beams, which are vitally important in coping with the rapid increments in path loss that is expected in future mmW/subterahertz wireless systems. In particular, we propose a low-SWaP approach to generate 1024 beams using a 32×32 aperture and ultralow-complexity digital very large scale integration (VLSI) hardware. We propose a 32-beam subsystem based on a novel 32-point DFT approximation as the building block of such a 32×32 system. The proposed 32-beam subsystem has been implemented at 5.8 GHz, and the digital beams have been measured and compared with those from exact DFT (EDFT) based beams. The measured beams have been used to derive the beam patterns of the corresponding 32×32 rectangular aperture by assuming identical element patterns in all directions.

This article is structured as follows. Section I provides an introduction to this article. Section II, followed by the introduction, describes the role of DFT for spatial filtering in multibeam transceivers. Section III describes a 32-point approximate DFT (ADFT) algorithm with zero multiplicative complexity. Section IV describes an experimental realization of a 32-element receiving array that can implement the proposed ADFT algorithm for digital beamforming. Experimental results from this array are presented in Section V. Finally, Section VI concludes this article.

II. Role of the DFT in Multibeam Transceivers

Multibeam beamforming on an $N \times M$ ($N,\ M \in \mathbb{Z}^+$) linearly spaced rectangular array can be achieved by uniformly sampling the spatial frequency domains to define a set of far-field plane waves having spatial frequencies determined by setting $(\omega_x, \omega_y) = ((2\pi/N)k_1, (2\pi/M)k_2)$ where $k_1 = 0, 1, \ldots, M-1$ and $k_2 = 0, 1, \ldots, N-1$. For this analysis, we consider $M = N$ so that the same proposed N-point transform can be used rowwise and columnwise in the rectangular aperture for generating 2-D beams. The spatial frequency points $((2\pi/N)k_1, (2\pi/N)k_2)$ correspond to beams pointing at unique angle pairs indexed by $(k_1, k_2) \in \mathbb{Z}^2$. The corresponding spatially sampled time-continuous plane waves at the terminals of the array elements can be expressed in a Fourier basis as $E(n_x, n_y, t) = E_0 \sum_{k_1=0}^{N-1} \sum_{k_2=0}^{N-1} x_m(t) e^{j(n_x\omega_x + n_y\omega_y + 2\pi f_c t)}$, f_c is the unmodulated carrier frequency, E_0 is a constant that sets the signal power, and $x_m(t)$ is the complex-modulated information component of the signal. Note that we assume the bandwidth of $x_m(t)$ is much smaller than f_c, since our analysis is only valid for narrowband signals for which the so-called spatial-wideband effect is negligible [26], [27].

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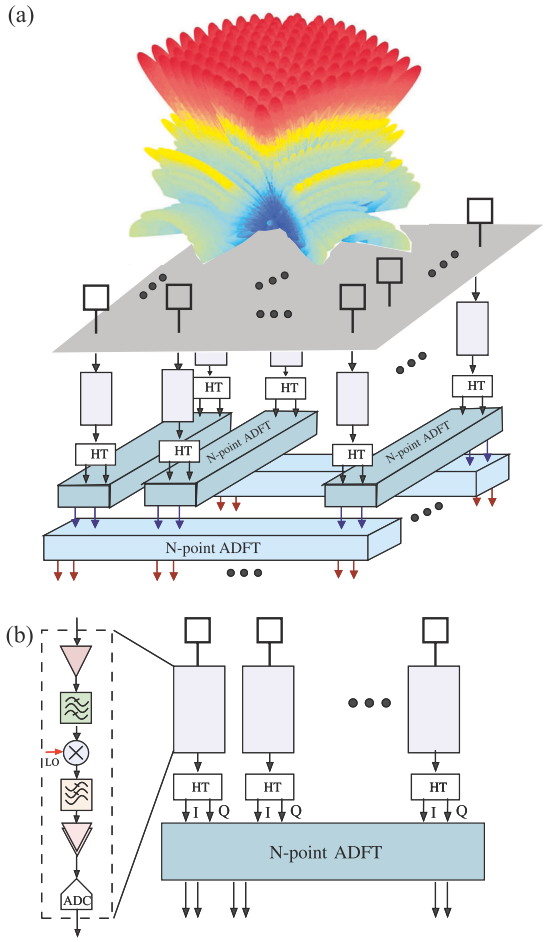

Fig. 1. (a) Digital beamforming architecture for obtaining N^2 beams using an $N \times N$ URA. (b) Block diagram of an N-element subsystem that acts as a building block for the N^2 rectangular aperture array. The **HT** block in the figure denotes the Hilbert transform operation.

In receiver mode, the plane waves present at the antennas are sampled in the spatial domain, amplified and filtered, down-converted to baseband [or an intermediate frequency (IF)], and finally digitized by an analog-to-digital converter (ADC) present at each array location. The digitized signals at each location are interpreted as complex, using in-phase (I) and quadrature (Q) components. For example, downconversion using a quadrature mixer (which is modeled as multiplication by $e^{-j2\pi f_c t}$) leaves the spatial frequency components $E_{BB}(n_x, n_y, t) = x_{m,k}(t)e^{j(n_x\omega_x + n_y\omega_y)}$ intact. As a result, the spatial spectrum of the wave remains localized at (ω_x, ω_y). The creation of a sharp RF beam for extracting directional information for a particular plane wave therefore involves the application of a 2-D spatial bandpass filter having the sharpest possible selectivity centered on a particular frequency pair in the spatial frequency domain. From filter theory, it is known that the DFT realizes a filterbank of finite impulse response (FIR) filters with sharp bandpass responses that take the well-known sinc(ω) response shape; the peak stopband magnitude for this shape has an asymptote of -13.25 dB for increasing filter order N. Therefore, to simultaneously receive an $N \times N$ array of signals, the multibeam beamformer must compute the 2-D DFT spatially across the n_x–n_y dimensions of the array.

For transmit applications, the waves to be transmitted at simultaneous multiple directions are applied to the inputs of the 2-D inverse DFT (IDFT), with the corresponding IDFT outputs being converted to analog using digital-to-analog converters (DACs), filtered, upconverted to the desired carrier frequency, and amplified before being applied to the input terminals of the transmit array. Thus, the computation of the 2-D spatial DFT/IDFT for each new sample of the digital baseband signal is a straightforward technique for achieving a large number of simultaneous RF beams in both receive and transmit modes.

Fig. 1(a) shows the digital beamforming architecture for an $N \times N$ uniform rectangular aperture (URA) that generates N^2 beams. The block diagram of an N-element ULA subsystem that acts as a building block for the N^2 URA is shown in Fig. 1(b). The direct computation of the DFT of an N-point vector of input values is defined as the matrix-vector multiplication $\mathbf{X} = \mathbf{F}_N \cdot \mathbf{x}$, where $\mathbf{x}$ and $\mathbf{X}$ are both N-point complex column vectors and $\mathbf{F}_N$ is the $N \times N$ complex matrix, known as the DFT matrix [28]. The direct matrix–vector multiplication requires a number of complex arithmetic operation in $\mathcal{O}(N^2)$, where $\mathcal{O}(\cdot)$ is O-notation [29, p. 429]. However, because of the symmetries of the DFT matrix, it is possible to compute the matrix–vector product $\mathbf{X} = \mathbf{F}_N \cdot \mathbf{x}$ with less than N^2 complex arithmetic operations. Algorithms that exploit the DFT matrix structure are called fast Fourier transforms (FFTs). FFTs are a famous and well-explored class of fast algorithms based on sparse matrix factorizations, which ultimately reduce the arithmetic complexity to compute $\mathbf{X} = \mathbf{F}_N \cdot \mathbf{x}$ to be of $\mathcal{O}(N \log N)$. The complexity reduction from $\mathcal{O}(N^2)$ to $\mathcal{O}(N \log N)$ is substantial as N grows large, which explains the importance of the use of FFTs in place of the DFT.

If we consider a single-beam conventional digital beamforming scenario, then that would need $3N$ real multiplications and $5N + 2(N\text{-}1) = 7N\text{-}2$ addition operations per beam. Considering this complexity, if N arbitrary beams are needed, then such system would demand for $3N^2$ real multiplications and $7N^2 - 2N$ real additions. The use of FFTs brings down this complexity to the order of $N \log N$. Using the proposed approach mentioned in Section III, we can obtain FFT-like 32 1-D beams at no multiplications and with only addition operations. We believe that these kind of large number of beams are required for applications like millimeter wave 5G communications as described in the introduction of this article. This method can be an overkill for applications that require only few number of beams. But for applications that do need multiple simultaneous beams, the proposed method provides an attractive solution with a much lower power consumption and area in VLSI implementations.

III. 32-Point DFT Approximation and Fast Algorithm for RF Beamforming

A. Approximate Computing

The implementation of FFT/DFT in fixed-point digital hardware always leads to errors in representing the twiddle factors [30], which are mostly irrational. Therefore, the implementation of an FFT in physical systems is not perfect and

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is always an approximation. If an approximation can be used with better overall performance than that results from the error sources of the system, then it makes sense to adopt such an approximation with the guarantee that it does not cause other impairments.

The difficulty in proposing DFT approximations for larger sequences relies on the hardness of deriving efficient fast algorithms for generated approximations [31], simply because the approximate transforms may not preserve the same symmetries and mathematical properties that exist in the exact DFT matrix.

B. 32-Point Approximate DFT

Here, we describe a 32-point ADFT matrix $\hat{\mathbf{F}}_{32}$ for which the matrix–vector multiplication operation can be computed without multipliers. Let $\mathbb{P}$ be the set $\{0, \pm 1, \pm 2, \pm 1/2\}$. Let $\mathcal{M}_{\mathbb{P}^2}(32)$ be the set of 32×32 complex matrices such that the real and the imaginary parts are defined over the set $\mathbb{P}$. The approximate transform $\hat{\mathbf{F}}_{32}$ can be found according to a multi-criterion optimization considering the search space represented by the parametrized mapping in the following:

$$\begin{aligned} g : \mathbb{R} &\longrightarrow \mathcal{M}_{\mathbb{P}^2}(32) \\ \beta &\longmapsto \text{round}(\beta \cdot \mathbf{F}_{32}) \end{aligned}$$

and objective functions given by the following selected matrix-based metrics: 1) Frobenius norm of the matrix difference; 2) total error energy; 3) average percentage absolute error; and 4) orthogonality deviation. The optimal solution for the DFT approximation can be found by the determination of the Pareto efficient solution set, which is the set of nondominant solutions [32] using $\beta \in (0, 5]$ with steps of 10^{-2}.

The optimal matrix resulting from the above optimization problem is given by

$$\hat{\mathbf{F}}_{32} = \begin{bmatrix} \mathbf{A}_0 & \mathbf{A}_1 \\ \mathbf{A}_2 & \mathbf{A}_3 \end{bmatrix}, \tag{1}$$

where $\mathbf{A}_i$, $i \in \{0, 1, 2, 3\}$, are 16×16 submatrices given by equation set (2) [33]. Among the efficient solutions, the matrix $\hat{\mathbf{F}}_{32}$ exhibits the smallest total error energy of approximately 3.32×10^2. The Frobenius norm of the matrix error per matrix element $(1/32^2)\|\hat{\mathbf{F}}_{32} - \mathbf{F}_{32}\|_F = 1.004 \cdot 10^{-2}$, where $\|\cdot\|_F$ is the Frobenius norm. This measurement is 54.9% lower than the error per element of the DFT approximation described in [25], [34], and [35], and can be regarded as acceptable.

Fig. 2 shows a comparison of the frequency responses of all the bins for the 32-point proposed ADFT and the DFT. The shapes and locations of the main beams are almost identical to the exact DFT. The relative errors of the magnitude response of each filter response are largely confined to the stopbands away from the main lobe (i.e., deep side lobes), and are generally below the -15 dB level. Fig. 2(c) shows the magnitude error plot of the filter bank responses of the proposed DFT approximation. The plot in Fig. 2(c) is computed by evaluating the difference of the magnitude responses of ADFT and exact DFT transforms for each filter (i.e., DFT/ADFT bin). The plots in Fig. 3 show the bins in Fig. 2(c) that have the highest magnitude error. All other bins have a magnitude error that is smaller than -13 dB. The deviations in the filter bank responses with respect to the DFT filter bank responses is a fact that arises due to filter coefficients not being ideal as they have been approximated by small integers. Thus, the performance level is mainly set by the size of the optimization search space.

It is also noted that the proposed approximation, due to its numerical structure, would not directly work with conventional windowing functions. However, these functions can be modified to achieve the desired windowing performance. The idea of the proposed transform is to generate multiple beams simultaneously and serve the applications that need simultaneous multiple look-directions with the sharpest beams.

C. Fast Algorithm for Computing the 32-Point ADFT

A fast algorithm for computing the approximate transform $\hat{\mathbf{F}}_{32}$ in (1) to be used in place of usual FFTs can be derived by means of sparse matrix factorization in a decimation-in-frequency approach [28]. The matrix transform $\hat{\mathbf{F}}_{32}$ can be factorized as follows:

$$\hat{\mathbf{F}}_{32} = \mathbf{W}_8 \cdot \mathbf{W}_7 \cdot \mathbf{W}_6 \cdot \mathbf{W}_5 \cdot \mathbf{W}_4 \cdot \mathbf{W}_3 \cdot \mathbf{W}_2 \cdot \mathbf{W}_1, \tag{3}$$

where $\mathbf{W}_i$ for $i \in \{1, 2, 3, 4, 5, 6, 7, 8\}$ are sparse matrices (factorization stages). The nonzero matrix elements of each matrix $\mathbf{W}_i$ are given in Table I. The matrix factorization in (3) is not unique (i.e., can admit multiple different factorizations) unlike factorization of a composite integer [36]. The number of stages (i.e., sparse matrices) in the matrix factorization depend on the factorization method employed. The number of stages is not important as long as the overall number of elementary arithmetic operations in the factorized form is lower when compared to the direct nonfactorized form of the matrix-vector product.

Note that the entries of sparse matrices $\mathbf{W}_i$ only contain the elements from the set $\mathbb{P}_0 = \{+1, -1, +j, -j\}$ which imply trivial arithmetic operations. Given the fast algorithm in (3), the computational complexity associated with computing can be quantified. Let us consider the complex input signals which correspond to inputs being the I and Q outputs of the received signal from the array to the digital processor and evaluate the arithmetic complexity in terms of real operations. The arithmetic cost of each matrix in each factorization stage of (3) is evaluated as described in [28]. As the coefficients of the real and imaginary parts of $\mathbf{W}_i$ for $i \in \{1, 2, 3, 4, 5, 6, 7, 8\}$ are also in $\mathbb{P}_0$, only additions are required; multiplications and bit-shifting operations are absent. The additive cost is based on the number of nonzero elements, i.e., the rows of each $\mathbf{W}_i$ matrix, as detailed in [28]. Therefore, the matrices $\mathbf{W}_1$, $\mathbf{W}_2$, and $\mathbf{W}_5$ require 60 real additions; the matrices $\mathbf{W}_3$, $\mathbf{W}_4$, and $\mathbf{W}_6$ require 28 real additions; and the matrix $\mathbf{W}_7$ requires 24 real additions. The only complex matrix in the factorization, $\mathbf{W}_8$, requires only 60 real additions. In total, the transform $\hat{\mathbf{F}}_{32}$ requires 348 real additions. Table II shows the real multiplicative and additive costs associated with several well-known FFT algorithms compared with the proposed algorithm. Table II also shows the additive complexity achieved through the proposed fast algorithm is 40% lower when compared to direct computation of $\hat{\mathbf{F}}_{32}$.

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$$
\mathbf{A}_0 = \begin{bmatrix}
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1-1i & 1-1i & 1-1i & -1i & -1i & -1i & -1i & -1i & -1-1i & -1-1i & -1-1i & -1 & -1 \\
1 & 1 & 1-1i & -1i & -1i & -1i & -1-1i & -1 & -1 & -1 & -1+1i & 1i & 1i & 1i & 1+1i & 1 \\
1 & 1-1i & -1i & -1i & -1-1i & -1 & -1 & -1+1i & 1i & 1+1i & 1 & 1 & 1-1i & -1i & -1i & -1-1i \\
1 & 1-1i & -1i & -1-1i & -1 & -1+1i & 1i & 1+1i & 1 & 1-1i & -1i & -1-1i & -1 & -1+1i & 1i & 1+1i \\
1 & 1-1i & -1i & -1 & -1+1i & 1i & 1 & 1-1i & -1i & -1-1i & -1 & 1i & 1+1i & 1 & -1i & -1-1i \\
1 & -1i & -1-1i & -1 & 1i & 1 & 1-1i & -1i & -1 & 1i & 1+1i & 1 & -1i & -1 & -1+1i & 1i \\
1 & -1i & -1 & -1+1i & 1+1i & 1-1i & -1i & -1 & 1i & 1 & -1i & -1-1i & -1+1i & 1+1i & 1 & -1i \\
1 & -1i & -1 & 1i & 1 & -1i & -1 & 1i & 1 & -1i & -1 & 1i & 1 & -1 & -1i & 1i \\
1 & -1i & -1 & 1+1i & 1-1i & -1-1i & 1i & 1 & -1i & -1 & 1i & 1-1i & -1-1i & -1+1i & 1 & -1i \\
1 & -1i & -1+1i & 1 & -1i & -1 & 1+1i & -1i & -1 & 1i & 1-1i & -1 & 1i & 1 & -1-1i & 1i \\
1 & -1-1i & 1i & 1 & -1-1i & 1i & 1 & -1-1i & 1i & 1-1i & -1 & 1i & 1-1i & -1 & 1i & 1-1i \\
1 & -1-1i & 1i & 1-1i & -1 & 1+1i & -1i & -1+1i & 1 & -1-1i & 1i & 1-1i & -1 & 1+1i & -1i & -1+1i \\
1 & -1-1i & 1i & -1i & -1+1i & 1 & -1 & 1+1i & -1i & -1+1i & 1 & -1 & 1+1i & -1i & 1i & 1-1i \\
1 & -1 & 1+1i & -1i & 1i & -1i & -1+1i & 1 & -1 & 1 & -1-1i & 1i & -1i & 1i & 1-1i & -1 \\
1 & -1 & 1 & -1-1i & 1+1i & -1-1i & 1i & -1i & 1i & -1i & 1i & 1-1i & -1+1i & 1-1i & -1 & 1
\end{bmatrix}
$$

$$
\mathbf{A}_1 = \begin{bmatrix}
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
-1 & -1 & -1 & -1+1i & -1+1i & -1+1i & 1i & 1i & 1i & 1i & 1+1i & 1+1i & 1+1i & 1+1i & 1 & 1 \\
1 & 1 & 1-1i & -1i & -1i & -1i & -1-1i & -1 & -1 & -1 & -1+1i & 1i & 1i & 1i & 1+1i & 1 \\
-1 & -1+1i & 1i & 1i & 1+1i & 1 & 1 & 1-1i & -1i & -1-1i & -1 & -1 & -1+1i & 1i & 1i & 1+1i \\
1 & 1-1i & -1i & -1-1i & -1 & -1+1i & 1i & 1+1i & 1 & 1-1i & -1i & -1-1i & -1 & -1+1i & 1i & 1+1i \\
-1 & -1+1i & 1i & 1 & 1-1i & -1i & -1 & -1+1i & 1i & 1+1i & 1 & -1i & -1-1i & -1 & 1i & 1+1i \\
1 & -1i & -1-1i & -1 & 1i & 1 & 1-1i & -1i & -1 & 1i & 1+1i & 1 & -1i & -1 & -1+1i & 1i \\
-1 & 1i & 1 & 1-1i & -1-1i & -1+1i & 1i & 1 & -1i & -1 & 1i & 1+1i & 1-1i & -1-1i & -1 & 1i \\
1 & -1i & -1 & 1i & 1 & -1i & -1 & 1i & 1 & -1i & -1 & 1i & 1 & -1i & -1 & 1i \\
-1 & 1i & 1 & -1-1i & -1+1i & 1+1i & -1i & -1 & 1i & 1 & -1i & -1+1i & 1+1i & 1-1i & -1 & 1i \\
1 & -1i & -1+1i & 1 & -1i & -1 & 1+1i & -1i & -1 & 1i & 1-1i & -1 & 1i & 1 & -1-1i & 1i \\
-1 & 1+1i & -1i & -1 & 1+1i & -1i & -1 & 1+1i & -1i & -1+1i & 1 & -1i & -1+1i & 1 & -1i & -1+1i \\
1 & -1-1i & 1i & 1-1i & -1 & 1+1i & -1i & -1+1i & 1 & -1-1i & 1i & 1-1i & -1 & 1+1i & -1i & -1+1i \\
-1 & 1+1i & -1i & 1i & 1-1i & -1 & 1 & -1-1i & 1i & 1-1i & -1 & 1 & -1-1i & 1i & -1i & -1+1i \\
1 & -1 & 1+1i & -1i & 1i & -1i & -1+1i & 1 & -1 & 1 & -1-1i & 1i & -1i & 1i & 1-1i & -1 \\
-1 & 1 & -1 & 1+1i & -1-1i & 1+1i & -1i & 1i & -1i & 1i & -1i & -1+1i & 1-1i & -1+1i & 1 & -1
\end{bmatrix}
$$

$$
\mathbf{A}_2 = \begin{bmatrix}
1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\
1 & -1 & 1 & -1+1i & 1-1i & -1+1i & -1i & 1i & -1i & 1i & -1i & 1+1i & -1-1i & 1+1i & -1 & 1 \\
1 & -1 & 1-1i & 1i & -1i & 1i & -1-1i & 1 & -1 & 1 & -1+1i & -1i & 1i & -1i & 1+1i & -1 \\
1 & -1+1i & -1i & 1i & -1-1i & 1 & -1 & 1-1i & 1i & -1-1i & 1 & -1 & 1-1i & 1i & -1i & 1+1i \\
1 & -1+1i & -1i & 1+1i & -1 & 1-1i & 1i & -1-1i & 1 & -1+1i & -1i & 1+1i & -1 & 1-1i & 1i & -1-1i \\
1 & -1+1i & -1i & 1 & -1+1i & -1i & 1 & -1+1i & -1i & 1+1i & -1 & -1i & 1+1i & -1 & -1i & 1+1i \\
1 & 1i & -1-1i & 1 & 1i & -1 & 1-1i & 1i & -1 & -1i & 1+1i & -1 & -1i & 1 & -1+1i & -1i \\
1 & 1i & -1 & 1-1i & 1+1i & -1+1i & -1i & 1 & 1i & -1 & -1i & 1+1i & -1+1i & -1-1i & 1 & 1i \\
1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i \\
1 & 1i & -1 & -1-1i & 1-1i & 1+1i & 1i & -1 & -1i & 1 & 1i & -1+1i & -1-1i & 1-1i & 1 & 1i \\
1 & 1i & -1+1i & -1 & -1i & 1 & 1+1i & 1i & -1 & -1i & 1-1i & 1 & 1i & -1 & -1-1i & -1i \\
1 & 1+1i & 1i & -1 & -1-1i & -1i & 1 & 1+1i & 1i & -1+1i & -1 & -1i & 1-1i & 1 & 1i & -1+1i \\
1 & 1+1i & 1i & -1+1i & -1 & -1-1i & -1i & 1-1i & 1 & 1+1i & 1i & -1+1i & -1 & -1-1i & -1i & 1-1i \\
1 & 1+1i & 1i & 1i & -1+1i & -1 & -1 & -1-1i & -1i & 1-1i & 1 & 1 & 1+1i & 1i & 1i & -1+1i \\
1 & 1 & 1+1i & 1i & 1i & 1i & -1+1i & -1 & -1 & -1 & -1-1i & -1i & -1i & -1i & 1-1i & 1 \\
1 & 1 & 1 & 1+1i & 1+1i & 1+1i & 1i & 1i & 1i & 1i & 1i & -1+1i & -1+1i & -1+1i & -1 & -1
\end{bmatrix}
$$

$$
\mathbf{A}_3 = \begin{bmatrix}
1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\
-1 & 1 & -1 & 1-1i & -1+1i & 1-1i & 1i & -1i & 1i & -1i & 1i & -1-1i & 1+1i & -1-1i & 1 & -1 \\
1 & -1 & 1-1i & 1i & -1i & 1i & -1-1i & 1 & -1 & 1 & -1+1i & -1i & 1i & -1i & 1+1i & -1 \\
-1 & 1-1i & 1i & -1i & 1+1i & -1 & 1 & -1+1i & -1i & 1+1i & -1 & 1 & -1+1i & -1i & 1i & -1-1i \\
1 & -1+1i & -1i & 1+1i & -1 & 1-1i & 1i & -1-1i & 1 & -1+1i & -1i & 1+1i & -1 & 1-1i & 1i & -1-1i \\
-1 & 1-1i & 1i & -1 & 1-1i & 1i & -1 & 1-1i & 1i & -1-1i & 1 & 1i & -1-1i & 1 & 1i & -1-1i \\
1 & 1i & -1-1i & 1 & 1i & -1 & 1-1i & 1i & -1 & -1i & 1+1i & -1 & -1i & 1 & -1+1i & -1i \\
-1 & -1i & 1 & -1+1i & -1-1i & 1-1i & 1i & -1 & -1i & 1 & 1i & -1-1i & 1-1i & 1+1i & -1 & -1i \\
1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i \\
-1 & -1i & 1 & 1+1i & -1+1i & -1-1i & 1i & -1 & -1i & 1 & 1i & -1-1i & 1-1i & -1+1i & -1 & -1i \\
1 & 1i & -1+1i & -1 & -1i & 1 & 1+1i & 1i & -1 & -1i & 1-1i & 1 & 1i & -1 & -1-1i & -1i \\
-1 & -1-1i & -1i & 1 & 1+1i & 1i & -1 & -1-1i & -1i & 1-1i & 1 & 1i & -1+1i & -1 & -1i & 1-1i \\
1 & 1+1i & 1i & -1+1i & -1 & -1-1i & -1i & 1-1i & 1 & 1+1i & 1i & -1+1i & -1 & -1-1i & -1i & 1-1i \\
-1 & -1-1i & -1i & -1i & 1-1i & 1 & 1 & 1+1i & 1i & -1+1i & -1 & -1 & -1-1i & -1i & 1-1i & 1 \\
1 & 1 & 1+1i & 1i & 1i & 1i & -1+1i & -1 & -1 & -1 & -1-1i & -1i & -1i & -1i & 1-1i & 1 \\
-1 & -1 & -1 & -1-1i & -1-1i & -1-1i & -1i & -1i & -1i & -1i & -1i & 1-1i & 1-1i & 1-1i & 1 & 1
\end{bmatrix}
\quad (2)
$$

D. Hardware Metrics of the Proposed ADFT Realization

The 32-point ADFT fast algorithm in (3) was realized as a digital core and synthesized using 45 nm complementary metal–oxide–semiconductor (CMOS) free-process design kit (PDK) standard cells [39]. For comparison purposes, a 32-point FFT core based on the Duhamel algorithm was implemented digitally and synthesized using the same technology. Both the approximate and fixed point exact FFT digital cores assume inputs of 8 bit word length. The fixed-point exact FFT core was designed with 10 bit twiddle factors [30], which maintains a precision of 2^{-9} in the phasing coefficients. The multiplications throughout the signal paths were handled such that they preserve at least the coefficient precision. Table III gives the comparison of the following metrics for the two implementations: chip area A, critical path delay (CPD) T, maximum clock frequency F_{max}, area time (AT), area time-squared (AT^2), frequency- and voltage-normalized dynamic power consumption D_p, and maximum sidelobe level. It can be seen that the proposed ADFT algorithm consumes 46% less

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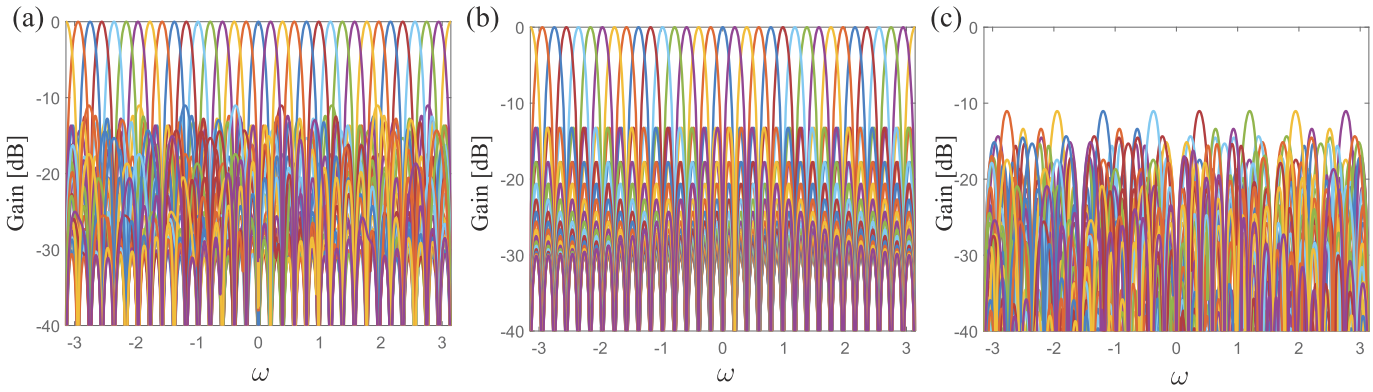

Fig. 2. Simulated frequency responses of the 32 output bins of the (a) proposed 32-point ADFT, (b) exact DFT, and (c) magnitude error of the two responses.

TABLE I

MATRIX FACTORS $\mathbf{W}_i$ REPRESENTED BY THEIR NONZERO INDEXES

Factorized Stage	$+1$	-1
$\mathbf{W}_1$	(1,1), (1,17), (2,2), (2,16), (3,3), (3,15), (4,4), (4,14), (5,5), (5,13), (6,6), (6,12), (7,7), (7,11), (8,8), (8,10), (9,9), (10,8), (11,7), (12,6), (13,5), (14,4), (15,3), (16,2), (17,1), (18,18), (18,32), (19,19), (19,31), (20,20), (20,30), (21,21), (21,29), (22,22), (22,28), (23,23), (23,27), (24,24), (24,26), (25,25), (26,24), (27,23), (28,22), (29,21), (30,20), (31,19), (32,18)	(10,10), (11,11), (12,12), (13,13), (14,14), (15,15), (16,16), (17,17), (26,26), (27,27), (28,28), (29,29), (30,30), (31,31), (32,32)
$\mathbf{W}_2$	(1,1), (2,2), (2,18), (3,3), (3,19), (4,4), (4,20), (5,5), (5,21), (6,6), (6,22), (7,7), (7,23), (8,8), (8,24), (9,9), (9,25), (10,10), (10,26), (11,11), (11,27), (12,12), (12,28), (13,13), (13,29), (14,14), (14,30), (15,15), (15,31), (16,16), (16,32), (17,17), (18,2), (19,3), (20,4), (21,5), (22,6), (23,7), (24,8), (25,9), (26,10), (27,11), (28,12), (29,13), (30,14), (31,15), (32,16)	(18,18), (19,19), (20,20), (21,21), (22,22), (23,23), (24,24), (25,25), (26,26), (27,27), (28,28), (29,29), (30,30), (31,31), (32,32)
$\mathbf{W}_3$	(1,1), (1,9), (2,2), (2,8), (3,3), (3,7), (4,4), (4,6), (5,5), (6,4), (7,3), (8,2), (9,1), (10,10), (10,16), (11,11), (11,15), (12,12), (12,14), (13,13), (14,12), (15,11), (16,10), (17,17), (18,18), (19,19), (20,20), (21,21), (22,22), (23,23), (24,24), (25,25), (26,26), (27,27), (28,28), (29,29), (30,30), (31,31), (32,32)	(6,6), (7,7), (8,8), (9,9), (14,14), (15,15), (16,16)
$\mathbf{W}_4$	(1,1), (1,5), (2,2), (2,4), (3,3), (4,2), (5,1), (6,6), (7,7), (7,9), (8,8), (9,7), (10,10), (11,11), (11,13), (12,12), (13,11), (14,14), (14,16), (15,15), (16,14), (17,17), (17,29), (18,18), (19,19), (20,20), (21,21), (21,25), (22,22), (23,23), (24,24), (25,21), (26,26), (27,27), (28,28), (29,17), (30,30), (31,31), (32,32)	(4,4), (5,5), (9,9), (13,13), (16,16), (25,25), (29,29)
$\mathbf{W}_5$	(1,1), (1,3), (2,2), (3,1), (4,4), (4,5), (5,4), (6,6), (6,9), (7,7), (7,8), (8,7), (9,6), (10,10), (10,13), (11,11), (11,12), (12,11), (13,10), (14,14), (14,15), (15,14), (16,16), (17,31), (18,18), (19,19), (19,25), (20,20), (20,22), (20,24), (21,21), (21,23), (22,20), (23,21), (24,20), (25,19), (26,26), (27,27), (27,29), (28,28), (28,30), (28,32), (29,27), (30,28), (31,17), (31,31), (32,28)	(3,3), (5,5), (8,8), (9,9), (12,12), (13,13), (15,15), (17,17), (22,22), (23,23), (24,24), (25,25), (29,29), (30,30), (32,32)
$\mathbf{W}_6$	(1,1), (1,2), (2,1), (3,3), (4,4), (5,5), (6,6), (7,7), (8,8), (9,9), (10,10), (11,11), (12,12), (13,13), (14,14), (15,15), (16,16), (17,17), (18,18), (18,22), (19,19), (20,20), (20,21), (21,20), (22,18), (23,23), (24,18), (24,24), (25,25), (26,26), (26,30), (27,27), (28,28), (28,31), (29,29), (30,26), (31,28), (32,26), (32,32)	(2,2), (18,24), (21,21), (22,22), (26,32), (30,30), (31,31)
$\mathbf{W}_7$	(1,1), (2,2), (3,3), (4,4), (5,5), (6,6), (7,7), (8,8), (9,9), (10,10), (11,11), (12,12), (13,13), (14,14), (15,15), (16,16), (17,17), (17,30), (18,18), (18,25), (19,24), (20,20), (21,21), (22,22), (22,23), (23,22), (24,19), (24,24), (25,18), (26,26), (26,27), (27,26), (28,28), (29,29), (29,32), (30,17), (31,31), (32,29)	(19,19), (23,23), (25,25), (27,27), (30,30), (32,32)

	$+1$	-1	$+j$	$-j$
$\mathbf{W}_8$	(1,1), (2,28), (3,7), (5,4), (6,26), (9,3), (11,9), (15,8), (17,2), (19,8), (23,9), (25,3), (28,26), (29,4), (31,7), (32,28)	(4,29), (7,6), (8,17), (10,30), (12,27), (13,5), (14,32), (16,31), (18,31), (20,32), (21,5), (22,27), (24,30), (26,17), (27,6), (30,29)	(5,14), (13,15), (15,12), (18,21), (20,19), (22,25), (23,13), (24,22), (25,16), (26,23), (27,10), (28,18), (30,24), (31,11), (32,20)	(4,24), (12,25), (14,19), (16,21), (19,12), (21,15)

area than the reference FFT-based design, while achieving a 50% drop in CPD. It is also noted that the metrics AT and AT^2 are reduced by 73% and 86%, respectively, where the metric AT is important when area/cost is more important, and AT^2 is critical when speed performance is crucial. Note that the speed values mentioned in Table III are only based on

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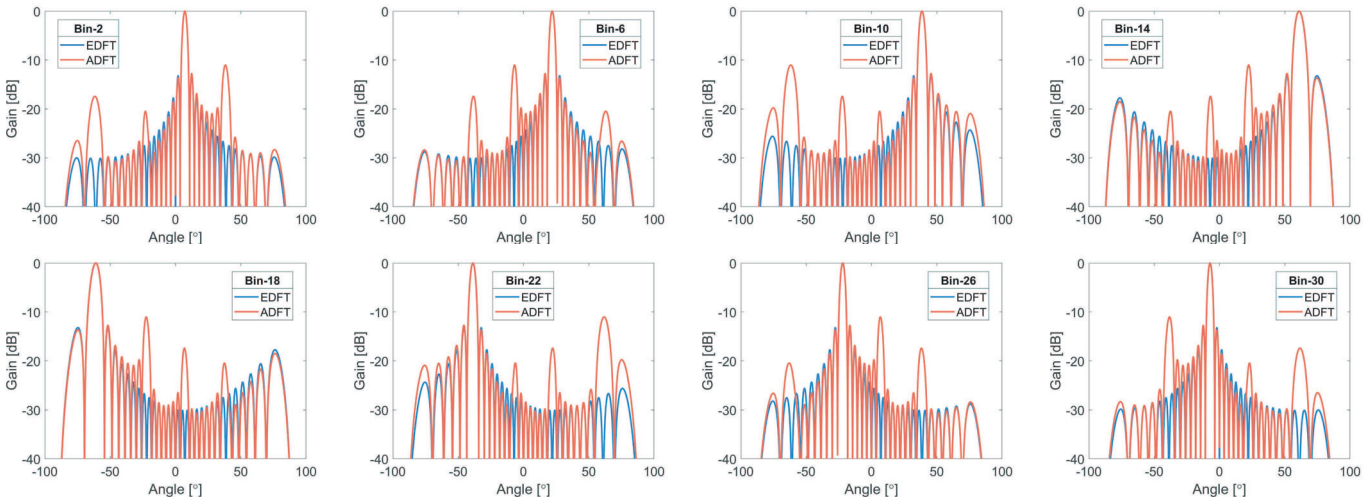

Fig. 3. Bins that have the highest magnitude error in Fig. 2(c).

TABLE II
COMPARISON OF ARITHMETIC COMPLEXITIES FOR PERFORMING THE 32-POINT DFT USING DIFFERENT FFT ALGORITHMS

Method	No. of real additions	No. of real multipliers
Radix-2 FFT [28, p. 76]	408	88
Split-Radix FFT [37]	388	68
Winograd FFT [38]	388	68
Direct Computation $\hat{\mathbf{F}}_{32}$	584	0
Fast Algorithm $\hat{\mathbf{F}}_{32}$	348	0

TABLE III
COMPARISON OF APPLICATION-SPECIFIED INTEGRATED CIRCUIT (ASIC) REALIZATION METRICS FOR THE PROPOSED ADFT VERSUS A 32-POINT FFT (DUHAMEL) USING A 45 nm PDK

Metric	Duhamel algorithm	ADFT	Change
Area, A (mm^2)	0.856	0.465	46%↓
Critical path delay, T (ns)	1.73	0.86	50%↓
Frequency, F_{max} (GHz)	0.58	1.16	100%↑
AT ($\text{mm}^2 \cdot \text{ns}$)	1.481	0.400	73%↓
AT^2 ($\text{mm}^2 \cdot \text{ns}^2$)	2.562	0.344	86%↓
Dynamic Power, D_p (mW/GHz)	1303	580	55%↓
Largest side-lobe level (dB)	−13.26	−11.03	2.23↑

**The proposed algorithm achieves $\approx 50\%$ reduction in area and time at the expense of $\approx$ 2dB increase in side lobe levels.

synthesis results, i.e., do not consider layout effects that slow down the performance of physical implementations. However, such effects will be present in both designs, so the relative improvements in AT and AT^2 metrics are expected to remain valid. The compromise is an $\approx$ 2 dB increase in sidelobe level, which we assume to be tolerable in most RF beamforming applications where unwanted signals (jammers) can fall on larger sidelobes.

E. N-Beam Beamforming Architectures for ULAs and URAs

Fig. 1 shows the top-level hardware architectures for realizing N and N^2 simultaneous orthogonal beams for an N-element and an $N \times N$ aperture, respectively, using an N-point spatial DFT digital core as the basic signal processing block. The front end is shown as a direct-conversion receiver chain followed by ADC for digital beamforming. The digitized data can be converted to complex (I–Q) form using a Hilbert transform. This can also be achieved by using a quadrature mixer in the RF chain, with the luxury of going to baseband directly at the cost of double the amount of ADCs.

The numerically simulated array factors resulting from a 32-element spatially Nyquist-sampled ULA are given in Fig. 4(i). Fig. 4(i-b) shows the beams generated using the proposed 32-point ADFT algorithm, and Fig. 4(i-a) shows the corresponding beams of the exact algorthm with (i-c) showing the error magnitude between them. Fig. 4(ii) shows three simulated example beams out of 1024 beams generated by the proposed ADFT algorithm when it is applied to a 32×32 element URA. Fig. 4(ii-d) and (ii-e) shows the beams corresponding to the exact and ADFT, respectively; Fig. 4(ii-f) and (ii-g) shows the errors between the two algorithms in the elevation and azimuthal planes, respectively, which are small enough to be ignored for most microwave and mmW beamforming applications.

IV. 32-BEAM ULA-BASED MULTIBEAM BEAMFORMER

The system architecture used for verifying the proposed low-complexity multibeam beamforming algorithm is shown in Fig. 5(a). This section explains the system design.

A. 5.8 GHz Front-End Design

The RF front end of the receive-mode beamformer is constructed by integrating a 32-element ULA at 5.8 GHz with

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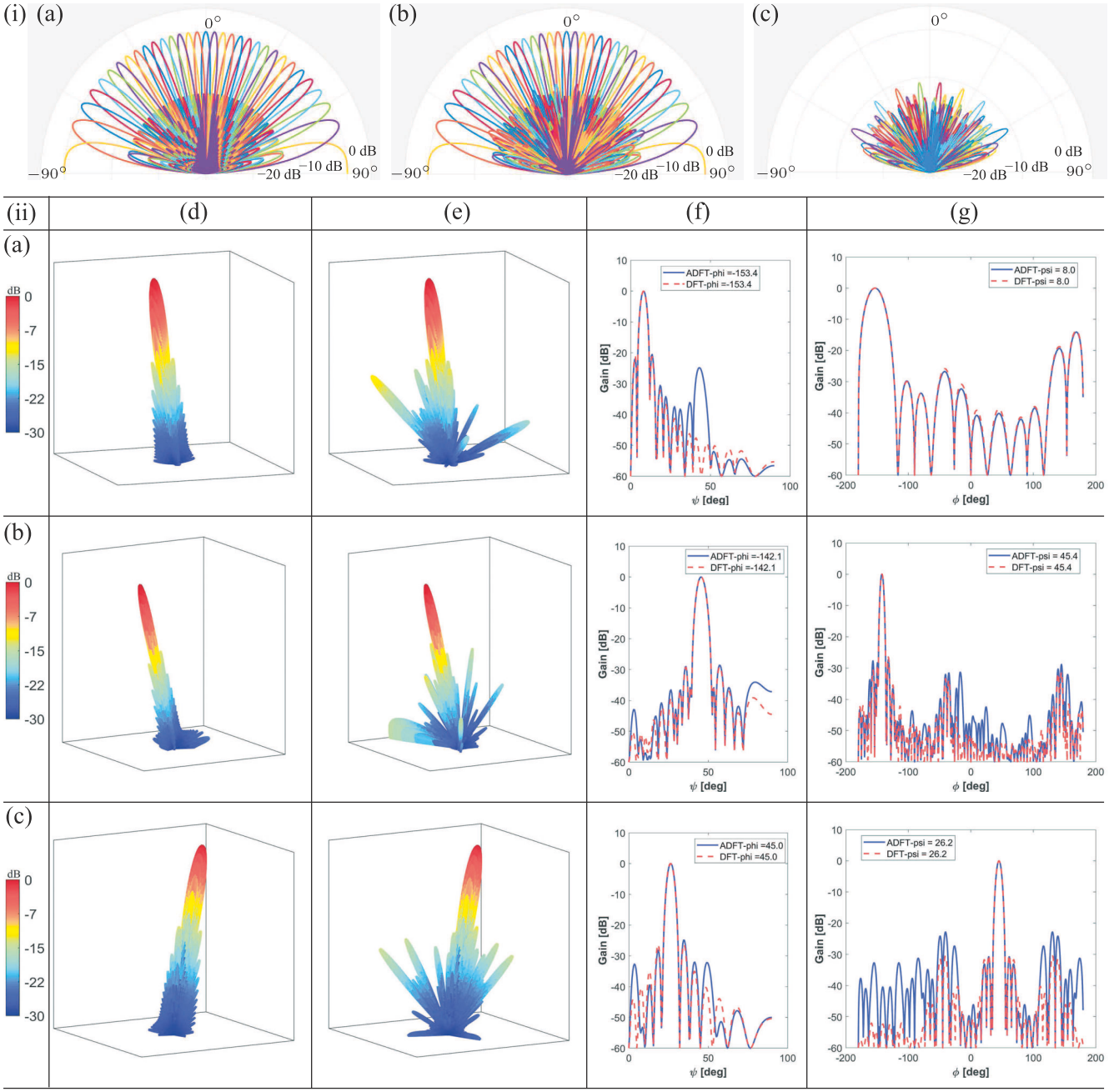

Fig. 4. (i) Simulated polar patterns of the 32 beams for an ULA with $\lambda/2$ element spacing. (i-a) Beams corresponding to the ADFT. (i-b) Beams obtained with the ideal FFT. (i-c) Magnitude error between the ADFT and the exact FFT. (ii) Example simulated beam patterns from a Nyquist-spaced URA. (ii-a) $\psi = 8.0°, \phi = -153.4°$. (ii-b) $\psi = 45.4°, \phi = -142.1°$. (ii-c) $\psi = 26.2°, \phi = 45.0°$ (the plots are color-coded on a decibel scale).

32 direct conversion RF receiver chains (on PCB) as shown in Fig. 5(b). The interelement spacing of the array Δx was set to 0.6λ, which is ≈ 31 mm at 5.8 GHz.

Each antenna element of the ULA was designed as a 4×1 vertical subarray of patch antennas that employ passive beamforming at RF in the orthogonal (vertical) plane. This design improves the gain in the vertical plane, thus simplifying array factor measurements in the azimuthal plane. In principle, such analog beamforming is independent of the 1-D/2-D spatial FFT-based beamforming algorithms discussed in this article. The subarray is designed by feeding antenna elements in series along a uniform transmission line and perform a parametric sweep to provide better impedance matching and performance [40]. Note that such analog beamforming does not affect the performance of the beamforming algorithm under consideration as it happens in the azimuthal plane. The specifications of the antenna array design are summarized in Table IV. The antenna outputs are directly fed into 32 heterodyne receivers designed on PCBs using surface-mount devices. The local oscillator (LO) signals for each receiver are provided through a centralized LO scheme that consists of a 32-output power divider network connected to

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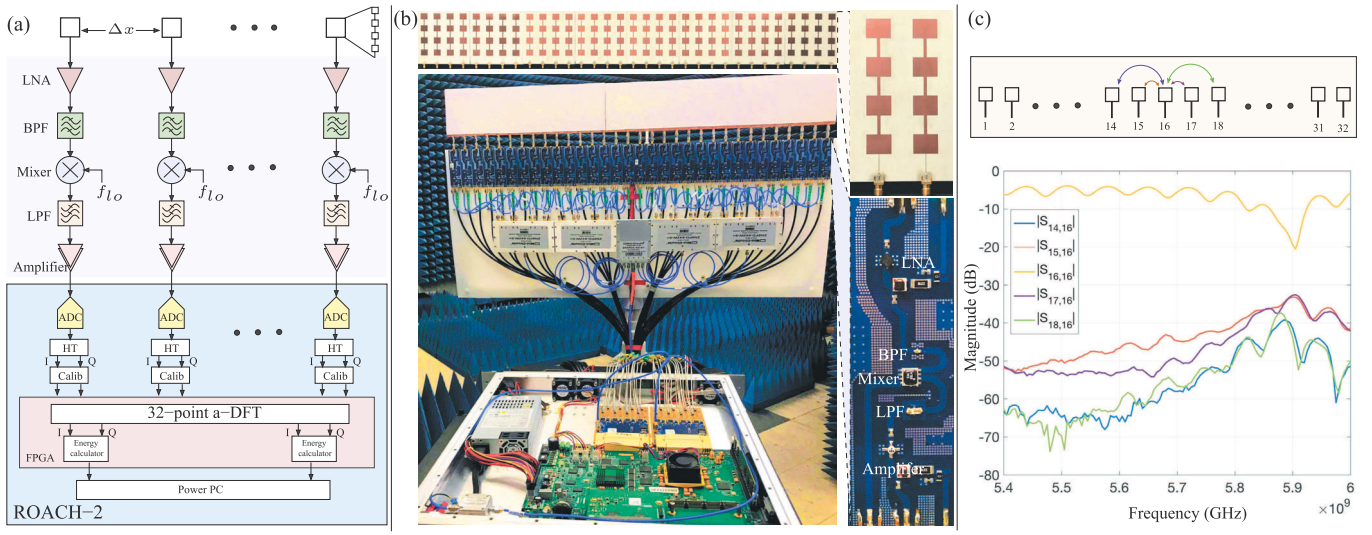

Fig. 5. (a) Overall architecture of the test setup. (b) 5.8 GHz 32-beam array receiver setup (starting at 2 m:44 s in the video in [48]). (c) Measured S-parameters (return loss and mutual coupling) of the designed antenna array.

TABLE IV
DESIGN SPECIFICATIONS FOR THE PATCH ANTENNA

Frequency (f_0)	5.8 GHz
Substrate	Rogers RO4350B
Dielectric constant (ϵ_r)	3.66
Substrate thickness (h)	0.508 mm
Conductor (copper) thickness (ct)	35 μm

a low-phase-noise oscillator. The first stage of each receiver consists of a low-noise amplifier (LNA) that provides 16 dB gain at 5.8 GHz with a noise figure of 2.4 dB. The amplified signal is bandpass filtered within the frequency range 4.7–6 GHz, which helps to reject the out-of-band interference and noise. The band-limited amplified signal is then passed through a mixer and low-pass filter to produce a downconverted low-IF input. The 32 downconverted low-IF signals are further amplified by $\sim$30 dB and then digitized in parallel using two ADC16x250-8 ADC cards (16 single-ended input channels, 8 bit, up to 250 MS/s per channel) [41]. The in-band gain and noise figure of the entire receiver are estimated to be 38.6 and 2.9 dB, respectively; the latter is dominated by the LNA.

The ADCs used a sample clock of 200 MHz for real-time hardware experiments. The same clock was also routed to the digital circuits implemented on the field-programmable gate arrays (FPGAs). The clock frequency was chosen to be smaller than the maximum allowed for the digital design, which is limited by the CPD and thus denoted by $f_{max,CPD}$.

B. Digital Back End

Digital processing of sampled signals was performed using the reconfigurable open architecture computing hardware (ROACH-2) platform [42] designed by the Collaboration for Astronomy Signal Processing and Electronics Research (CASPER). ROACH-2 is based on a Xilinx Virtex-6 FPGA chip; it also includes an integrated on-board processor that handles communications and control functions with the FPGA. The platform has two ZDOK interfaces (each supporting 42 pins) that connects high bandwidth input–output (I/O) to the FPGA. The ADC16x250-8 ADC cards mentioned previously were designed to be compatible with the ROACH-2 hardware and can be accessed using CASPER-supplied software routines. These routines, which are available at [43], also allow the ADCs to be calibrated.

The overall architecture of the digital beamforming test setup is shown in Fig. 5(a). The digital design consists of four main subsystems: 1) a digital calibration stage; 2) an I-Q decomposition FIR filter that implements the Hilbert transform [44]; 3) the 32-point DFT/ADFT algorithm implementation; and 4) an energy calculation subsystem for facilitating real-time measurements on each output beam. The exact DFT core was designed using 10 bit precision twiddle factors which provide a good compromise between circuit size and maximum operating frequency.

V. EXPERIMENTAL RESULTS

This section describes experimental results obtained from the 32-element ULA, including antenna characterization and beam measurements.

A. Antenna Array Characterization

The performance of the array can be characterized using S-parameters [45], which were measured using a commercial vector network analyzer. For example, the return loss of the mth antenna, which represents the amount of power reflected from it, is given by $|S_{m,m}|$. The measured return loss for $m = 16$, namely $|S_{16,16}|$, is shown in Fig. 5(c). The proposed patch antenna resonates at a frequency of 5.9 GHz with an excellent return loss of -20.6 dB.

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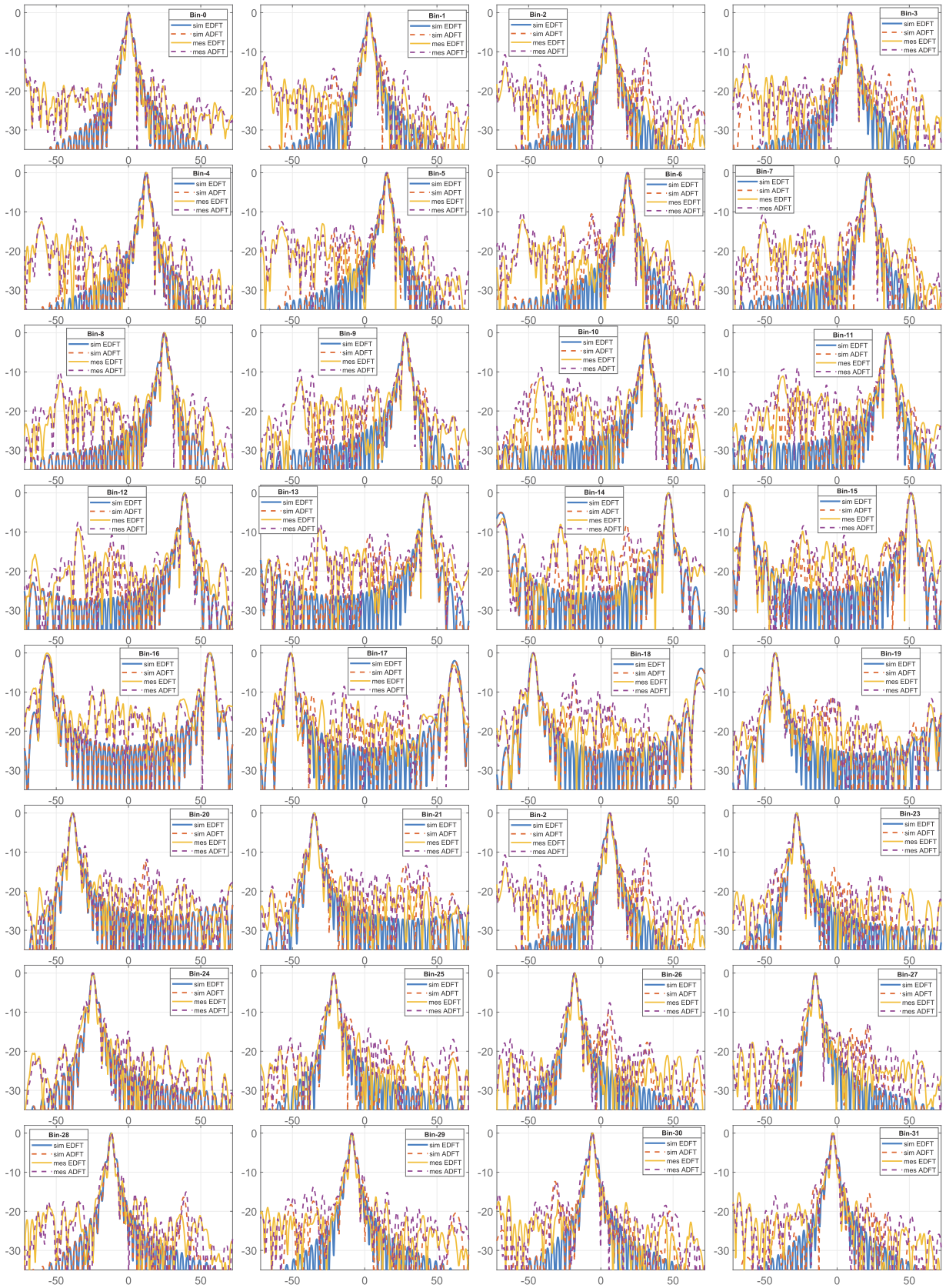

Fig. 6. 32 beams measured from the 5.8 GHz array (vertical axis is in decibel and the horizontal axis is the azimuthal angle $[-72, 72]$). Each subfigure contains the measured beams pattern using the fixed-point FFT digital core, the ADFT core, and the simulated beams for both scenarios. Simulated beams account antenna element pattern and the actual separation of the transmitter and the receiver in the measurement setup.

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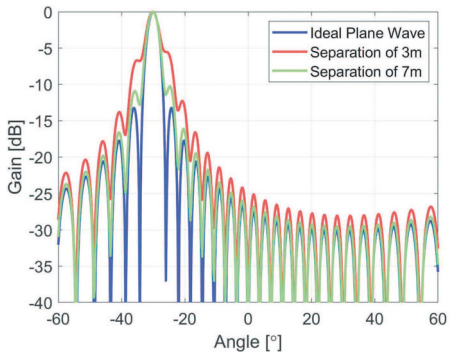

Fig. 7. Impact of the measurement setup geometry on the measured beam response.

Mutual coupling is another important issue during the design of an antenna array. In an array, the fields radiated by individual elements tend to interact with each other, thus causing interchange of energy [46]. Mutual coupling describes the energy absorbed by one antenna when a nearby antenna is operating and depends upon many factors including antenna design parameters, interelement spacing, and the direction of arrival (DOA) of the wave [47]. It can also be measured using S-parameters. Specifically, $S_{n,m}$ is a measure of coupling between ports m and n. We measured the mutual coupling between an antenna element and its nearest neighbors using $S_{n,m}$ measurements. In particular, we measured $S_{14,16}$, $S_{15,16}$, $S_{17,16}$, and $S_{18,16}$, which characterize the coupling between ports 16 and its near neighbors (ports 14, 15, 17, and 18). The results are shown in Fig. 5(c) versus frequency: the values at 5.8 GHz are relatively low and given by $|S_{14,16}| = -39.2$ dB, $|S_{15,16}| = -33.2$ dB, $|S_{17,16}| = -33.0$ dB, and $|S_{18,16}| = -37.3$ dB. As expected, mutual coupling decreases with interelement separation.

B. Calibration

Calibration of the RF array system is vital for obtaining optimal beamforming performance. Calibration was performed in two stages. The first stage was performed on the ADCs, and used open-source routines that have already been developed for the same hardware by members of the CASPER group [43]. The second stage focused on digitally removing the effects of mismatches in the microwave front end. Relative gain and phase mismatches of the IF outputs for each chain were calculated with respect to a reference chain using an input reference carrier at 5.86 GHz. Since the overall system is narrowband, the recorded gain and phase values were directly used to equalize the gain and phase of the sampled IF inputs. This was achieved by adding a complex multiplier after the digital Hilbert transform in each channel.

C. Beam Measurements

As shown in Fig. 5(b), the entire 5.8 GHz 32-element digital array placed in an anechoic chamber for measuring the received beam patterns ([48] shows a short real-time demo of the total system). Power patterns were measured by sending a continuous-wave (CW) signal at $f_{RF} = 5.86$ GHz. The LO signal frequency f_{LO} determines the IF $f_{RF} - f_{LO}$. The measurements, in this article, were generated by setting $f_{LO} = 5.85$ GHz, thus resulting in an IF of 10 MHz, and digitizing the downconverted outputs at $f_{clk} = 200$ MHz. Fig. 6 shows the measured beams from the real-time experimental setup for both the exact and approximate algorithms along with the corresponding simulated curves. The measurement was conducted using digital integrators at each FFT/ADFT bin output to calculate the received energy for a fixed amount of time.

The measured array factor of the beams highly depends on the measurement setup geometry. Ideally, the transmitter and the receiver should be placed far enough apart for waves incident on the receiver array to be approximated as plane waves. Numerical simulation in Fig. 7 shows how the actual array factor being measured deviates from this ideal depending on the geometry of the test setup. Based on the standard rules [49, p. 42], the transmitter and receiver should have a separation exceeding 20 m at 5.8 GHz in order for the receiver aperture to be in the far-field. However, such a large separation was not achievable within our test facility. In particular, the beams were measured in an open parking deck with a transmitter–receiver separation of approximately 7 m. Due to this reason, the measured beams shown in Fig. 6 have been compared with numerically simulated beams that account for both finite transmitter–receiver separation and the actual element pattern.

Fig. 6 shows that the measured beam patterns for both the algorithms closely follow each other for all the bins. The measured beams also follow the expected patterns quite well in the vicinity of the main beam. For both algorithms, the measured plots have higher sidelobe levels in the deeper stop bands compared to the simulated ones. We believe that such degradation in stopband performance is mainly due to postcalibration errors of the system; these are dominated by the performance of the analog front ends in the receiver. Measurement errors, including the fact that the tests were not performed in an anechoic environment, also lead to deviations from the expected patterns.

The 2-D array factor of each beam arising from the proposed linear transform can be expressed as

$$\Psi_{k,l}(\omega_x, \omega_y) = \sum_{n=0}^{31} \sum_{m=0}^{31} [\hat{\mathbf{F}}_{32}(k,m)\hat{\mathbf{F}}_{32}(l,n)e^{-j(\omega_x \Delta x m + \omega_y \Delta y n)}], \tag{4}$$

which may be rearranged to

$$\Psi_{k,l}(\omega_x, \omega_y) = \left(\sum_{m=0}^{31} \hat{\mathbf{F}}_{32}(k,m)e^{-j\omega_x \Delta x m}\right) \times \left(\sum_{n=0}^{31} \hat{\mathbf{F}}_{32}(l,n)e^{-j\omega_y \Delta y n}\right) \tag{5}$$

$$= \Upsilon(k, \omega_x) \times \sum_{n=0}^{31} \hat{\mathbf{F}}_{32}(l,n)e^{-j\omega_y \Delta y n}, \tag{6}$$

where $k, l \in [0, 1, \ldots, 31]$, $\omega_x = \omega_{ct} \sin\psi \cos\phi$, $\omega_y = \omega_{ct} \sin\psi \cos\phi$, ψ and ϕ are elevation and azimuthal angles,

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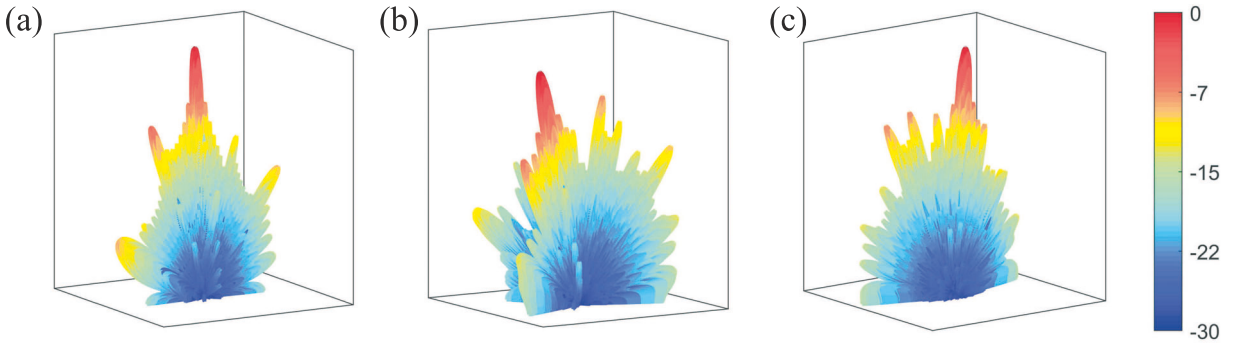

Fig. 8. (a)–(c) 2-D beam patterns computed from 1-D array beam measurements using the ADFT algorithm. The beams correspond to the bin outputs (same angles) as the beams shown in Fig. 4(a)–(c).

respectively. Δx and Δy denote the interelement spacing in the x- and y-directions. The relationship in (6) can be used to compute the 2-D beam responses corresponding to a 2-D URA consisting of 32 linear arrays, each with the measured responses shown in Fig. 6. In particular, the term $\Upsilon(k, \omega_x)$ denotes the array factor of the kth beam in the 32-element linear array subsystem. The measured 1-D beam patterns were thus used in place of $\Upsilon(k, \omega_x)$ to synthesize the corresponding 2-D beam patterns from a 2-D aperture. Fig. 8 shows the 2-D beam patterns obtained using the measured ULA beam measurements for the same beams shown in Fig. 4 assuming $\Delta x = \Delta y$.

VI. Conclusion

A large number of simultaneous beams has become an essential requirement for emerging mmW-based 5G systems. Moreover, future communication applications, such as space-based Internet services, demand an ultrahigh number of beams. An $N \times N$ square antenna array aperture can generate up to N^2 orthogonal simultaneous beams using the 2-D N-point spatial DFT. The upper bound of the multiplicative complexity associated with such processing using FFT algorithms is $\mathcal{O}(2N^2 \log N)$. This article has discussed a low-complexity digital beamforming architecture for generating 1024 simultaneous RF beams using a 32-point DFT approximation that completely eliminates multiplication operations. The proposed ADFT algorithm consumes 46% less chip area than the reference FFT-based design, while achieving a 50% drop in CPD. The VLSI metrics AT and AT^2 for the proposed algorithm are reduced by 73% and 86%, respectively. We have validated the proposed approach on a fully functional 32-element digital 1-D receive array that operates at 5.8 GHz. This design will serve as the main subsystem for future implementations of a 32×32 2-D rectangular aperture that could generate 1024 simultaneous RF beams with significantly lower SWaP in VLSI implementations. The 1-D array uses 32 parallel ADCs for sampling the antenna outputs and the ADFT (implemented on a Xilinx FPGA) for computing 32 RF beams in real time. The measured RF beams show a per-beam bandwidth of 120 MHz when all 32 beams are realized in real time, with only marginal (<2 dB) degradation in side lobe performance compared to a control experiment based on the Duhamel FFT core.

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References

[1] W. Rotman and R. F. Turner, "Wide-angle microwave lens for line source applications," *IEEE Trans. Antennas Propag.*, vol. AP-11, no. 6, pp. 623–632, Nov. 1963.

[2] H. Moody, "The systematic design of the Butler matrix," *IEEE Trans. Antennas Propag.*, vol. AP-12, no. 6, pp. 786–788, Nov. 1964.

[3] N. J. G. Fonseca, "Printed S-band 4 × 4 Nolen matrix for multiple beam antenna applications," *IEEE Trans. Antennas Propag.*, vol. 57, no. 6, pp. 1673–1678, Jun. 2009.

[4] S. Sun, T. S. Rappaport, M. Shafi, and H. Tataria, "Analytical framework of hybrid beamforming in multi-cell millimeter-wave systems," *IEEE Trans. Wireless Commun.*, vol. 17, no. 11, pp. 7528–7543, Nov. 2018.

[5] S. Sun, T. S. Rappaport, M. Shafi, P. Tang, J. Zhang, and P. J. Smith, "Propagation models and performance evaluation for 5G millimeter-wave bands," *IEEE Trans. Veh. Technol.*, vol. 67, no. 9, pp. 8422–8439, Sep. 2018.

[6] C. Fulton, M. Yeary, D. Thompson, J. Lake, and A. Mitchell, "Digital phased arrays: Challenges and opportunities," *Proc. IEEE*, vol. 104, no. 3, pp. 487–503, Mar. 2016.

[7] T. S. Rappaport *et al.*, "Wireless communications and applications above 100 GHz: Opportunities and challenges for 6G and beyond," *IEEE Access*, vol. 7, pp. 78729–78757, 2019.

[8] D. R. Bull and D. H. Horrocks, "Primitive operator digital filters," *IEE Proc. G Circuits, Devices Syst.*, vol. 138, no. 3, pp. 401–412, Jun. 1991.

[9] W. Hong *et al.*, "Multibeam antenna technologies for 5G wireless communications," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6231–6249, Dec. 2017.

[10] T. S. Rappaport, Y. Xing, G. R. MacCartney, A. F. Molisch, E. Mellios, and J. Zhang, "Overview of millimeter wave communications for fifth-generation (5G) wireless networks—With a focus on propagation models," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6213–6230, Dec. 2017.

[11] D. Choudhury, "5G wireless and millimeter wave technology evolution: An overview," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4.

[12] S. Sun, T. S. Rappaport, and M. Shaft, "Hybrid beamforming for 5G millimeter-wave multi-cell networks," in *Proc. IEEE Conf. Comput. Commun. Workshops (INFOCOM WKSHPS)*, Apr. 2018, pp. 589–596.

[13] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "An ultra low-cost 32-element 28 GHz phased-array transceiver with 41 dBm EIRP and 1.0–1.6 Gbps 16-QAM link at 300 meters," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 73–76.

[14] M. K. Khattak, C. Lee, D. Han, and S. Kahng, "Flat Rotman lens for 5G beamforming antenna," in *Proc. IEEE 5th Asia–Pacific Conf. Antennas Propag. (APCAP)*, Jul. 2016, pp. 205–206.

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[15] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A 28 GHz transceiver chip for 5G beamforming data links in SiGe BiCMOS," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Oct. 2017, pp. 74–77.
[16] R. Chen, H. Xu, C. Li, L. Zhu, and J. Li, "Hybrid beamforming for broadband millimeter wave massive MIMO systems," in *Proc. IEEE 87th Veh. Technol. Conf. (VTC Spring)*, Jun. 2018, pp. 1–5.
[17] M. Sayginer and G. M. Rebeiz, "An eight-element 2–16-GHz programmable phased array receiver with one, two, or four simultaneous beams in SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4585–4597, Dec. 2016.
[18] J. Lota, S. Sun, T. S. Rappaport, and A. Demosthenous, "5G uniform linear arrays with beamforming and spatial multiplexing at 28, 37, 64, and 71 GHz for outdoor urban communication: A two-level approach," *IEEE Trans. Veh. Technol.*, vol. 66, no. 11, pp. 9972–9985, Nov. 2017.
[19] (Jul. 2018). *3GPP the Mobile Broadband Standard*. Accessed: Oct. 2018. [Online]. Available: http://www.3gpp.org/release-15
[20] J. Jeong, N. Collins, and M. P. Flynn, "A 260 MHz IF sampling bit-stream processing digital beamformer with an integrated array of continuous-time band-pass $\Delta\Sigma$ modulators," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1168–1176, May 2016.
[21] S. Jang, J. Jeong, R. Lu, and M. P. Flynn, "A 16-element 4-beam 1 GHz IF 100 MHz bandwidth interleaved bit stream digital beamformer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1302–1312, May 2018.
[22] T. Okuyama *et al.*, "Experimental evaluation of digital beamforming for 5G multi-site massive MIMO," in *Proc. 20th Int. Symp. Wireless Pers. Multimedia Commun. (WPMC)*, Dec. 2017, pp. 476–480.
[23] P. Xingdong, H. Wei, Y. Tianyang, and L. Linsheng, "Design and implementation of an active multibeam antenna system with 64 RF channels and 256 antenna elements for massive MIMO application in 5G wireless communications," *China Commun.*, vol. 11, no. 11, pp. 16–23, Nov. 2014.
[24] R. Miura, T. Tanaka, I. Chiba, A. Horie, and Y. Karasawa, "Beamforming experiment with a DBF multibeam antenna in a mobile satellite environment," *IEEE Trans. Antennas Propag.*, vol. 45, no. 4, pp. 707–714, Apr. 1997.
[25] V. Ariyarathna, D. F. G. Coelho, S. Pulipati, R. J. Cintra, F. M. Bayer, V. S. Dimitrov, and A. Madanayake, "Multibeam digital array receiver using a 16-point multiplierless DFT approximation," *IEEE Trans. Antennas Propag.*, vol. 67, no. 2, pp. 925–933, Feb. 2019.
[26] W. Liu and S. Weiss, *Wideband Beamforming: Concepts and Techniques* (Wireless Communications and Mobile Computing). Hoboken, NJ, USA: Wiley, 2010.
[27] B. Wang *et al.*, "Spatial-wideband effect in massive MIMO with application in mmWave systems," *IEEE Commun. Mag.*, vol. 56, no. 12, pp. 134–141, Dec. 2018.
[28] R. E. Blahut, *Fast Algorithms for Digital Signal Processing*. Cambridge, U.K.: Cambridge Univ. Press, 2010.
[29] R. Graham, D. Knuth, and O. Patashnik, *Concrete Mathematics: A Foundation for Computer Science* (A Foundation for Computer Science). Reading, MA, USA: Addison-Wesley, 1994.
[30] W. M. Gentleman and G. Sande, "Fast Fourier transforms: For fun and profit," in *Proc. AFIPS*, New York, NY, USA, 1966, pp. 563–578.
[31] R. J. Cintra, "An integer approximation method for discrete sinusoidal transforms," *Circuits, Syst., Signal Process.*, vol. 30, no. 6, pp. 1481–1501, 2011.
[32] M. Ehrgott, *Multicriteria Optimization*, 2nd ed. Springer, 2005.
[33] D. Suárez, "Aproximações para a transformada discreta de Fourier e aplicações em deteção e estimação," M.S. thesis, Univ. Federal Pernambuo, Recife, Brazil, 2015.
[34] D. Suarez, R. J. Cintra, F. M. Bayer, A. Sengupta, S. Kulasekera, and A. Madanayake, "Multi-beam RF aperture using multiplierless FFT approximation," *Electron. Lett.*, vol. 50, no. 24, pp. 1788–1790, 2014.
[35] V. A. Coutinho, V. Ariyarathna, D. F. G. Coelho, R. J. Cintral, and A. Madanayake, "An 8-beam 2.4 GHz digital array receiver based on a fast multiplierless spatial DFT approximation," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 1538–1541.
[36] D. M. Burton, *Elementary Number Theory*, 7th ed. New York, NY, USA: McGraw-Hill, 2010.
[37] P. Duhamel and H. Hollmann, "'Split radix' FFT algorithm," *Electron. Lett.*, vol. 20, no. 1, pp. 14–16, Jan. 1984.
[38] S. Winograd, *Arithmetic Complexity of Computations* (CBMS-NSF Regional Conference Series in Applied Mathematics). 1980. [Online]. Available: https://books.google.com/books/about/Arithmetic_Complexity_of_Computations.html?id=eWb9EF7BmCYC
[39] (2009). *45 nm Free Process Design Kit*. [Online]. Available: https://www.eda.ncsu.edu/wiki/FreePDK45:Contents
[40] R. A. Sainati, *CAD of Microstrip Antennas for Wireless Applications*. Norwood, MA, USA: Artech House, 1996.
[41] CASPER. *ADC16x250-8 COAX Rev 2 Daughter Cards*. [Online]. Available: https://casper.berkeley.edu/wiki/ADC16x250-8_coax_rev_2
[42] CASPER. (Oct. 2013). *Reconfigurable Open Architecture Computing Hardware (ROACH-2) FPGA Platform*. Accessed: Feb. 2018. [Online]. Available: https://casper.berkeley.edu/wiki/ROACH-2Revision2
[43] Department of Astronomy, University of Berkeley. (2014). *Calibrating ADC16x250-8 ADCs*. Accessed: Mar. 2016. [Online]. Available: http://w.astro.berkeley.edu/~davidm/gems/
[44] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2009.
[45] D. M. Pozar, *Microwave Engineering*. Hoboken, NJ, USA: Wiley, 2009.
[46] C. A. Balanis, *Antenna Theory: Analysis and Design*. Hoboken, NJ, USA: Wiley, 2016.
[47] H. Singh, H. L. Sneha, and R. M. Jha, "Mutual coupling in phased arrays: A review," *Int. J. Antennas Propag.*, vol. 2013, Mar. 2013, Art. no. 348123.
[48] *Ted Tours the 2018 Brooklyn 5G Summit Expo*. Accessed: Sep. 2018. [Online]. Available: https://ieeetv.ieee.org/ieeetv-specials/ted-tours-the-brooklyn-5g-summit-expo-floor-3
[49] W. L. Stutzman and G. A. Thiele, *Antenna Theory and Design* (Antenna Theory and Design). Hoboken, NJ, USA: Wiley, 2012.

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