32-Element Array Receiver for 2-D Spatio-Temporal Δ-Σ Noise-Shaping

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***Abstract*—The concept of two-dimensional (2-D) space-time Δ-Σ noise-shaping for radio frequency (RF) array processing systems has been proposed in earlier work. This approach can provide supralinear improvements in the overall noise figure (NF), linearity, and resolution of an N-port receiver at the cost of a linear increase in the number of elements. This paper describes a proof-of-concept 32-element array receiver that is suitable for driving first-order spatio-temporal Δ-Σ noise-shaping analog-to-digital converters (ADCs). The design has been realized using board-level components. It operates at a center frequency of 2.6 GHz and uses an on-board dense sleeve monopole antenna array with a spatial oversampling factor of 4. Calibration is achieved to decrease the mismatch between channels, resulting in gain mismatch reduction by a factor of 1.8 and phase mismatch reduction by a factor of 2.9. Over-the-air measurement results prove the functionality of the proposed array receiver.**

I. Introduction

Microwave and mm-wave spectral bands are critical for emerging applications in wireless communications, radio astronomy, radar, and imaging due to their large bandwidth and high directionality [1]. However, microwave and mm-wave channels also suffer from relatively high propagation losses. Narrow RF beams generated by multi-channel phased-array receivers are commonly used to improve system link budgets by reducing these losses. State-of-the-art transceivers for N-element arrays simply replicate N high-sensitivity receivers (or modular transmitters) at each element in the array in order to create an N-element aperture [2]. This approach is not optimal because it ignores the physical relationships that must exist between signals, noise, interference, and non-linear distortion across the elements of the array. In order to solve the above issues, our previous work [3]–[7] has demonstrated that multi-dimensional (2-D or 3-D) spatio-temporal Δ-Σ noise-shaping can greatly improve the linearity, noise figure, and ADC resolution of such phased-array receivers.

The idea of spatio-temporal Δ-Σ noise-shaping [8] comes from the fact that Special Relativity defines a region of causality (i.e., the light cone) outside which no propagating electromagnetic waves can exist [9], [10]. Therefore, spatially-oversampled arrays shown in Fig. 1(a) i) compress the light cone of the input signals (i.e., their region of support (ROS)) such that it occupies a smaller portion of the 2-D (space, time) frequency domain as shown in Fig. 1(b); and ii) spectrally shape the noise and distortion from practical amplifiers, mixers, and ADCs to higher spatial frequencies such that they do not overlap with the compressed light cone as shown in Fig. 1(c). These unwanted signals can be easily removed by spatial low-pass filtering, as shown in Fig. 1(d) [3], [11].

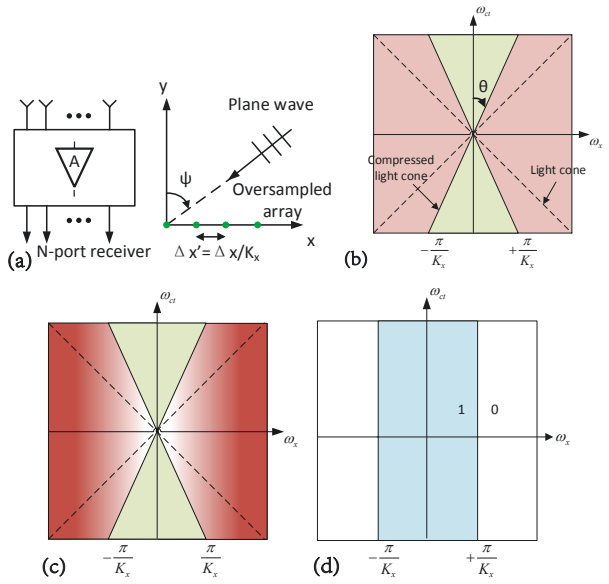

Fig. 1. (a) A K_x-times spatially-oversampled antenna array, i.e., with an antenna spacing of $\lambda/(2K_x)$ where λ is the EM wavelength; (b) The ROS of waves received by the array (green), which consists of a narrow light cone that overlaps with receiver noise and distortion (red); (c) Spatial Δ-Σ noise-shaping ensures that noise lies outside the ROS of the received signals; (d) A space-time low-pass filter removes shaped noise from the outputs.

In previous work, we have experimentally verified the proposed spatio-temporal noise-shaping method by developing and testing a low-speed ($f_s < 40$ MHz) discrete 64-channel board-level ADC (4 boards in total with 16 channels per board) based on 1-bit quantization [5]. Although the measured performance proved the functionality of the noise-shaping concept, the converter was only tested by applying broadband input signals from a signal generator. Such inputs correspond to amplitude- and phase-modulated plane waves after amplification and downconversion to baseband. In order to design a complete array receiver and test it with real RF signals, here we propose a board-level spatially-oversampled receiver system, including antennas to receive over-the-air RF signals, an analog front-end (AFE) to downconvert the signal to baseband, a programmable gain amplifier (PGA) stage

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to change the signal amplitudes, and a phase compensation stage to compensate the phase mismatch between all the baseband outputs. The proposed system can directly drive the previously-mentioned 64-channel ADC to realize complete digital array receivers with 2-D Δ-Σ noise-shaping.

II. System Design

A. Array Board Design

The block diagram of the discrete array receiver board is shown in Fig. 2. There are 16 elements per board, resulting in a 32-element array receiver when two boards are aligned together. Note that each channel generates baseband I/Q outputs, resulting in a total of 64 outputs. The receiver board uses an on-board 32-port dense sleeve monopole antenna array with a center frequency of 2.6 GHz. The planar array uses a spatial oversampling factor of $K_u = 4$ and coplanar waveguide (CPW) feeds with ground-shorted sleeves to minimize coupling between adjacent elements. Both simulations and measurements show a peak element gain of -5 dBi [12].

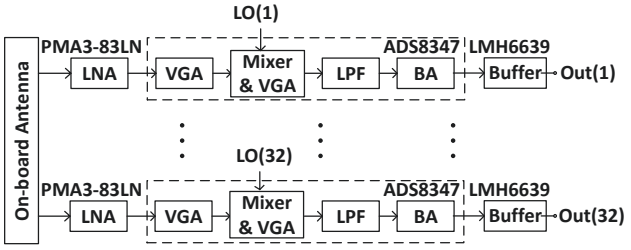

Fig. 2. Block diagram of the 32-element array receiver board.

The on-board antenna outputs are fed to broadband low-noise amplifiers (LNAs) in each channel. The chosen LNA (PMA3-83LN from Mini Circuits) uses pHEMTs to obtain i) a low noise figure of 1.3 dB at 2 GHz, and ii) flat gain of 22.1$\pm$0.9 dB over the frequency range from 0.5 to 8 GHz. After the LNAs, we use broadband direct quadrature demodulators (AD8347 from Analog Devices) that i) include RF and baseband amplifiers with automatic gain control (AGC), and ii) support an input frequency range of 800 MHz to 2.7 GHz, making them suitable for our 2.6 GHz design. Each demodulator passes the RF signal from an LNA through two stages of variable gain amplifiers (VGAs) prior to demodulation by two Gilbert-cell mixers. An on-chip quadrature phase splitter for the local oscillator (LO) employs polyphase filters to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range. Separate I and Q channel VGAs follow the baseband outputs of the mixers. The outputs of the baseband VGAs are brought off-chip into third-order Butterworth low-pass filters (LPFs) with a cut-off frequency of 30 MHz. The filtered signals are sent back to on-chip baseband output amplifiers that provide a final amplification of 30 dB.

The RF and baseband VGAs together provide 69.5 dB of gain control (-30 to $+39.5$ dB), resulting in a total receiver gain of 22.1-91.6 dB. The use of a precision gain control circuit results in a linear-in-dB RF gain response to the gain control voltage. In particular, the AGC loop uses baseband level detectors to control the VGAs such that the maximum output amplitude of the demodulator is limited to approximately 380 mV. These baseband I and Q outputs are fed to baseband buffers (LMH6639 from Texas Instruments) so that the receiver can properly drive the following boards.

B. PGA Board Design

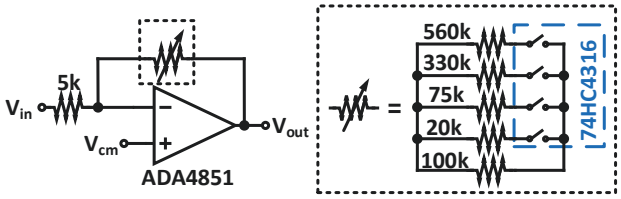

Fig. 3. Schematic of the PGA stage to vary the baseband signal amplitudes. A resistor ladder is implemented as the feedback resistor of the inverting amplifier structure to control the overall gain in the range of 12 dB to 20 dB.

Since the signal amplitudes at the outputs of the demodulator are controlled by its internal AGC loop, a PGA board is needed to vary the signal amplitudes before the ADC so that the peak effective number of bits (ENOB) of the converter can be obtained. A simple inverting amplifier stage is utilized to achieve this target, and the schematic is shown in Fig. 3. The gain of the PGA stage is set by the ratio of resistors in the inverting amplifier structure, while the feedback resistor is built as a ladder. An analog switch chip (74HC4316 from Nexperia) is used in each inverting amplifier to change the equivalent resistance of the feedback resistor ladder, allowing the overall gain of the PGA to be varied from 12 dB to 20 dB.

C. Phase Mismatch Compensation

Ideally, the baseband signals at the outputs of the PGA stage can be directly sent to the ADC inputs. However, there is phase mismatch between all the channels, which may arise from mismatched cables, discrete components, PCB traces, etc. such mismatch should be minimized before sending the signals to the ADC, otherwise it is able to generate energy at high spatial frequencies and therefore ruin the signal-to-noise ratio (SNR) of the system.

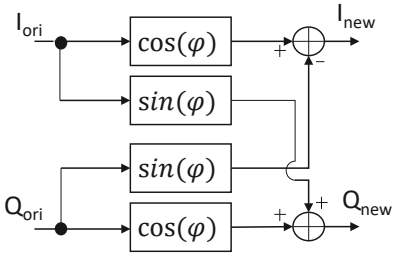

Fig. 4. Phase mismatch compensation method.

If we assume that the demodulator chip behaves as expected, i.e., the amplitudes of real and imaginary parts are the same and the phase difference between real and imaginary parts is

90°, then we have the complex signal at the PGA output as $e^{j(\omega t+\phi_0)}$, where ω is the signal frequency and ϕ_0 is the signal phase. However, due to the mismatch mentioned above, all the channels have the same frequency but different phases. Such phase mismatch can be removed by shifting each channel by a different compensation phase ϕ_c, resulting in

$$\begin{aligned} & e^{j(\omega t+\varphi_0)} \times e^{j(\phi_c)} \\ & = \cos(\omega t+\phi_0)\cos(\phi_c) - \sin(\omega t+\phi_0)\sin(\phi_c) \\ & + j\left[\sin(\omega t+\phi_0)\cos(\phi_c) + \cos(\omega t+\phi_0)\sin(\phi_c)\right]. \end{aligned} \quad (1)$$

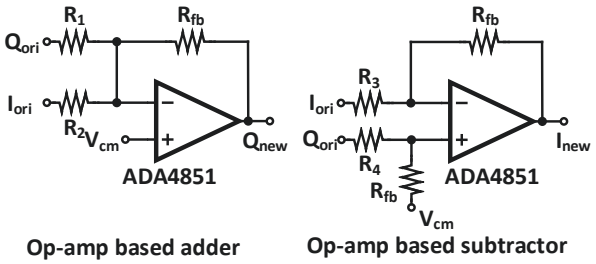

Fig. 5. Schematic of the phase compensation stage when the compensation phase ϕ_c is in the range of 0° to 90°.

From eqn. (1), the compensated I/Q signals can be easily obtained by multiplying the original I/Q signals with some constants which are dependent on the needed compensation phase. The block diagram of the compensation method is shown in Fig. 4. In order to implement this method, another phase compensation board must be added to the system. To perform the sum and subtraction operations in the compensation method, an operational amplifier (op-amp) based adder and subtractor are needed for each I/Q signal. Fig. 5 shows the circuit used for phase compensation when the needed compensation phase ϕ_c is in the range of 0° to 90°. In addition, since the compensation factors $\sin(\phi_c)$ and $\cos(\phi_c)$ can be positive or negative based on the needed ϕ_c, it is necessary to add an additional unity-gain inverting amplifier to shift the signal if a larger compensation phase is required. For example, if the compensation phase ϕ_c is in the range of 90° to 180°, an adder is needed to compensate the real part, while both a subtractor and an unity-gain inverting amplifier are needed to compensate the imaginary part. The compensated outputs are then fed into the ADC.

The block diagram of the complete array receiver system is shown in Fig.6(a), including an array receiver board to receive the RF signal and downconvert it to baseband, a PGA board to vary the signal amplitudes, and a phase compensation board to minimize the phase mismatch between all the channels. This system can be then used to drive the 2-D Δ-Σ noise-shaping ADC for digitization. A photograph of the complete array receiver is shown in Fig. 6(b).

III. Experimental Results

The proposed array receiver board was tested with a RF signal generator and broadband (2-18 GHz) horn antenna

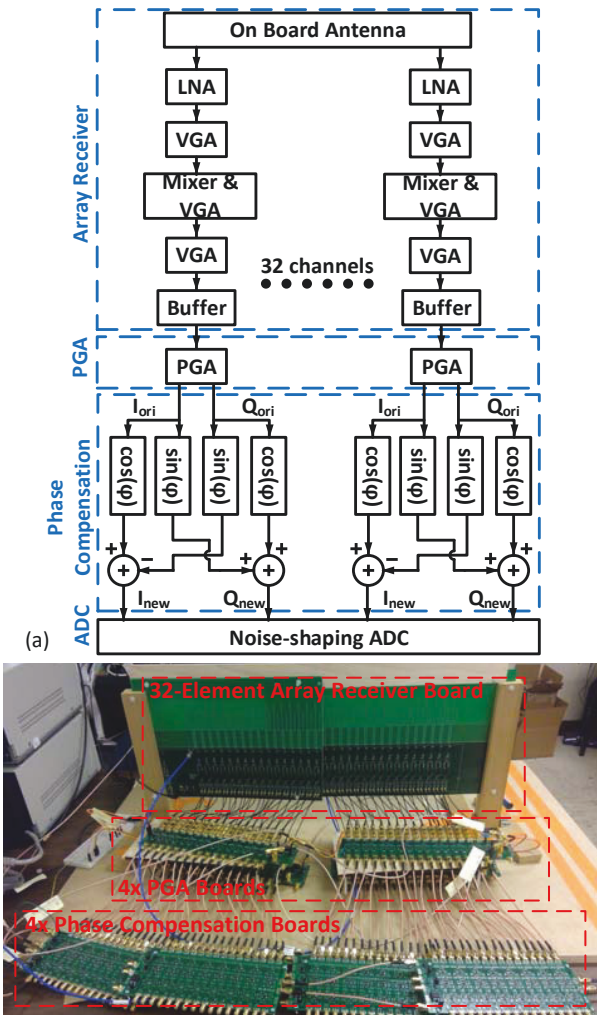

Fig. 6. (a) The complete system block diagram. Four sets of PCBs are included in the system. (b) Photograph of the proposed array receiver system.

(LB-20180 from A-INFO). In order to sweep the signal arrival angle, the horn antenna is mounted on a rotation stage (8MR190-2-28 from Standa Ltd.) with a rotation range of 360° and a resolution of 0.01°. A stepper and DC motor controller (8SMC5-USB from Standa Ltd.) is used to control the rotation stage by using a custom XILab interface through USB connection. The horn antenna was placed far enough ($\sim$ 1.8 m) from the array to ensure far-field operation. RF absorbers were used during testing to reduce unwanted reflections from the floor. The received RF signals were amplified and downconverted to baseband by the array receiver and then sampled by an oscilloscope with fast enough sampling rate. A photograph of the measurement setup is shown in Fig. 7.

As mentioned above, the outputs from different channels have significant amplitude and phase mismatches. In order to calibrate out these errors, the array was fed with a uniform plane wave (0° incidence angle), which in theory should result in identical outputs from all the channels. Fig. 8 shows the measured analog baseband complex signals at

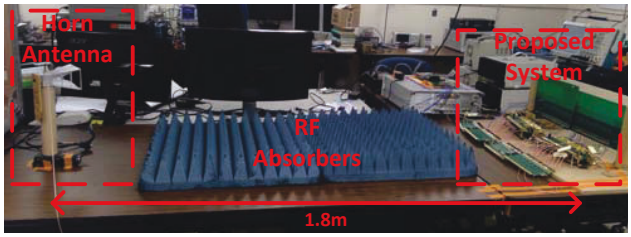

Fig. 7. Photograph of the measurement setup.

the outputs of the PGA board without any calibration. It is interesting to see that the gain mismatch is 58%, which is calculated as $(V_{max} - V_{min})/V_{ave}$, where V_{max} and V_{min} are the maximum and minimum values among all the channels, respectively, while V_{ave} is the average of all the channels. In addition, the measured output phase mismatch has a standard derivation of 35°.

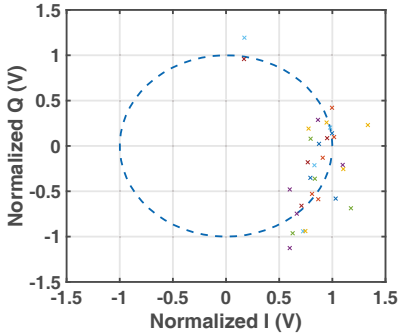

Fig. 8. Measured 32-channel I/Q outputs for plane waves incident at 0° without any calibration. Amplitude and phase mismatches exist between all the baseband outputs.

The gain error calibration and the phase mismatch compensation are then achieved by adjusting the voltage gains of the baseband buffers and the gains of the phase compensation stage. Experimentally, calibration was found to reduce the amplitude mismatch by a factor of ∼1.8 (33% gain mismatch after calibration) and the phase mismatch by a factor of ∼2.9 (standard derivation of 12° after compensation). The calibrated experimental results are shown in Fig.9 with waves incident at 0°. The complex outputs are clearly closer to each other compared to the uncompensated results shown in Fig. 8. The residual error is limited by the random measurement error as well as the tolerance of the discrete resistors which set the gains of the buffers and phase compensation stage.

IV. Conclusion

In summary, a spatially-oversampled 32-element array receiver for spatio-temporal Δ-Σ noise-shaping is proposed. The initial outputs have significant amplitude and phase mismatch, and calibration is achieved by adjusting the gains of the baseband buffers and utilizing the proposed phase compensation method to minimize the errors. The experimental results discussed in this paper prove the functionality of the proposed 32-element array receiver system. In the future, this array receiver will be further utilized to drive Δ-Σ ADCs, thus validating the proposed 2-D space-time noise-shaping algorithm. The PGA board will be utilized to adjust the signal amplitudes to the full-scale range of the ADC, thus improving the system SNR and the ENOB of the converter.

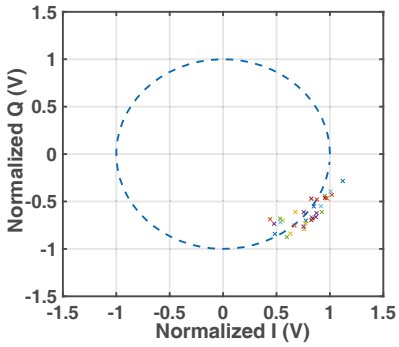

Fig. 9. Measured 32-channel I/Q outputs for plane waves incident at 0° after calibration. Gain and phase mismatches are reduced.

Acknowledgment

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