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Effects of Long-Time Current Annealing to the Hysteresis in CVD Graphene on SiO_2

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ABSTRACT

Graphene specimens produced by chemical vapor deposition usually show p-type characteristics and significant hysteresis in ambient conditions. Among many methods, current annealing appears to be a better way of cleaning the sample due to the possibility of in-situ annealing in the measurement setup. However, long-time current annealing could increase defects in the underlying substrate. Studying the hysteresis with different anneal currents in a graphene device is, therefore, a topic of interest. In this experimental work, we investigate electron/hole transport in a graphene sample in the form of a Hall bar device with a back gate, where the graphene was prepared using chemical vapor deposition on copper foils. We study the hysteresis before and after current annealing the sample by cooling down to a temperature of 35 K from room temperature with a back-gate bias in a closed cycle refrigerator.

INTRODUCTION

Graphene is one of the most popular 2D materials [1-7]. It is semimetallic and, has charge carriers that behave like Dirac fermions (zero effective mass) [1]. Graphene also shows high mobilities up to 200,000 $cm^2V^{-1}s^{-1}$ [2], and many other extraordinary effects. Half-integer quantum Hall effect [4] and ballistic transport properties at room temperature [3] are a few examples. Production of high-frequency electronic devices [5] and transparent low resistance conductors [7] will be feasible due to high carrier mobility and lower visible light absorption of graphene.

Obtaining disorder free graphene is essential and investigating the obstacles for doing that is crucial for the future of nanotechnology. The highest quality graphene with minimum structural defects is achieved by mechanical exfoliation of pyrolytic graphite [8]. However, the exfoliation method cannot be utilized in creating large-area monolayer graphene. Therefore, a method that can fabricate uniform monolayer graphene in large scale is required. Chemical Vapor Deposition (CVD) of graphene was demonstrated as a

method of growing single-layer graphene [9]. It has been shown that large area of single-crystal, monolayer graphene (0.5 mm on a side) can be grown with good control, on copper foils [10-11].

The problem with CVD graphene is the process-induced impurities and defects. Such defects would make our samples inhomogeneous, causing the transport properties to deviate from what we expect theoretically for ideal graphene. Since graphene is zero bandgap semi-conductor, conversion of dominant carrier type can be induced using a gate bias. The conversion from holes to electrons happens without crossing a bandgap [12]. Having the Fermi level at the Dirac point would mean there is no net carrier density. Therefore, one can expect diverging Hall resistance and diagonal resistivity. However, experimental observations suggest that holes and electrons undergo ambipolar transport over a wide range of gate voltage near the Charge Neutrality Point (CNP) of CVD monolayer graphene. This observation was explained by the formation of electron-hole streams [13] or puddles [14] at the Dirac point, that arise due to impurities or graphene ripples [15].

Possible impurities involved with CVD graphene

Graphene transferred on to silicon dioxide substrates are found to be p-type in most cases due to doping by unintentional adsorbates [16]. Clean mono-layer graphene is considered hydrophilic [17]. Graphene placed on a defective substrate (i.e., SiO_2), is more likely to be affected by water and that the underlying substrate can influence the transport properties of graphene significantly [18]. At ambient conditions, molecules like water and oxygen can easily interact with the underlying substrate since the graphene is only a single atomic layer. Once the sample is exposed to ambient conditions, the doping state remains unchanged even in a vacuum.

The traditional wet transfer method used to transfer graphene grown on copper to the substrate can leave metal ions such as Cu^{2+} and Fe^{3+} trapped between the graphene layer and the substrate. The copper layer is typically etched by oxidant solutions such as iron (III) nitrate [19] iron (III) chloride [20] and then cleaned by distilled water. Even after cleaning several times, there can be Fe^{3+} ions that could contaminate the graphene [21].

Effect of impurities to the carrier transport

Impurities influence the transport properties of graphene through several mechanisms. Silicon dioxide (SiO_2) forms silanol bonds (Si-OH) on its surface at ambient conditions. Oxygen and water molecules that are close to the graphene SiO_2 interface will undergo a chemical redox reaction by trapping and de-trapping electrons [22]. If there is an applied electric field (Gate bias), electron trapping, or de-trapping can be stimulated based on the polarity of the field.

Adsorbed water molecules will act as dipoles that oriented randomly. In an applied electric field, these dipoles will align themselves along the electric field direction, which will create a capacitive gating effect locally [16].

Ions that are trapped in the interface can drift through the SiO_2 at higher temperatures [23]. The movement of these ions will vary the distance to the graphene layer leading to a change in the localized gating effect. Figure 1(a) demonstrates that the gating effect occurs due to water dipole and charged impurities. The combination of localized gating and charge trapping de-trapping effects emerge as the hysteresis in CVD graphene samples. Figure 1 (b) explains the hysteresis using the drift of a positively charged impurity through SiO_2 in an applied electric field. Here, we consider the voltage that we observe at the charge neutrality point while forward and backward sweeping the gate voltage (GV). The impurity is at a different location while backward sweeping than it was in forward

sweeping the GV. Therefore, the influence of impurity is different. A typical hysteresis loop for a p-type graphene sample is shown in Figure 1(c).

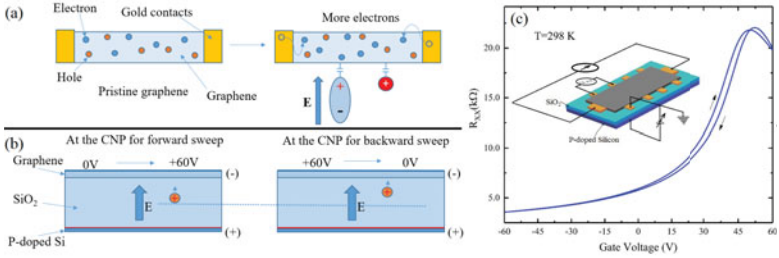

Figure1. Gate hysteresis effect in CVD graphene on SiO_2 substrate. (a) Electrostatic gating effect caused by water and charged impurities in an applied electric field. (b) Hysteresis caused by impurity migration through the SiO_2 substrate due to an applied electric field. The figure demonstrates an instance where the gate voltage is at the charge neutrality point for the forward and backward sweep from the left and right figures respectively. Note that the position of the charged impurity is different in two situations. (c) Typical hysteresis loop of a p-type graphene sample at room temperature where the diagonal resistance is measured against the gate voltage in a range of -60V to +60V as a loop. Inset is showing the measurement configuration of the graphene sample.

Here we investigate the influence of long-time current annealing on the hysteresis effect and carrier transport of graphene specimen grown by the standard CVD method. We also demonstrate that the charge neutrality gate voltage can be controlled by cooling the sample with gate bias. Further, we study the effect of current annealing to the controllable range of CNP.

EXPERIMENTAL METHOD

The monolayer graphene was grown on 25 µm copper foils by chemical vapor deposition using a methane and hydrogen mixture as carbon precursor at about 1000° Celsius [9]. The graphene was transferred onto a 500 µm p-doped silicon wafer (100) with 285 nm of oxide layer using conventional wet transfer method [20]. Here we used millimeter-scale Hall bar devices with p-doped silicon as the back gate in the configuration depicted as in the inset of figure 1(c).

A closed-cycle refrigerator was utilized for the experiment. The sample was kept under vacuum for two days prior to the start of measurements using a turbo molecular pump ($10^{-5}\,Torr$). We can assume that most of the water molecules and other adsorbents are removed by pumping. The dominant effect will be from charge trapping (ionic impurities/ substrate trap sites). We studied the temperature and anneal-current dependence of the gate hysteresis effect. Samples were annealed for 10 hours with annealing currents of 100 µA, 1.5 mA, and 2 mA. The sample was held at a fixed -60 V back gate bias in order to create electron deficiency on graphene. We were able to cool the specimen to 35 K within four hours. A sweep rate of 0.2 V/s and a range of ± 60 V was used to sweep the back-gate voltage. To get an idea about the time frame for charge trapping and de-trapping, we carried out several hysteresis loops with different wait time at +60 V. A direct current of 10 µA was supplied to the sample, and the diagonal voltages were measured using digital multimeters.

RESULTS AND DISCUSSION

Initially, we measured the hysteresis loops of our hall bar device at the room temperature. As shown in figure 2(a), the back-gate voltage was cycled from -60 V to +60 V and then back to -60 V without any delay at +60 V for a first gate bias sweep, and then with a delay of 5, 10 and 15 minutes for subsequent sweeps. The results are shown in solid (orange), dotted (green), dashed (blue) and dotted dashed (red) lines respectively. Inset is showing an enlarged portion from the region near the charge neutrality point. The difference between the gate voltage at the CNP for the forward and backward sweeps is an indication of the hysteresis. When the wait time increases, the voltage difference between the CNP for forward and backward sweep also shows an increasing pattern. The voltage difference was 2.1 V for the data collected without any delay at +60 V. Then the difference increased to 3.8 V and 4.5 V after waiting for 5 and 10 minutes at +60 V respectively. It appears that the difference between up-sweep and down-sweep CNP's is not changing much after 10 minutes.

The hysteresis we observed here can be explained by charge trapping and de-trapping at the SiO_2-graphene interface and the top surface of graphene. When we are at a positive gate voltage, the electron concentration on graphene is higher compared to the holes. Trapping centers will trap electrons and reduce the effective electron concentration on graphene. This will reduce the effective gate voltage, moving the CNP to a more positive voltage. Similarly, the effect of a negative gate voltage can be explained as trapping and de-trapping of holes. Trapped charges will remain trapped until the polarity of the gate is switched. Silicon dioxide has silanol groups on the surface that act as charge traps. Thermally grown SiO_2 has effective trap density of about 5×10^{10} cm^{-2} interface traps and about 5×10^{11} cm^{-2} oxide traps [16].

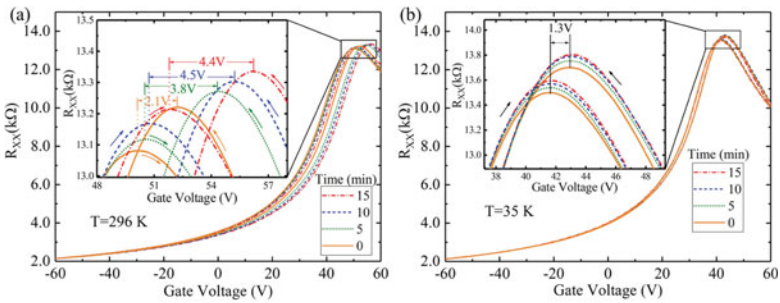

Figure 2. Hysteresis loops with different wait times at +60 V GV at (a) room temperature and (b) 35 K. Diagonal resistance (R_{xx}) vs. the gate voltage for the wait times of 0, 5, 10 and 15 minutes at +60 V is shown in solid (orange), dotted (green), dashed (blue) and dotted dashed (red) lines respectively. Inset is a zoomed-in figure of the plot near the charge neutrality point in all the curves.

We observed a reduction of hysteresis with reduced temperature. Figure 2 (b) shows that the difference between the gate voltage of CNP for the forward and backward sweep at the temperature of 35 K is 1.3 V which is smaller than what we observed at the room temperature. There is no observable difference between the data collected with different wait times at +60 V that may be due to the prolonged time constant of charge trapping and de-trapping mechanism at lower temperatures. However, the observation of 1.3 V difference between the CNP for forward and backward sweeping indicates there is

something that changed the effective gate voltage quickly even at 35 K. Since we did not change the polarity of gate voltage and only change the magnitude until we reach 0 V from +60 V, we cannot reason this observation as an effect of dipolar impurities such as water or ice. The number of electrons or holes trapped by the silanol traps near the graphene SiO_2 interface can be increased or decreased based on the magnitude of the applied electric field [24]. However, we must investigate this further to have a better understanding.

Annealing the graphene sample with a DC supply.

We started current annealing the graphene Hall bar device with 100 μA DC supply. We annealed the sample for 10 hours in order to study the effects of long-time current annealing to the carrier transport. Figure 3 (a) demonstrate the hysteresis loops at room temperature before and after annealing by a solid (blue) and dotted dashed line (red) respectively. If we consider the gate bias we observed the CNP for the forward sweep, it was 44.5 V before annealing and is reduced to 37 V afterward. So, the annealing shifted the CNP toward the zero gate-voltage direction. Which means, the sample became less p-type. However, the difference between the CNP gate voltage for forward and the backward sweep was 2.4 V before, and the value increased to 5.6 V after annealing. This is an indication of a significant increase in the hysteresis.

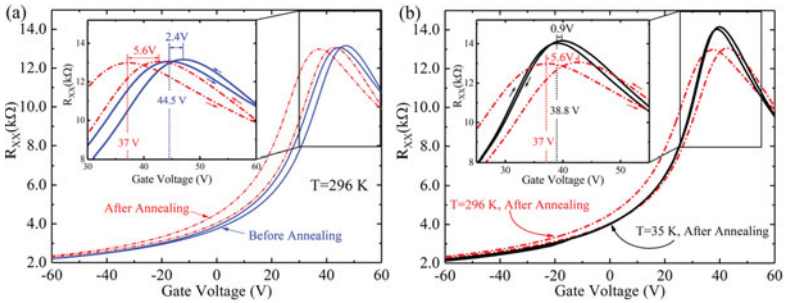

Figure 3. Hysteresis loops after annealing the sample for 10 hours with 100 μA DC supply. Diagonal resistance (R_{xx}) is plotted against the back gate voltage, before annealing the sample in (a) solid (blue) line and after annealing in dashed-dotted line (red) in both (a) & (b) at the room temperature, (b) dotted dashed (red) line represent the data collected at 35 K after the annealing. Inset is a zoomed-in figure of the curves near the charge neutrality point.

Figure 3 (b) shows the diagonal resistance (R_{xx}) plotted against the back-gate voltage after the current annealing at room temperature in the dotted dashed line and 35 K in solid (black) line. CNP voltage for the forward sweep at room temperature was 37 V, and it increased slightly to 38.8 V when cooled. The difference between the CNP voltage for the forward and backward sweep decreased to 0.9 V, which indicates a significant reduction of hysteresis. The increase of the CNP voltage observed at low temperature compared to the room temperature may be due to trapped charges within the surface or bulk charge traps during the sweep performed at the room temperature.

We annealed the sample further using a DC supply of 1.5 mA and 2 mA. The results are shown in figure 4. The diagonal resistance (R_{xx}) is plotted against the back-gate voltage at 35 K. The data collected without annealing the sample is shown in solid (black) line, and after annealing with 100 μA is depicted in dotted-dashed (blue) line. The plots obtained after annealing with 1.5 mA and 2 mA are shown in dotted line (green) and dashed line (red) respectively. The inset shows an enlarged version of the plot near CNP of all the curves.

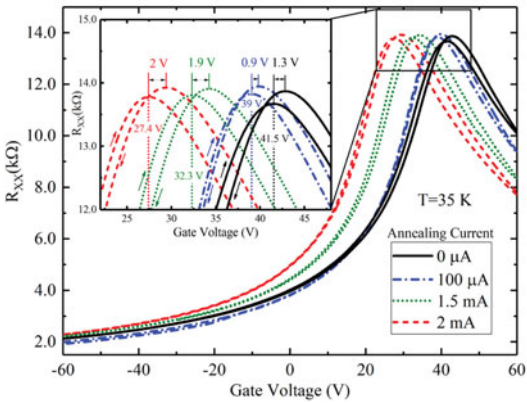

Figure 4. Effect of the current annealing to the charge neutrality point. Diagonal resistance (R_{xx}) vs. the back-gate voltage is shown at 35 K without annealing the sample in solid (black) line, after annealing with 100 μA in dotted -dashed (blue)line, 1.5 mA in dotted line(green) and with 2 mA in dashed line (red).

The CNP voltage observed while sweeping the back-gate voltage to the forward direction before annealing was 41.5 V. The voltage value shifted toward the zero with current annealing. We were able to get the CNP to 39 V with 100 μA anneal current and to 32.3 V and 27.4 V with 1.5 mA and 2 mA DC supply respectively. The difference between the CNP voltage for forward and backward sweep is decreased for 100 μA anneal current and then increased when the anneal current is increased. This observation indicates that the hysteresis increases even though the CNP shifted toward the zero voltage when annealed with a higher current for longer times.

Since the CNP changes in a broad range at room temperature and the change is significantly reduced at cryogenic temperatures, we studied the capability of controlling the charge neutrality voltage with a biased gate voltage supplied during sample cool down from room temperature. We observed that the CNP could be easily shifted toward the higher positive voltage side with a positive bias. With a negative back gate bias, we were able to get the CNP shifted toward lower positive voltage, but not to the negative voltage region where the device becomes n-type. Here we looked at the lower and upper limits of CNP shift we can achieve. We kept the sample for one hour with -60 V bias at room temperature and cooled to 35 K within 4 hours and then did the same thing with +60 V bias. We performed this both before and after current annealing the sample. The results are shown in figure 5.

Before current annealing, we were able to shift the CNP to 55.8 V with a +60 V cooldown back-gate bias and to 41.4 V with a -60 V back gate bias. The difference was 14.4 V between the lower and upper limit of CNP shift. Once we performed current annealing for a long time, this difference increased to 26.1 V. The CNP shifted to 51.2 V with a +60 V cooldown bias. With a -60 V cooldown bias, the CNP shifted to 25.1 V. This observation indicates the annealing we performed somehow increased the range that we can control the CNP.

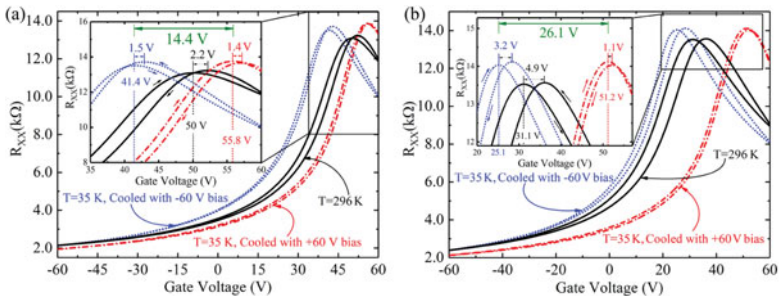

Figure 5. Effect of current annealing on the tunable range of the charge neutrality point by cooling with a back-gate bias. (a) Demonstrates the situation before starting the current annealing, and the data collected afterward are plotted in (b). Both figures (a) and (b) shows the diagonal resistance (R_{xx}) plotted against the back-gate voltage after cooling with a -60 V gate bias in dotted line (blue) and with +60 V bias in dotted-dashed line (red) at 35 K. The solid (black) line corresponds to the data collected at room temperature. Insets provide a closer look at the region that we can observe the charge neutrality point.

CONCLUSION

The hysteretic and electrical properties of back-gated graphene Hall bar devices prepared by standard CVD method were investigated by varying the back-gate voltage at room temperature as well as at cryogenic temperatures. A significant reduction of hysteresis was observed with cooling the device. The hysteresis effect can be explained as a result of the capacitive gating effect that can occur due to localized impurity potentials and the charge trapping and de-trapping mechanism near graphene top and bottom surfaces. The influence of gate sweeping toward impurity potentials got decreased significantly at a lower temperature (35 K).

We found that our samples were always p-type. The CNP shifted toward positive gate voltage with a positive gate bias suggesting that the charge trapping/de-trapping is dominant over the capacitive gating in our samples. The reason is, a capacitive gating will shift the CNP toward the negative gate voltage direction (or toward zero gate voltage from a higher positive value) while sweeping the gate voltage toward the positive direction, which is opposite to what we observed. The charge trapping mechanism agrees with our results. Observation of increased hysteresis after current annealing the sample for a long time may be due to the formation of charge traps in the substrate. Passing a higher current through the sample for a long time yield high temperature on the sample, which anneals the graphene and might create oxygen deficiency on SiO_2, which acts as charge trapping centers [25]. Our observation of increasing the controllable range of CNP with respect to the applied back gate bias after current annealing also suggests a modification in the dielectric layer. However, further studies are necessary to understand the mechanism behind our observations. We are continuing this work further by studying the surface topography as well as carrier mobility and density at different stages of the current annealing process, which would provide us much clear picture.

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