TITLE:
Capping Layers to Improve the Electrical Stress Stability of $MoS_2$ Transistors

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ABSTRACT:

Two-dimensional (2D) materials offer exciting possibilities for numerous applications, including next-generation sensors and field-effect transistors (FETs). With their atomically thin form factor, it is evident that molecular activity at the interfaces of 2D materials can shape their electronic properties. Although much attention has focused on engineering the contact and dielectric interfaces in 2D material-based transistors to boost their drive current, less is understood about how to tune these interfaces to improve the long-term stability of devices. In this work, we evaluated molybdenum disulfide ($MoS_2$) transistors under continuous electrical stress for periods lasting up to several days. During stress in ambient air, we observed temporary threshold voltage shifts that increased at higher gate voltages or longer stress durations, correlating to changes in interface trap states ($\Delta N_{it}$) of up to $10^{12}$ $cm^{-2}$. By modifying the device to include either SU-8 or $Al_2O_3$ as an additional dielectric capping layer on top of the $MoS_2$ channel, we were able to effectively reduce or even eliminate this unstable behavior. However, we found this encapsulating material must be selected carefully, as certain choices actually amplified instability or compromised device yield – as was the case for $Al_2O_3$, which reduced yield by 20% versus all other capping layers. Further refining these strategies to preserve stability in 2D devices will be crucial for their continued integration into future technologies.

TEXT:

## SECTION: Introduction

Transition metal dichalcogenides (TMDs) are a class of atomically thin two-dimensional (2D) nanomaterials with many promising applications in electronics.[1,2] In particular, molybdenum disulfide ($MoS_2$) is a naturally abundant TMD with a large bandgap, making it a prime candidate for the channel material in future low-power field-effect transistors (FETs).[3–6] Scaled $MoS_2$ FETs commonly demonstrate impressive on-off current ratios and subthreshold swing, but obtaining consistently high drive current remains challenging.[7–9] One key issue is the highly variable room-temperature field-effect mobility commonly observed in scaled $MoS_2$ FETs.[10,11] While some variation could arise from imperfections in mobility extraction techniques, it is possible that much of this variation is due to disorder or charged impurities around the $MoS_2$ channel. Many methods have been investigated to reduce disorder, such as modification of the substrate chemistry underneath the channel,[12–14] full encapsulation of the channel with a high-k dielectric or 2D insulator such as hexagonal boron nitride,[15–18] and repair of sulfur vacancy defects in the $MoS_2$ lattice.[19,20] Recent $MoS_2$ FETs built on corrugated substrates even exceeded many projected mobility limits at room temperature,[21] indicating that the dielectric interfaces to $MoS_2$ can be engineered to resolve and even reverse the mobility degradation issue. Further improvements at the dielectric interface will be crucial to the continued development of scaled $MoS_2$ transistors.

In addition to scaled transistors, larger form-factor $MoS_2$ FETs have been explored for their application in photovoltaic cells,[22,23] non-volatile memories,[24,25] and gas sensors.[26–28] Although resolving mobility variability is important for devices used in these applications, it is also critical for these devices to function without significant degradation over long operating

lifetimes. Therefore, it is important for the structure of these devices to be designed with stability in mind. Many $MoS_2$ FETs studied use a simple back-gated design so that the surface of the $MoS_2$ channel is exposed. It has been shown previously that these devices are susceptible to the adsorption of oxygen and water molecules,[29,30] which contribute to interface trap density[31] and cause increased hysteresis.[32–35] When these devices are biased at a particular gate voltage for extended periods of time, the gradual accumulation or depletion of charge in these interface trap states causes the device threshold voltage ($V_T$) to temporarily shift.[36,37] These transient effects are highly undesirable, and to mitigate them it is necessary to identify effective strategies for preventing molecular adsorption onto the surface of $MoS_2$.

One strategy for mitigating the impact of ambient exposure is the encapsulation of the $MoS_2$ with additional layers of protection on top of the channel. Although there have been many studies to date investigating a wide variety of capping layers on $MoS_2$ FETs, their effectiveness at preventing molecular adsorption has received comparatively little attention as most have focused on how modification of the $MoS_2$-dielectric interface can boost field-effect mobility.[10,13,15–17] Studies of polymer capping layers to protect $MoS_2$ FETs from the ambient have focused on fluorinated CYTOP[38] and p(V4D4-co-CHMA) copolymers,[39] although neither one appeared to completely stabilize the threshold voltage under extended periods of bias stress. One group has also studied the effects of bias stress on $MoS_2$ FETs encapsulated by hexagonal boron nitride (h-BN)[40] and ALD-grown alumina ($Al_2O_3$).[41] Both of these approaches significantly suppressed hysteresis in the devices, although both still allowed $V_T$ shifts under certain conditions. Finally, a more recent study incorporated a 3-nm-thick $TiO_2$ interfacial encapsulation layer in order to study electrical stress and the role of Fermi-level pinning at the contacts.[42] However, note that none of these reports have systematically examined more than one

capping material for the comparative impact of electrical stress on device stability. Unfortunately, due to variations in device fabrication and characterization methodologies across the various studies, it is challenging to compare the results and identify the definitive strengths and weaknesses of diverse passivation approaches. A study of multiple passivation materials using consistent characterization techniques would reveal which passivation material properties impact the physical mechanisms that drive molecular adsorption and would guide efforts across applications with different material integration requirements.

Here, we investigated the effects of gate- and drain-bias stress on $MoS_2$ field-effect transistors capped with a variety of passivation layers, including a study of the impact of the electrical stress on device operation under ambient air conditions. We further explored the sensitivity of the devices to variations in stress time and voltage. After baseline device characterization, $MoS_2$ channels were covered with a variety of capping layers, including poly(methyl methacrylate) (PMMA), SU-8 photoresist, silicon nitride ($SiN_x$), and aluminum oxide ($Al_2O_3$). The hydrophilic PMMA layer proved to be ineffective passivation, while the much thicker and hydrophobic SU-8 film provided notable improvements, particularly in short-term stress tests. Devices capped with $SiN_x$ were surprisingly unstable, likely due to defects introduced during film deposition. Only the $Al_2O_3$-passivated devices demonstrated full stability, with no discernable threshold voltage shift after days of continuous bias; yet, the atomic layer deposition (ALD) process for the $Al_2O_3$ also resulted in the lowest device yield compared to the other passivation layers. These results shed light on the role of interface control and passivation material selection in the electrical stability and yield of $MoS_2$-based devices, highlighting some key trade-offs.

## SECTION: Results & Discussion

The $MoS_2$ FETs were fabricated using conventional lithography and thin-film deposition techniques. $MoS_2$ flakes (whose molecular diagram is shown in Fig. 1A) were mechanically exfoliated from a bulk crystal (2D Semiconductors Inc.) onto highly doped p++ silicon wafers with a 25-nm-thick thermal oxide. Thin multilayer $MoS_2$ flakes (approximately 4-8 nm thick – see Fig. S1 in the supporting information) were identified by an optical contrast technique developed previously,[43,44] after which metal contacts were defined by electron-beam lithography, electron-beam evaporation, and metal lift-off. A schematic of the finished device is shown in Fig. 1B, with optical and SEM images of typical devices shown in Fig. 1C-D. Electrical characterization (Fig. 1E) was performed using Keysight B2900A source measure units under ambient conditions unless otherwise specified. To facilitate extensive long-term testing, many completed chips were wire-bonded to ceramic packages (Fig. 1F) that fit the sockets on custom measurement systems, as previously described.[45] A full description of fabrication and characterization procedures is available in the supporting information, along with a detailed extraction of performance metrics for all devices studied (see Table S1, Fig. S2-S8). Of particular note in Table S1 are the "initial device yield" percentages recorded for every chip, showing that yield improved from ~30% up to ~81% by several simple fabrication improvements including: using sufficiently wide metal lines for signal routing, avoiding very thick $MoS_2$ flake deposits, and limiting electrical connection between devices so that individual failures are isolated. The total yield of $MoS_2$ devices in this study finished at 49% (100 out of 204 devices).

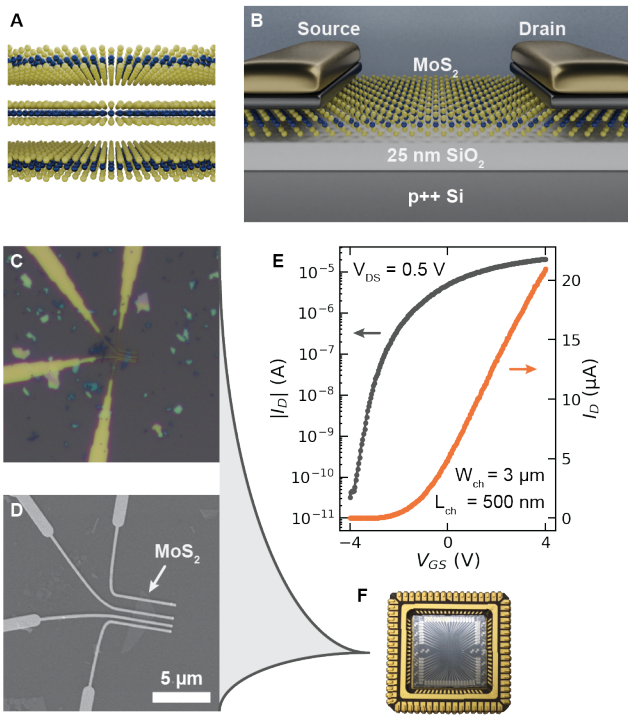


**Figure 1.** $MoS_2$ FET device structure and wire-bonding for long-term characterization. (**A**) Molecular diagram of the van der Waals-layered structure of $MoS_2$. (**B**) Device schematic of a back-gated $MoS_2$ FET with 10 nm Ni (topped with 20 nm Pd) source/drain contacts. (**C**) Optical microscope and (**D**) SEM image of a set of three devices with different channel lengths. (**E**) Typical transfer and subthreshold characteristics of a device measured in ambient conditions. (**F**) Chip installed and wire-bonded into chip carrier for testing at the end of fabrication.

Prior to studying the influence of different capping layers on $MoS_2$ FET stability and performance, baseline back-gated devices were fully characterized. Due to previous reports[36,37] of the threshold voltage instability of $MoS_2$ transistors under bias stress, focus was given to this behavior in our devices. Fig. 2A shows the results of an experiment in which a $MoS_2$ FET was held in the on-state with a drain voltage of $V_{DS}$ = 0.5 V and a gate voltage of $V_{GS}$ = 3 V for four consecutive time segments of length $t_{Hold}$ = 2 hr. Between bias-stress segments, the gate voltage was swept in order to extract the device characteristics shown in Fig. 2B. From the initial device behavior, there is a positive threshold voltage shift ($\Delta V_T$) in each of the other four measurements of the transfer characteristics. This simple experiment yields several important insights into the back-gated, non-passivated $MoS_2$ FET operating in ambient air: (1) even though we applied

constant drain and gate voltages, the drain current was not constant over time, changing by up to 45% from its initial value; (2) the drain current was changing because the threshold voltage of the device was changing; (3) the act of sweeping the gate voltage partially reset the threshold voltage shift in the device, but in the subsequent period of $t_{Hold}$ the threshold voltage returned to the same terminal value; and (4) this process is repeatable, indicating that most of these effects are transient rather than permanent changes to the device. This unstable behavior was extremely consistent across many devices on different chips and wafers, including those with significantly different oxide thicknesses (see Fig. S9-S11 for identical behavior in multilayer and monolayer devices on 90 nm $SiO_2$ substrates).

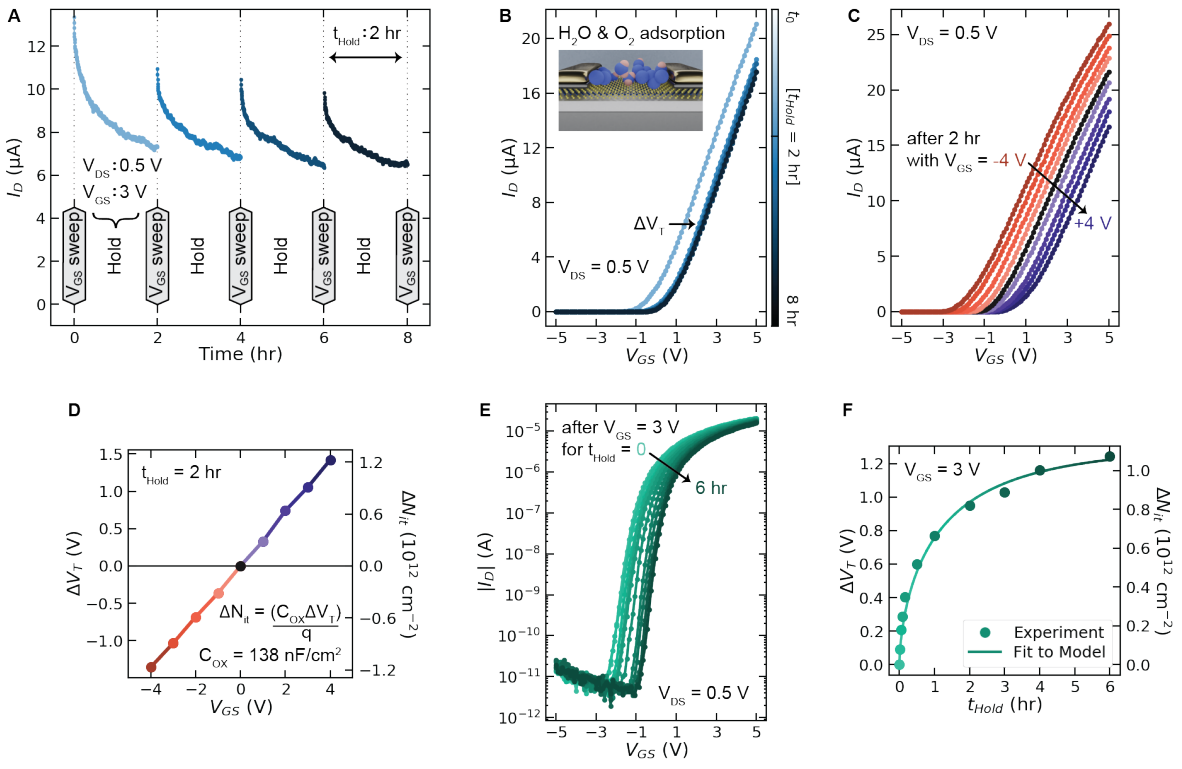


**Figure 2.** Susceptibility of non-passivated $MoS_2$ FETs to molecular adsorption from ambient air conditions. (**A**) Long-term biasing of a $MoS_2$ FET in ambient air at $V_{DS}$ = 0.5 V and $V_{GS}$ = 3 V with periodic interruptions every 2 hours to measure transfer characteristics ($V_{GS}$ sweep). (**B**) Transfer curves measured throughout the experiment in (A), showing a positive threshold voltage shift as a result of the accumulation of adsorbed species on the surface of the $MoS_2$

channel. (**C**) Transfer curves measured after 2 hours of biasing at a static gate voltage; tested for $V_{GS}$ = -4 V to +4 V in increments of 1 V. (**D**) Magnitude of threshold voltage shifts extracted from (C), showing equal and opposite shifts for positive and negative $V_{GS}$ bias voltages, where the dual axis shows the corresponding estimated change in interface trap occupancy. (**E**) Transfer curves measured after biasing at a static gate voltage of $V_{GS}$ = 3 V for hold times ranging up to $t_{Hold}$ = 6 hr. (**F**) Magnitude of threshold voltage shifts and change in interface trap occupancy extracted from (E), showing their fit to a stretched exponential bias-stress model. $L_{ch}$ = 500 nm and $W_{ch}$ = 3 µm for this device.

Repeating the experiment shown in Fig. 2A under low vacuum or in dry nitrogen conditions (see Fig. S12) yielded a significant improvement in threshold voltage stability, consistent with previous reports.[37] This indicates that the dominant factor driving this behavior is the adsorption and desorption of oxygen and water molecules from the ambient air onto the surface of the $MoS_2$ channel. The impact of applying different polarity and magnitude of gate voltage to the device is seen in Fig. 2C, with the magnitudes of $\Delta V_T$ resulting from each bias stress $V_{GS}$ shown in Fig. 2D. There is a clear linear dependence of $\Delta V_T$ on the stress gate voltage that is symmetric for positive and negative gate voltages. This symmetry demonstrates that traps can just as easily be filled or emptied by applying a positive or negative gate voltage; however, interestingly the subthreshold swing is not symmetric, improving under negative stress and slightly degrading under positive stress (see Fig. S13). Since SS degradation is associated with increased trap states, this suggests that positive stress is filling electron traps while negative stress is emptying those traps. The symmetry in $\Delta V_T$ is consistent with other reports of the non-passivated $MoS_2$ FET,[37] but note that this behavior is not always symmetrical – as seen in CYTOP-passivated $MoS_2$ FETs which show larger $\Delta V_T$ under negative gate voltage stress.[38]

Although the observed $\Delta V_T$ is indicative of the behavior of trapped charges in these devices, $V_T$ itself can vary widely across the device structures reported in different studies, so it is preferable to use a different metric, such as change in interface trap occupancy ($\Delta N_{it}$), that

does not depend on the gate oxide thickness. By assuming a parallel plate capacitor model[15] for the oxide capacitance of the 2D FET structure, we are able to directly convert $\Delta V_T$ to the change in surface charge on the $MoS_2$ flake. A change in the surface charge during bias stress indicates that there has been a change in the density of electrons or holes occupying trap states ($N_{it}$) at the gate oxide interface. Therefore we are able to use the inset equation in Fig. 2D to compute an approximated change in $N_{it}$ that corresponds to the observed $\Delta V_T$, which is shown on the secondary axis of Fig. 2D. The usefulness of $\Delta N_{it}$ as a figure of merit is highlighted more in the supporting information, which shows a device fabricated on a different substrate (90 nm $SiO_2$) experiencing the same stress as Fig. 2C-D and exhibiting an almost identical relationship between gate bias and $\Delta N_{it}$ (see Fig. S10). As a final note, for a sheet of charge with density $10^{12}$ $cm^{-2}$, the nearest-neighbor spacing was calculated to be approximately 10 nm, which was found to be a helpful metric for visualizing $N_{it}$ (see Fig. S14).

The final aspect of the baseline $MoS_2$ FETs that was investigated is the impact of stress time at a constant gate stress voltage, as shown in Fig. 2E-F. Here we see that $V_T$ evolves over time according to the same stretched-exponential model that has been widely used to model bias stress in $MoS_2$ transistors[39,46] as well as thin-film transistors based on zinc oxides[47,48] or organic semiconductors:[49,50]

$$\Delta V_T(t) = V_0\left(1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right)$$

where $V_0$ is the value of $\Delta V_T$ as $t \to \infty$ and $\tau$ is known as the relaxation time. The solid line in Fig. 2F shows a fit to the experimental data with $\beta$ of 0.65 and a relaxation time of 4500 seconds (1.25 hr). Hence, the time scale over which these FETs should be analyzed for electrical stress behavior should be on the order of 1-2 hours.

To briefly summarize, the baseline, back-gated $MoS_2$ FETs experienced a threshold voltage shift under gate bias stress largely driven by $O_2$ and $H_2O$ molecules in the ambient air environment. This threshold voltage instability exhibited a linear dependence on the stress voltage and a stretched-exponential dependence on stress time, with the majority of the change occurring within the first two hours of stress, but with several hundred millivolts of shift happening within the first few minutes. For many applications of $MoS_2$ FETs, this bias-induced drifting behavior of the threshold voltage would be unacceptable.

To passivate $MoS_2$ transistors in an effort to eliminate these deleterious effects of bias stress, we explored the incorporation of four distinct protective barrier layers to cover the exposed $MoS_2$ channel. Fig. 3A illustrates the modified device schematic with the introduction of a passivation layer, and Fig. 3B shows several of the actual chips with the central device area covered with a passivation layer. The results of the bias stress test at a fixed $V_{GS}$ = 3 V (as presented for the baseline, non-passivated device in Fig. 2A-B) reveal that some of the passivation layers actually exacerbate the threshold voltage shifts while others ameliorate them (Fig. 3C-D). To improve statistical rigor, the experiments shown in Fig. 3C-D were repeated on three separate devices on each chip, with the final results (mean and standard deviation) summarized in Fig. 3E.

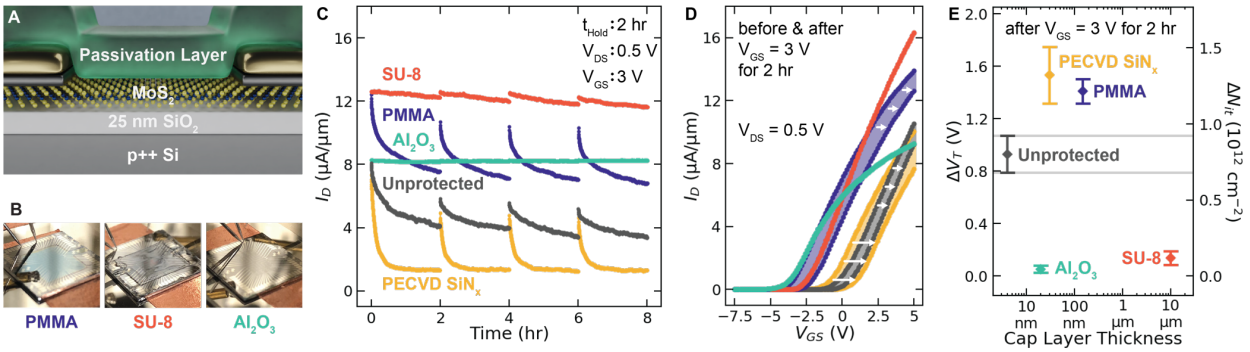

**Figure 3.** Accumulation of trapped charge with different passivation layers capping back-gated $MoS_2$ FETs when stressed for two-hour intervals. (**A**) Modified device schematic with passivation layer. (**B**) Photographs of chips coated in variety of passivation layers. (**C**) Long-term biasing of $MoS_2$ FETs with different passivation layers, performed in ambient conditions with periodic interruptions every two hours to measure transfer characteristics. (**D**) Transfer curves measured before and after the first two hours of biasing shown in (C). (**E**) Magnitude of threshold voltage shift and corresponding approximate change in interface trap occupancy at the end of two hours of biasing at $V_{DS}$ = 0.5 V and $V_{GS}$ = 3 V. Error bars show the mean and standard deviation of measurements from three different devices on each chip. $L_{ch}$ = 500 nm for all devices shown.

Selection of the four capping layers was made to explore distinct deposition and material differences. PMMA was spin-coated and is commonly used as a passivation coating for research-level devices. SU-8 was also spin-coated, but is significantly thicker than PMMA and known for its effective resistance to permeation, including in liquid environments.[51–53] The $SiN_x$ was deposited by plasma-enhance chemical vapor deposition (PECVD), which introduces potential damage to the $MoS_2$ during deposition but is also a more standard passivation material for solid-state devices. Finally, $Al_2O_3$ was grown via atomic layer deposition (ALD), which is a less aggressive reactive environment (compared to PECVD) and allows for precise and comparatively thin film deposition (20 nm in this case). This variety of passivation films allows for insight into which offers most effective protection of $MoS_2$ from ambient effects while preserving the intrinsic $MoS_2$ electrical properties.

One first point of interest in Fig. 3C-D are the relative device current levels at $V_{GS}$ = 3 V. In general, the polymer-capped devices (PMMA and SU-8) displayed slightly higher width-normalized on-current due to a combination of their negative threshold voltage and their ability to sustain high transconductance across a wide voltage range. In contrast, the $Al_2O_3$-capped device in Fig. 3D shows a similar threshold voltage but a more substantial roll-off in transconductance in the on-state, leading to an overall lower current at $V_{GS}$ = 3 V. It is also

striking how similar in shape the PMMA-capped response over time is to the baseline unprotected device (Fig. 3C), indicating that the PMMA offers no noticeable improvement in device stability. Although the $SiN_x$-capped device begins at a similar current level to the baseline device, it falls precipitously in a short time and displayed the most severe threshold voltage instability. Lastly, both the $Al_2O_3$-capped and SU-8-capped devices show improvement in stability compared to the baseline, with the $Al_2O_3$ device showing the flattest and most stable response over time (Fig. 3C).

The PMMA-capped devices displayed such a large threshold voltage shift in Fig. 3D at least in part because the introduction of PMMA caused a distinct permanent negative threshold voltage shift in all devices tested (see Fig. S3). As previous reports have indicated, this is due to the fact that devices susceptible to bias stress instability will tend to shift until $V_T = V_{GS}$.[48,49] Therefore, because the PMMA-capped devices had more negative initial $V_T$, and they were experiencing the same $V_{GS} = 3$ V during stress as all the other devices in Fig. 3C-D, they "had farther to go" in a sense and thus experienced a $V_T$ shift that was larger than the baseline unprotected device. Note that if the PMMA had been an effective passivation layer, then we would not have expected to see any threshold voltage shift in Fig. 3D, regardless of how negative $V_T$ was to begin with. Exactly why PMMA was unable to prevent molecular adsorption onto the surface of $MoS_2$ remains unclear, but some researchers have proposed that PMMA films can form pockets of air on the surface of 2D materials[54] – leading to oxidation and degradation of sensitive 2D materials over extended periods of time. This bias-stress performance of PMMA is most comparable to results from p(V4D4-co-CHMA) copolymer,[39] which yielded devices that were only slightly more stable than PMMA and with roughly similar threshold voltage and transconductance. Regardless, it is clear that the PMMA provided inadequate protection.

The $SiN_x$-capped devices also experienced larger $V_T$ shifts under stress, even though their threshold voltages were much closer to the uncapped device (see Fig. S5). However, it is important to note that the $SiN_x$ capping layer was deposited by PECVD, during which the $MoS_2$ was exposed to a 50 W plasma for at least the first few seconds of deposition. We expect that this process damaged the $MoS_2$ crystal structure, and it is possible that having a higher density of surface defects could enhance molecular adsorption during bias stress, as has been previously suggested for oxygen adsorption in particular.[55,56] Enhanced trap filling could account for the higher $V_T$ shifts and the three times steeper drain current settling for $SiN_x$ seen in Fig. 3C (see also Fig. S15). The thickness of 30 nm for our $SiN_x$ encapsulation was chosen based on another report of encapsulated $MoS_2$ FETs,[32] but based on these results and more extensive review[57] it now seems most likely that our PECVD tool is incapable of producing such a thin film without any pinhole defects that allow molecular adsorbents to reach the $MoS_2$ surface.

The results of initial tests in Fig. 3 examining $V_T$ shift after two-hour bias-stress intervals were promising for devices capped by either SU-8 photoresist or ALD-grown $Al_2O_3$. A more rigorous methodology of exploring stress time and voltage was carried out (Fig. 4A-B) to examine further differences between the various passivation materials. From the results of Fig. 4A, it was discovered that devices capped by SU-8 experienced an initial threshold voltage shift in the opposite direction that was masking an underlying, long-term trend in $V_T$ that is similar to the unmodified devices; i.e., the SU-8-capped devices first exhibited an abrupt negative $V_T$ shift over the initial minutes of bias stress, followed by a more gradual positive shift that resulted in a net change after two hours that was actually rather small (hence, the results of Fig. 3C). From Fig. 4B, we further see that SU-8 does not follow the linear trend of $V_T$ shifting under increasingly positive gate-stress bias seen in all other devices, and shows a net positive $V_T$ shift

after two hours of bias at any voltage. Both of these distinctions in bias stress behavior for the SU-8-passivated devices are attributed to the existence of new and different trap states at the $MoS_2$-polymer interface. Because the threshold voltage shift is always net positive after two hours, this means the trap states are filling with net negative charge. This could indicate a different mechanism is taking place, such as the injection of negatively charged hot carriers into the dielectric over the extended duration of bias. Importantly, the behavior observed in Fig. 4A for the SU-8-capped device was reversible as the trend was reproduced on the same device.

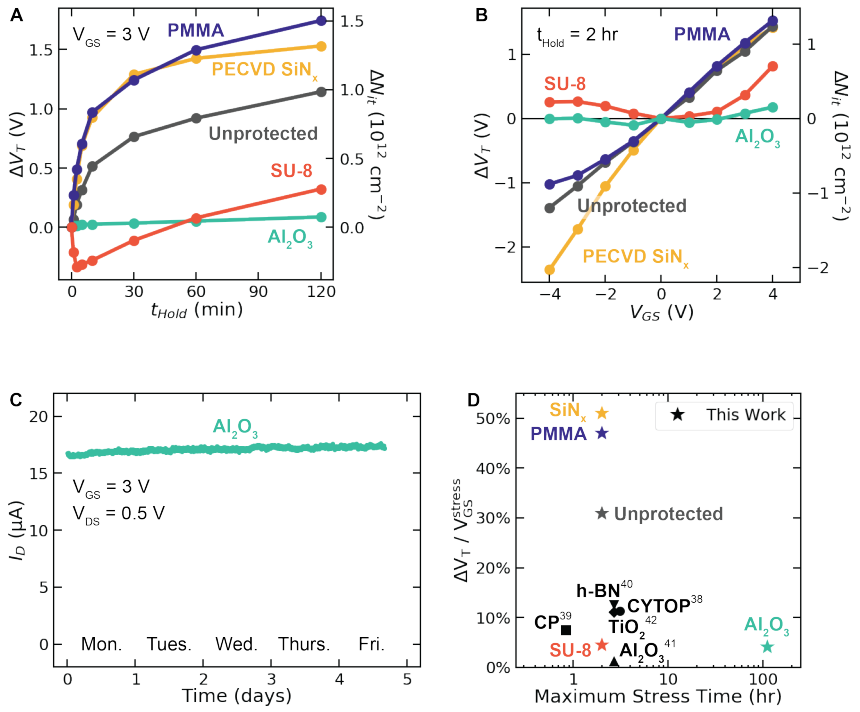


**Figure 4.** Reduction of trapped charge accumulation by the addition of passivation layers to back-gated $MoS_2$ FETs and the impact of bias stress time and voltage. (**A**) Comparison of interface trap accumulation under a variety of passivation layers as a function of bias time and (**B**) as a function of gate bias voltage. (**C**) Long-term biasing of $MoS_2$ FET passivated with $Al_2O_3$ showing stability over several days. Measurements were captured continuously and saved every 10 seconds for the entire duration. (**D**) Benchmarking $V_T$ shift versus maximum stress time against other encapsulation demonstrations for $MoS_2$ FETs. Percent $V_T$ shift was obtained by normalizing absolute $V_T$ shift by the magnitude of $V_{GS}$ applied during stress. Note that exact device structure and stress conditions vary, but all values are taken for positive $V_{GS}$ stress.

Despite the unique threshold voltage shifting behavior exhibited by the SU-8-passivated devices, qualitatively, they performed quite well – certainly far better than the completely unprotected, PMMA-passivated, or $SiN_x$-passivated devices. Additionally, the spin-coating encapsulation process was facile and high yield (~90%), especially compared to the reduced yield observed for devices with ALD $Al_2O_3$ passivation layers (~70%). These yield percentages are listed in Table S1 as the "post-capping yield" and were calculated from the number of functioning devices that survived the encapsulation step; hence, this provides an indication of how "risky" each process is for the devices. Devices were determined to fail to survive encapsulation if (1) their on-current reduced to effectively zero, or – more commonly – (2) their gate current increased to more than 50 nA. Interestingly, while PECVD $SiN_x$ devices did not perform well, that process was actually very high yield as well (90%) – possibly because it was so fast and the devices only spent a couple of minutes in the chamber at elevated temperature (unlike ALD, which takes several hours at 120 ºC). The reason this metric is critical for comparing capping layers is that many applications can become prohibitively expensive if yield is compromised too early in the fabrication processes. Importantly, SU-8 stands alone as the only capping layer that substantially improves device stability while also maintaining high yield. Finally, the SU-8 device instabilities were not obvious in Fig. 3 and only actually uncovered by the rigorous tests shown in Fig. 4, and the overall passivation quality is clearly good enough for there to be several reports of SU-8 encapsulation improving the shelf life of air-sensitive thin-film transistors.[58,59] For these reasons, we are optimistic that SU-8 can still be a good choice for most applications.

Another important takeaway from the gate bias-dependent threshold voltage shift data shown in Fig. 4B is how consistent the response of the PMMA-passivated and $SiN_x$-passivated

devices are with the unprotected device. This is evidence that the trap mechanisms responsible for $V_T$ instability in the unprotected device remain largely unaffected by these capping layers. While we cannot rule out the existence of additional traps introduced within the PMMA or $SiN_x$ capping layers, we might not have expected the curves in Fig. 4B to match so well if that were the case. The reality may be a combination of both internal traps within the PMMA and $SiN_x$ with molecular adsorption still playing a key role through PMMA air pockets or $SiN_x$ pinholes. In contrast, the SU-8 and $Al_2O_3$ both offer appreciable improvements to the $V_T$ shifting behavior under the varying gate stress magnitude and polarity, with the $Al_2O_3$ offering slightly better protection than the spin-coated polymer. This overall consistency in behavior (PMMA consistent with $SiN_x$ and also SU-8 consistent with $Al_2O_3$) seen across capping layers that have otherwise such different physical properties – in addition to the evidence from Fig. S12 for molecular adsorption as a dominant mechanism – inspires confidence that these results should be more broadly applicable to other 2D material systems in addition to $MoS_2$. Notably, alumina passivation on Black Phosphorus (BP) FETs has already been shown to both protect from ambient degradation and to enhance electrical stress stability.[60,61] In addition, tungsten selenide ($WSe_2$) FETs have been shown to be susceptible to p-type doping from oxygen adsorption.[62] Compared to $MoS_2$ however, experimental demonstrations of electrical stress in these FETs are much more sparse, and therefore we believe additional study of the effect of passivation on stress stability is warranted.

Ultimately, the $Al_2O_3$-capped devices exhibited the most encouraging stability under all bias stress conditions, demonstrating negligible changes in $V_T$ even after days of continuous bias stress, as shown in Fig. 4C. However, as previously noted, it is significant that $Al_2O_3$ devices showed the lowest post-capping yield, and so this is worth a closer look. A key problem was that

any devices capped with $Al_2O_3$ experienced a substantial negative threshold voltage shift immediately after deposition of the film, making it often impossible to gate the device fully off (see Fig. S16). This effect is commonly observed in $Al_2O_3$-capped devices,[63] and it indicates that the ALD films contain a significant amount of built-in fixed positive charge (such as unsatisfied $Al^+$ dangling bonds). We found this effect to be most prominent for 40-nm and 30-nm thick $Al_2O_3$ films, which is why the devices reported herein were only coated with 20 nm of $Al_2O_3$. More details can be found in the supporting information, and while these effects could potentially be overcome by further process optimization, at present the hampered yield of $Al_2O_3$-capped devices is a nontrivial cost to its use as a passivation layer. All of this is in contrast to the SU-8-capped devices, which demonstrated close to ideal yield for all devices tested and displayed the next-best electrical stability. Since SU-8 has also further shown compatibility as a passivation layer in biosensors and other liquid environments, it could therefore prove valuable for $MoS_2$ FETs used in this capacity.[51–53]

A benchmarking comparison of the threshold voltage shift versus bias stress time is provided in Fig. 4D. While this comparison looks only at one aspect of the electrical stability, it does reveal that both the SU-8 and $Al_2O_3$ provide stability that is on par with the best previously reported approaches and for longer bias stress durations. The overall performance of the $Al_2O_3$-capped devices is consistent with the one other report[41] of bias stress in an $MoS_2$ FET. It is notable that Illarionov et al. report pushing their devices to a gate stress field of 4.8 MV/cm, while we were limited to 1.6 MV/cm by some of the large metal features required for wire-bonding our devices (these chip features are even visible to the naked eye in Fig. 1F). With metal features of this size, our backside gate oxide was far more susceptible to breakdown if we exceeded a field of 2 MV/cm for hours at a time. While they report higher stress fields, we report

more than an order of magnitude longer stress duration – which is an equally important metric, particularly for applications that do not require high voltage. Since we have seen here that stress intensity and duration both contribute to the device response, it is reassuring that our two different approaches produced similar results.

## SECTION: Conclusion

In conclusion, we have investigated the bias stress stability of $MoS_2$ field-effect transistors in ambient air under a variety of stress time and voltage conditions. In uncapped devices, we observed substantial threshold voltage shifts occurring primarily in the first two hours of stress, with the magnitude and polarity of the shift depending linearly on the gate voltage under stress. These effects correlated to changes in interface charge trap density of up to $10^{12}$ $cm^{-2}$, but were fully reversible and significantly reduced under vacuum or dry nitrogen conditions, leading us to explore several capping layers to protect the devices. Devices capped with PMMA and PECVD $SiN_x$ showed no improvement or even worse electrical stability, while an SU-8 capping layer provided some notable improvement with a facile deposition process and very high device yield. ALD $Al_2O_3$-capped devices demonstrated the best stability, with no observable change in threshold voltage even after 5 days of continuous stress, but also showed low device yield post-passivation. These results demonstrate the importance of developing a rigorous characterization methodology when evaluating the stability of devices under stress to expose the flaws of unstable devices and the appropriateness of certain passivation layers. Not every capping layer is equally effective for protecting the channel of $MoS_2$ transistors, but one can be selected with care to produce devices that operate in ambient air with no sign of instability. This shows promise for the continued development and integration of air-stable 2D transistors into future electronic devices and sensors.

ASSOCIATED CONTENT

**Supporting Information**

Includes detailed description of processes used in the fabrication of the $MoS_2$ FETs, additional electrical characterization of each chip, comparison to multilayer and monolayer devices on 90-nm-$SiO_2$ substrates, and long-term characterization tests in vacuum and dry nitrogen environments (PDF)

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**Author Contributions**

J.L.D. and A.D.F. conceived the study. J.L.D. fabricated the devices, designed the experiments, and performed the device measurements. S.G.N. aided in the experimental design. Z.C. and H.A. contributed to device fabrication processes. A.D.F. supervised the research and provided scientific guidance. All authors contributed to the writing of the manuscript.

**Notes**

The authors declare no competing financial interest.

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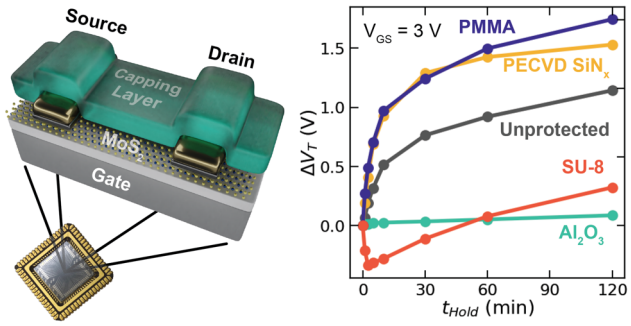
TOC Graphic:




KEYWORDS:
2D materials, molybdenum disulfide, field-effect transistor, electrical stress, threshold voltage, passivation