

Silicon Photonics with MEMS for Efficient Light Manipulation

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Abstract—Silicon photonic MEMS technology offers innovative features of low loss, low crosstalk, low power consumption, and simple digital control. In this talk, we describe the overview of silicon photonic MEMS technology and review the current state of the art of silicon photonic MEMS devices, focusing on large-scale photonic switch application.

Keywords—silicon photonics, MEMS, photonic integrated circuits, optical switching

I. INTRODUCTION

Silicon photonics, optics counterpart of microelectronics, is a technology platform to process, deliver, and detect information using photons (instead of electrons) on an integrated silicon chip [1]. High index contrast of silicon and surrounding cladding (typically air or silicon oxide) enables tight confinement of light in sub-micron scale silicon waveguides and high density integration of a myriad of photonic components. CMOS (complementary metal-oxide-semiconductor)-compatible process of silicon photonics facilitates mass production of high quality silicon photonic devices for commercialization. Owing to these strengths, silicon photonics has emerged as a powerful platform for large-scale photonic integrated circuits (PICs) with a broad range of potential applications such as photonic switches [2], photonic processors [3]–[5], and integrated optical phased arrays (OPAs) [6], [7].

As silicon photonics is being advanced and matured, the complexity of silicon PICs is also rapidly increasing. As a result, the number of photonic components in the present state of the art of large-scale silicon PICs is readily over thousands. For the scaling of silicon photonic devices, there are several essential features required for basic components: 1) low insertion loss; 2) low crosstalk; 3) low power consumption; and 4) easy driving control. Satisfying these requirements, recently suggested silicon photonic MEMS technology, synergistic hybridization of silicon photonics and MEMS technology, offers exceptional PIC scalability superior to traditional thermo-optic (TO) or electro-optic (EO) methods. In this paper, we will describe the overview of silicon photonic MEMS technology and review the state of the art of large-scale silicon photonic switches focusing on its photonic switch application.

II. LIGHT MANIPULATION METHODS IN SILICON

Active silicon photonic components traditionally utilize refractive index change of silicon by thermo-optic or electro-optic methods. Although the change of refractive index is

This work is supported in part by the ARPA-E ENLITENED program (DE-AR0000849), National Science Foundation (NSF) Center for Integrated Access Network (CIAN) (EEC-0812072), NSF PFI-TT Program (1827633), Google Faculty Research Award, Bakar Fellow program, and National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. 2018R1C1B6005302).

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small (a few percent), light modulation or switching can be achieved with Mach-Zehnder interferometers (MZIs) or ring resonators (RRs), on which most of standard silicon photonic circuits are based. However, these structures have non-negligible insert losses, which tend to be quickly accumulated in large-scale PICs. EO modulation method suffers from even higher loss due to free carrier absorption. For MZI structures, imperfect splitting ratio of 3-dB splitter/combiner and unbalanced losses in MZI arms degrade the extinction ratio and the crosstalk. Fabrication variations cause the optimum bias offset for π -phase shift, increasing complexity of driving control for large-scale systems. For RR structures, the extinction ratio and the crosstalk are limited by the critical coupling condition of the resonators. RRs have very narrow optical bandwidth on their resonances. The critical coupling and the resonance wavelength are very sensitive to fabrication variations. Therefore, RRs are most likely employed with resonance tuning circuits which add the driving complexity and also consume additional power.

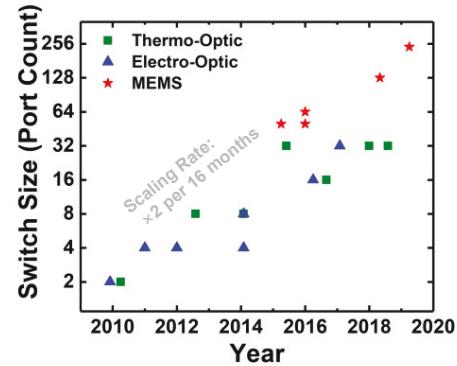


Fig. 1. Switch size (port count) of published silicon photonic switches versus year of publication.

III. SILICON PHOTONIC MEMS TECHNOLOGY

EO or TO approaches use the refractive index change of silicon, whereas silicon photonic MEMS directly modifies optical modes by introducing additional high index material. Depending on the shape and the dimensions of this active structure, it can slightly change the effective index of the original mode, or significantly modify the mode shape or numbers. The former can be used in phase changing applications (i.e. OPAs), and the latter for light switching applications. The strength of silicon photonic MEMS technology is to use the mechanical movement of the active structure. When the active structure is far enough from the original waveguide, it does not cause any optical loss. The crosstalk through the active structure (i.e. coupling waveguide) can be also extremely low. Electrostatic MEMS actuation does not have steady-state current, eliminating power

consumption for holding a state. By utilizing mechanical latching, easy control is possible without the requirement of precise bias optimization or compensation. These innovative features make silicon photonic MEMS technology suitable for large-scale PICs.

IV. LARGE-SCALE SILICON PHOTONIC SWITCHES

Among recent developments of various silicon photonics applications, silicon photonic switches have been leading the large-scale PIC technologies. In the past decade, many research groups have competitively reported high-radix silicon photonic switches. Figure 1 shows the port counts of the published silicon photonic switches versus the year of publication. The scaling trend of doubling switch size every 16 months is observed. In the early stage, EO silicon photonic switches were demonstrated with relatively small switch sizes ($\leq 8 \times 8$) [8]–[10]. As the port count scaled up, TO switches led the scaling trend up to the switch size of 32×32 [11]–[14].

The switches larger than 32×32 have been demonstrated with silicon photonic MEMS technology [2], [15]–[19]. The vertically actuated mechanical movement of the adiabatic couplers enables low loss and low crosstalk (-60 dB). The adiabatic couplers offer broadband operation (> 300 nm in wavelength range) and good tolerance against fabrication variations. Low power consumption and simple digital control without bias optimization also make the silicon photonic switches highly scalable. Leveraging on these scalable features, we have reported the silicon photonic MEMS switches of 64×64 [17], 128×128 [19], and 240×240 [2]. To the best of our knowledge, the 240×240 switch is the largest integrated photonic switch ever reported.

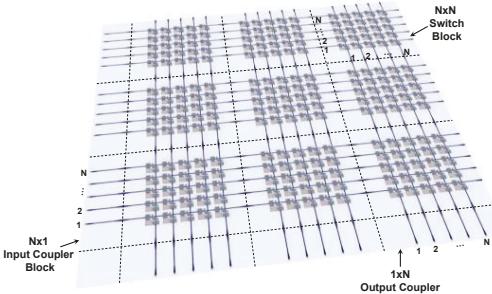


Fig. 2. Schematic of ultra-large silicon photonic switch by die-level stitching of $N \times N$ switch blocks.

As the switch size keeps scaling up, the chip size of a switch device approaches to the die size limit ($2\text{--}3$ cm) of lithography tools. To overcome this limitation, we developed a new method of die-level stitching of $N \times N$ switch blocks as shown in Fig. 2. The 240×240 switch was demonstrated by stitching a 3×3 array of 80×80 switch dies. At the stitched location, the waveguides are tapered to have $10\text{-}\mu\text{m}$ width for reducing the stitching loss to a negligible level (0.004 dB). The on-chip loss per port-count ratio of 0.04 dB/port is the lowest.

V. SUMMARY

We discussed the advantages of silicon photonic MEMS technology for large-scale PICs. Silicon photonic switches based on MEMS technology are more scalable than traditional approaches (EO or TO) thanks to low loss, low crosstalk, low

power consumption, and simple digital control. Recently developed die-level stitching technique allows to overcome the chip size limit of current lithography tools. Following the scaling trend of doubling every 16 months, it is expected that silicon photonic switches with 1000×1000 will be available in a few years.

ACKNOWLEDGMENT

The authors thank Prof. Niels Quack, Dr. Sangyo Han, Dr. Byung-Wook Yoo, Prof. Richard S. Muller, Dr. Kyungmok Kwon, Johannes Henriksson, and Jianheng Luo for their contributions to the work.

REFERENCES

- [1] D. Thomson *et al.*, “Roadmap on silicon photonics,” *J. Opt.*, vol. 18, no. 7, p. 073003, Jun. 2016.
- [2] T. J. Seok, K. Kwon, J. Henriksson, J. Luo, and M. C. Wu, “Wafer-scale silicon photonic switches beyond die size limit,” *Optica, OPTICA*, vol. 6, no. 4, pp. 490–494, Apr. 2019.
- [3] Y. Shen *et al.*, “Deep learning with coherent nanophotonic circuits,” *Nat Photon*, vol. 11, no. 7, pp. 441–446, Jul. 2017.
- [4] N. C. Harris *et al.*, “Quantum transport simulations in a programmable nanophotonic processor,” *Nat Photon*, vol. 11, no. 7, pp. 447–452, Jul. 2017.
- [5] N. C. Harris *et al.*, “Linear programmable nanophotonic processors,” *Optica, OPTICA*, vol. 5, no. 12, pp. 1623–1631, Dec. 2018.
- [6] J. Sun, E. Timurdogan, A. Yacobi, E. S. Hosseini, and M. R. Watts, “Large-scale nanophotonic phased array,” *Nature*, vol. 493, no. 7431, pp. 195–199, Jan. 2013.
- [7] D. N. Hutchison *et al.*, “High-resolution aliasing-free optical beam steering,” *Optica, OPTICA*, vol. 3, no. 8, pp. 887–890, Aug. 2016.
- [8] J. Van Campenhout, W. M. Green, S. Assefa, and Y. A. Vlasov, “Low-power, 2×2 silicon electro-optic switch with 110-nm bandwidth for broadband reconfigurable optical networks,” *Opt. Express*, vol. 17, no. 26, pp. 24020–24029, Dec. 2009.
- [9] M. Yang *et al.*, “Non-Blocking 4×4 Electro-Optic Silicon Switch for On-Chip Photonic Networks,” *Opt. Express*, vol. 19, no. 1, pp. 47–54, Jan. 2011.
- [10] A. V. Rylyakov *et al.*, “Silicon Photonic Switches Hybrid-Integrated With CMOS Drivers,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 345–354, 2012.
- [11] K. Suzuki *et al.*, “Ultra-compact 8×8 strictly-non-blocking Si-wire PILOSS switch,” *Optics Express*, vol. 22, no. 4, p. 3887, Feb. 2014.
- [12] S. Zhao, L. Lu, L. Zhou, D. Li, Z. Guo, and J. Chen, “ 16×16 silicon Mach-Zehnder interferometer switch actuated with waveguide microheaters,” *Photon. Res., PRJ*, vol. 4, no. 5, pp. 202–207, Oct. 2016.
- [13] P. Dumais *et al.*, “Silicon Photonic Switch Subsystem With 900 Monolithically Integrated Calibration Photodiodes and 64-Fiber Package,” *J. Lightwave Technol., JLT*, vol. 36, no. 2, pp. 233–238, Jan. 2018.
- [14] K. Suzuki *et al.*, “Low-Insertion-Loss and Power-Efficient 32×32 Silicon Photonics Switch With Extremely High- Δ Silica PLC Connector,” *J. Lightwave Technol., JLT*, vol. 37, no. 1, pp. 116–122, Jan. 2019.
- [15] S. Han, T. J. Seok, N. Quack, B.-W. Yoo, and M. C. Wu, “Large-scale silicon photonic switches with movable directional couplers,” *Optica*, vol. 2, no. 4, p. 370, Apr. 2015.
- [16] T. J. Seok, N. Quack, S. Han, R. S. Muller, and M. C. Wu, “Highly Scalable Digital Silicon Photonic MEMS Switches,” *J. Lightwave Technol., JLT*, vol. 34, no. 2, pp. 365–371, Jan. 2016.
- [17] T. J. Seok, N. Quack, S. Han, R. S. Muller, and M. C. Wu, “Large-scale broadband digital silicon photonic switches with vertical adiabatic couplers,” *Optica*, vol. 3, no. 1, p. 64, Jan. 2016.
- [18] S. Han, T. J. Seok, K. Yu, N. Quack, R. S. Muller, and M. C. Wu, “Large-Scale Polarization-Insensitive Silicon Photonic MEMS Switches,” *J. Lightwave Technol., JLT*, vol. 36, no. 10, pp. 1824–1830, May 2018.
- [19] K. Kwon *et al.*, “ 128×128 Silicon Photonic MEMS Switch with Scalable Row/Column Addressing,” in *Conference on Lasers and Electro-Optics (2018)*, paper SF1A.4, 2018, p. SF1A.4.