High Port Count Silicon Photonic Switches

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Abstract: *Silicon photonic switches with port count greater than 200 is realized by combining low-loss micro-electro-mechanical-system (MEMS) switching mechanism with wafer-scale integration. We will review the design, fabrication, and experimental results of recently demonstrated 240x240 switches.*
Keywords: *Si photonic and heterogeneous platform; Photonic integrated circuit;*

I. Introduction

Silicon photonic switches have attracted a great deal of attention for their potential applications in data centers and high performance computing platforms [1][2]. Silicon photonics enables large-scale integration by leveraging well-established foundries for complementary metal-oxide-semiconductor (CMOS) integrated circuits. This is an active research area, and several switches with 32x32 or larger port counts have been reported [3]–[11]. Most switches are based on Mach-Zehnder interferometers (MZI) with thermo-optic (TO) and electro-optic (EO) phase shifters. The maximum port count of these switches is limited by the cumulative losses of long cascaded MZI chains. Though an impressive loss-to-port count ratio of 0.18 dB/port (on-chip loss) was achieved in [3], lower optical loss is needed to scale the switch size beyond 100 ports. New switch designs are likely needed to overcome this fundamental limit.

Previously, we have reported a new switching design based on MEMS-actuated vertical adiabatic couplers [8]. Unlike MZIs that have finite losses in both BAR and CROSS states, the loss in the MEMS switching element is asymmetric: it has *nearly zero loss* in the BAR (non-switching) state, and a small loss in the CROSS (switching) state. This enables construction of large-scale crossbar switch. In all switching configurations, light only passes through only one switching cell in CROSS state. The rest of the switching cells in the light path are in BAR state. This offers a more favorable scaling path towards high port count switches. A 64x64 switch with 3.7 dB on-chip loss was successfully demonstrated [8]. In principle, ring resonator (RR)-based switches also have asymmetric losses and enjoy similar scaling benefits [12]. However, the RR is intrinsically narrowband and requires matching of signal and switch wavelengths. Alternatively, one can leverage the wavelength dependence for wavelength-selective switches [13].

With optical loss under control, the maximum port count of the switch is now limited by the die size. The maximum die area is determined by the reticle of lithography equipment, which is around 2 to 3 cm. Recently, we introduced wafer-scale integration to overcome this limit. Switch blocks are stitched lithographically across reticle boundaries with low loss (0.004 dB). This led to the demonstration of 240x240 switches on 4x4 cm^2 dies [11]. To our knowledge this is the largest integrated photonic switches of any technology platforms. Figure 1 summarize the port counts and switching time of recently reported silicon photonic switches with TO, EO, and MEMS switching mechanisms. The maximum port count of silicon photonic MEMS switches is approaching that of bulk, free-space-based 3D switches, but with 10,000 times faster switching time. The sub-microsecond switching time opens up new possibilities of flow level control of data center networks. In this paper, we will present the design, fabrication, and experimental results of the high port count silicon photonic MEMS switches.

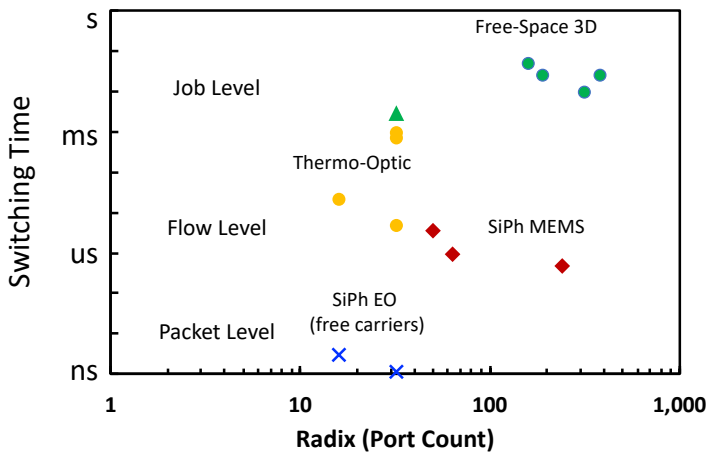

Figure 1. The switching time and port count of recently reported silicon photonic switches with thermo-optic (TO), electro-optic (EO), and micro-electro-mechanical-systems (MEMS) switching mechanisms. Commercially available free-space 3D switches are also shown for comparison.

II. WAFER-SCALE INTEGRATED SILICON PHOTONIC SWITCHES

The MEMS switch consists of NxN intersecting bus waveguides in a crossbar configuration and a MEMS switching element at each cross point. The switching element comprises a pair of adiabatic couplers with variable gap spacing. In the OFF state, the couplers are far above the bus waveguide (> 1 μm) and light propagates through the cross point with nearly zero loss. In the ON state, the coupler waveguides are physically pulled down to ~ 100 nm from the bus waveguides, and nearly 100% of light is coupled to the orthogonal waveguide (Drop port) through the two adiabatic couplers. Since there are 2N crossings in the longest optical path, they need to have very low optical loss (< 0.01 dB). This is realized by using multi-mode interference (MMI) focusing structures for both intersecting waveguides. This switch does not suffer from the cumulative losses typically seen in cascaded MZI switches as optical signal only propagates through one active switching element in the CROSS (ON) state. Prototype switches have been fabricated on 6-inch silicon-on-insulator (SOI) substrates at Marvell Nanofabrication Lab at UC Berkeley. 64x64 switches with low on-chip insertion loss (3.7 dB), fast switching time (< 1 μs), and broadband operation (> 300 nm optical bandwidth) have been demonstrated [8].

Figure 2 shows the die photographs of the 64x64, 128x128, and 240x240 switches on the same scale. Their die sizes are 1x1 cm^2, 1.6x1.7 cm^2, and 4x4 cm^2. The 128x128 switch is already approaching the maximum die size of our deep UV stepper. To overcome this limit, we have developed wafer-scale integration by stitching identical switch blocks across reticle boundaries. The mechanical placement accuracy is better than 100 nm (we measured that to be 70 nm in our experiments). To reduce the stitching loss, we tapered the waveguide width to 10 micrometers at reticle boundaries. This reduce the optical stitching loss to 0.004 dB, which is negligible compared with other losses.

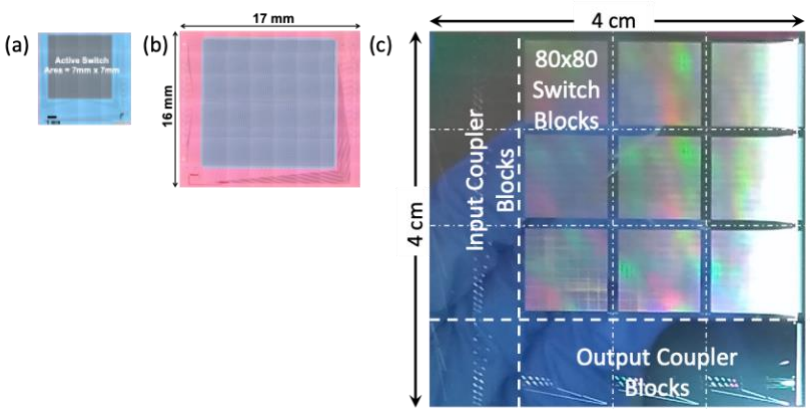

Figure 2. Die photographs of (a) 64x64, (b) 128x128, and (c) 240x240 switches on the same scale.

With wafer-scale integration, we have demonstrated 240x240 silicon photonic switches [11]. This switch uses modular design. Only three different reticles are required to create the switch: the switch matrix blocks, and the input and output blocks. Each switch block, or "switchlet", has 80x80 switches. In principle, we can use larger switchlet such as 128x128. We kept it to 80x80 so the block can fit within 1x1 cm^2 area. This allows us to tile multiple reticles on the same mask plate to save mask cost. If mask cost is not an issue, we could use larger switchlets. The resulting switch has an on-chip loss of only 9.8 dB. The loss-to-port count ratio of 0.04 dB/port is the lowest ever reported. This switch retains all the benefits of our previous silicon photonic MEMS switches, including high extinction (ON/OFF) ratio (70 dB), low crosstalk (< -60 dB) over a broad bandwidth (120 nm), and fast switching time (400 ns).

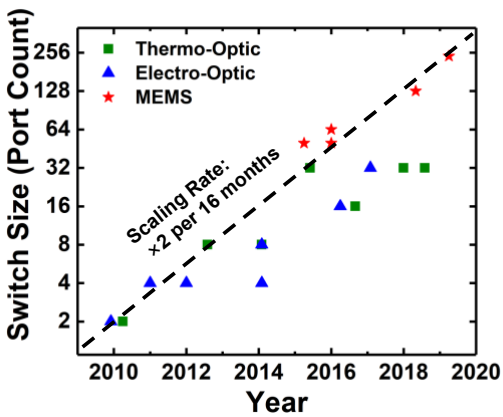

Figure 3. Port count of silicon photonic switches versus the year of publication. The maximum port count roughly doubles every 16 months from 2010 to 2019.

III. SCALING TREND

Figure 3 shows the port counts of silicon photonic switches versus the publication year for switches reported between 2010 and 2019. It is interesting to note that the maximum port count roughly doubles every 16 months, almost identical to the Moore's Law for microelectronics. With wafer-scale integration, this trend might continue to 1000x1000 switches and beyond. Packaging and electronic addressing of such large port count switches will no doubt be challenging, and will need to be addressed before successful commercial deployment.

IV. CONCLUSIONS

The combination of new silicon photonic MEMS switch design and wafer-scale integration has enabled large-scale integrated photonic switches with port count larger than 200. We have reported the concept, design, and prototype results of 240x240 switches. In addition to low optical loss (9.8 dB on-chip loss and 0.04 dB/port), the switch also has broadband operation (120 nm), fast switching time (400 ns), and low power consumption.

ACKNOWLEDGMENT

This project is supported in part by Advanced Research Projects Agency-Energy (ARPA-E) ENLITENED program (DE-AR0000849); National Science Foundation (NSF) Center of Integrated Access Networks (CIAN) Engineering Research Center (EEC-0812072) and Partnership for Innovation – Technology Transition (PFI-TT) (1827633); Google Faculty Research Award; UC Berkeley Bakar Fellow program; National Research Foundation of Korea (NRF) (2018R1C1B6005302).

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