A 120-330V, sub-µA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and over 99% Current Efficiency

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Abstract

This work presents a 4-channel, mm-scale, electrostatic and piezoelectric actuator driver that uses < 1µA total quiescent bias current and can drive actuator loads up to 120-330V at frequencies over 1kHz. The driver achieves over 99% current efficiency and can operate untethered with an integrated photovoltaic array driven by a collimated or diffuse optical power source. The circuit is tested with an off-chip boost circuit, generating over 1.5kV with 85% power efficiency at 45mW load. The system uses a simple 4-bit CMOS logic level interface with 100 kHz clock to actuate high voltage channels; on-chip photovoltaics also power the digital controller, and I/O bus.

Keywords: MEMS, DC-DC Converter, micro-robotics.

Introduction

Micro- and mm-scale robotic integration is promising for a variety of applications, but requires high-voltage electronics to actuate piezo- or electrostatic mechanical transducers [1]. Such electronics is ideally small, lightweight, and capable of driving multiple channels while untethered from physical wires [2]. Voltage requirements range from 30V-3kV at frequencies of 10-100's of Hz with actuators presenting as dominant-capacitive loads (10pF–10nF). Optical wireless power delivery can provide 100's of µW/mm^2 without the strict range limitations of near-field (inductive) coupling, yet remains underexplored for robotic applications.

Design Overview

This work presents a multi-channel actuator driver in a 650V SOI CMOS process, powered wirelessly by an on-chip silicon photovoltaic (PV) array, excited with a collimated (laser) or diffuse light source, or optionally by an off-chip voltage source. Shown in Fig. 1, the system comprises 4 actuation channels, each capable of driving a reactive actuator up to 330V. The system interfaces with an off-chip, low power microcontroller (MCU) which provides a 100 kHz clock and four logic-level CMOS control signals. A digital state machine conditions the low-voltage signals for a high-voltage level shifter and gate-driver circuit, providing needed deadtime, high-current switching activation, and low-current state-holding modes. Only *one off-chip component* is needed – a 10nF COG MLCC capacitor which decouples the HV supply during switching.

Shown in Fig. 2, solar cells are trench-isolated and stacked in series and parallel domains to provide several voltage rails. A high-voltage (HV) array uses 196 series connected cells to provide 120-140V at optical density of 1-5 mW/mm^2. A second array is used to power an off-chip MCU at ~1.8V and a third powers the I/O bus and on-chip digital control at ~3.6V.

Fig. 3 shows the HV level shift and drive circuit, state machine timing diagram, and oscilloscope screen shot of a single channel operating with the optical supply. The drive circuit uses 330V quasi-vertical DMOS devices in a complementary (class-B) configuration. The level shift circuit uses a low power 2-state current DAC to drive a floating 'accordion' OTA, referenced to the system high voltage (VDDH). When a switching transition is initiated, a high-current pulse sinks through HV

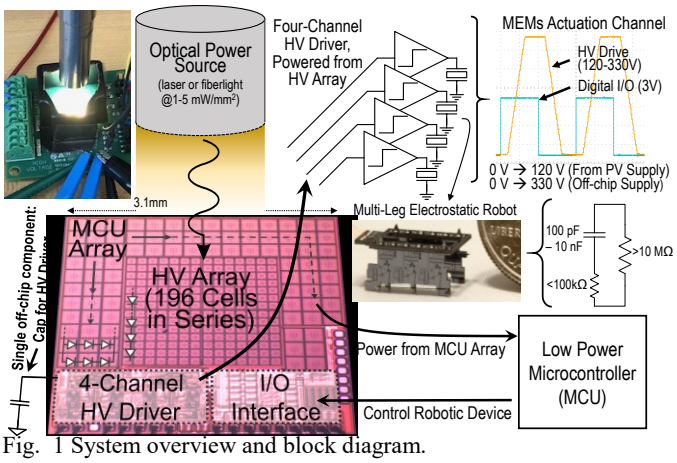


Fig. 1 System overview and block diagram.

DMOS cascode devices into differential diode-connected NMOS-PMOS pair at $V_{on,N/P}$ or $V_{off,N/P}$. The high current switching state remains for 5 clock cycles, then a low-current (90nA) state holding mode stays on for the duration of the switching state. Switching transitions are synchronized with a state machine including a 1-cycle (~10µs) deadtime between turn off/on of the complementary powertrain devices. A leakage clamp prevents residual sub-nA leakage in the DMOS cascodes from causing overvoltage stress on low voltage circuitry.

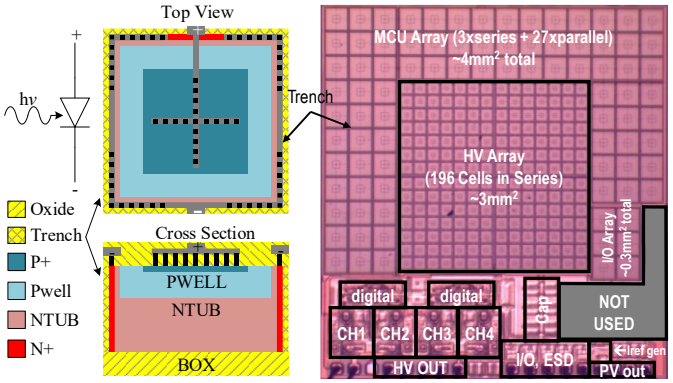
Fig 4 illustrates the operation of the floating accordion OTA which drives the HV-referenced PMOS device. When $V_{on,N/P}$ are pulled down, M1 turns on, pulling up the gate of M3/4; this charges floating nodes $V_{off,N/P}$, turning M2 off and allowing P_{gate} to pull down through M4 (turning the HVPMOS 'on'). When $V_{off,N/P}$ are pulled down, M3 and M2 turn on, pulling P_{gate} up and ensuring that M4 is off. Cross-coupling of the diode connected signals in the accordion OTA merges the gain of the PMOS differential pair and the NMOS current mirror, increasing gain, slew rate, and rise/fall time. This eliminates the use of any floating references, regulators, or latching structures, resulting in minimal quiescent power consumption other than the low-current state holding modes.

Measurement Results

The chip was tested on a PCB platform that allowed operation *either* untethered (optical power to on-chip PV arrays) *or* with a single off-chip HV supply (used to measure quiescent current, current efficiency, and the peak voltage range of the drive circuit). Shown in Fig. 5, with a 1mW/mm^2 optical power source, the circuit could achieve 125V$_{pp}$ driving capacitive loads (40pF to 1nF), used to model the input reactance of typical actuators. Drive frequency of 10-100's of Hz was achieved, limited by the available power of the PV arrays and required reactive power of capacitive loads at given frequency and voltage. An off-chip power supply was used to characterize the power consumption of the system. Since the actuator driver is *hard-switching*, it incurs loss of $C_{load}V^2_{drive}f_{sw}$ when driving reactive loads. Thus, like a linear regulator, we used current efficiency (*current delivered to load over current drawn from VDDH*) as a proxy for power utilization. With less than 1µA of

quiescent current used for the entire chip (all four channels), current efficiency remained above 99% for most of the delivered power range. This highlights the low power consumption of the level shift, drive functions, and digital interface compared to the reactive power delivery capabilities of the system.

Shown in Fig. 6, the system was also tested as a switching power stage for a HV boost DC-DC converter; two HV driver channels were configured to drive the inputs of a differential Dickson voltage multiplier, [3]. Here, the drive circuits switch the reactive impedance of a network of flying capacitors (COG) with increasing voltage rating up to 1.5kV; SMT HV diodes rectify the drive signal, providing a 5x multiplied DC voltage output. Total board area was 0.7 cm^2. Fig. 7 shows measured data for the boost converter, powered directly from a ~310V external voltage supply. The converter powertrain operated at ~1kHz to actuate the voltage multiplication stage,



	Cell Size	Cell Config.	Voltage	Notes
HV Array	125µm × 125µm	196 Series	~120-140V	• 650V SOI CMOS Process • PV Optical Efficiency ~11.5% (incl. area overhead for trench isolation) • Tested at 1mW/mm² and 5mW/mm²
MCU Array	220µm × 220µm	3 Series x 27 Par.	~1.8V	
I/O Array	220µm × 220µm	MCU + 3 Series	~3.6V	

Fig. 2 On-chip photovoltaic cells in 650V trench-isolated SOI CMOS

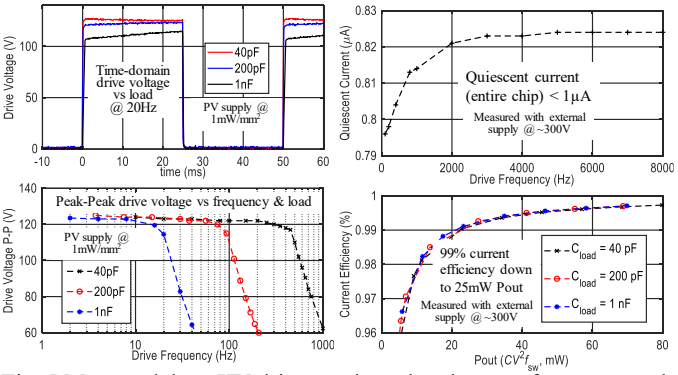


Fig. 5 Measured data: HV driver peak-peak voltage vs frequency and load cap; total quiescent current and current efficiency.

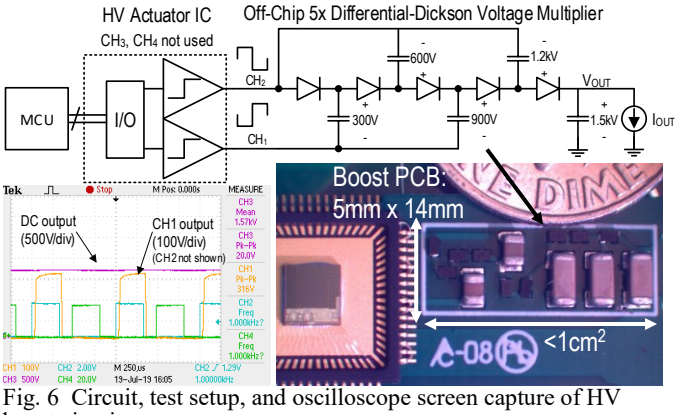


Fig. 6 Circuit, test setup, and oscilloscope screen capture of HV boost circuit

achieving output voltages over 1.5kV. Power conversion efficiency (P_{out}/P_{supply}) was up to 85% at delivered DC power of 45mW. Operating directly from the on-chip PV array with incident optical power of ~5mW/mm^2, the boost circuit achieved voltages up to 600V and peak output power over 1.4 mW.

Highlighted in Table I, this work is the first with optically powered high-voltage driving for MEMs-compatible voltages above 100V without custom post-processing steps. The PV array efficiency is the highest reported, due to the modular interconnect that increases the spatial efficiency compared to [4]. While overall system efficiency is lower compared to [5], which used a charge-recycling scheme, this work uses only *one off-chip component*, achieves higher driving voltages, and self-powered I/O and MCU control. **References**: [1] M. Karpelson, VLSI, 2011. [2] C. Bellew, TRANSDUCERS, 2003. [3] M. Forouzesh, TPEL, 2017. [4] Y. Hung, JEDS, 2017. [5] Y. Li, CICC, 2020

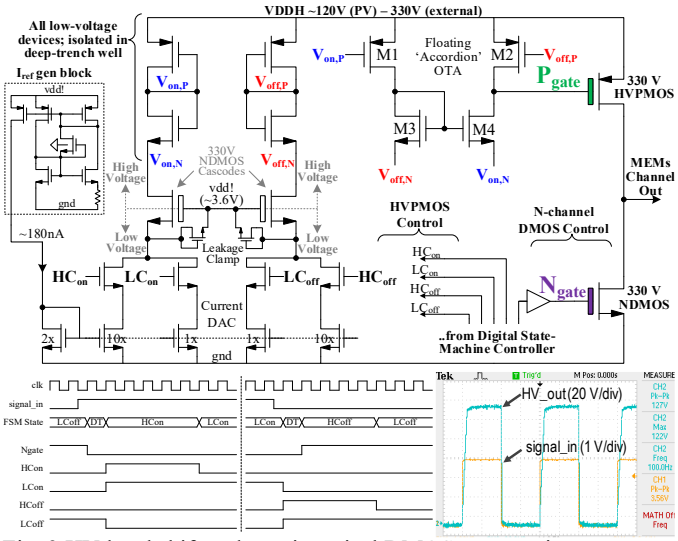


Fig. 3 HV level shift and quasi-vertical DMOS powertrain; state machine timing diagram and scope capture of driver operation.

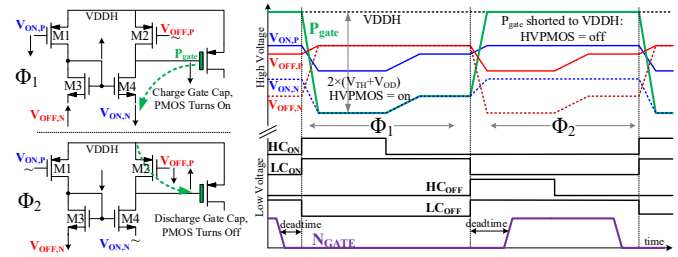


Fig 4. Floating OTA circuit and signal timing diagram

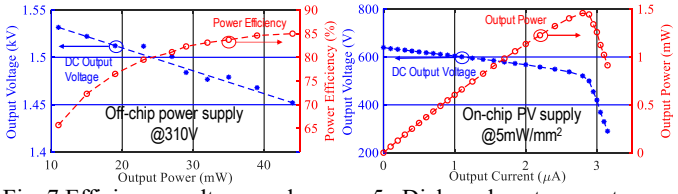


Fig. 7 Efficiency, voltage, and power: 5x Dickson boost converter.

Table I: Performance Summary

	[2] Bellew 03	[4] Hung 17	[5] Li 20	This Work
Process	Custom SOI	0.18 CMOS (cust. post-proc.)	650V SOI CMOS	650V SOI CMOS
V_{PV} (SC,max)	100 V	12.5 V	88 V (16x5.5 V)	125 V
Area Solar	32 mm^2	4 mm^2	6 mm^2	3 mm^2
Irradiation	0.76 mW/ mm^2	6 mW/ mm^2	1-5 mW/mm^2	1 mW/ mm^2
P (PV,out)	2010 µW	125 µW	Not reported	348 µW
Efficiency	8.3 %	0.5%		11.5%
LV Supply	4.5 V	No HV driver	7.4 V	3.6 V
HV Output	48 V (PV)		88/118 V (PV/ext)	125/310 V (PV/ext)
DC Gain	10.7 (20.6 dB)		16 (24.0 dB)	86.1 (38.7 dB)
# Off-Chip Components	Not reported		16×0402 Capacitors	1×0603 Capacitor