Semiconductor Science and Technology

PAPER

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To cite this article: Pramod Reddy *et al* 2020 *Semicond. Sci. Technol.* **35** 055007

IOP Publishing Semiconductor Science and Technology
Semicond. Sci. Technol. 35 (2020) 055007 (12pp) https://doi.org/10.1088/1361-6641/ab7775

Role of polarity in SiN on Al/GaN and the pathway to stable contacts

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Received 28 October 2019, revised 10 February 2020
Accepted for publication 18 February 2020
Published 25 March 2020

Abstract

Despite being the most widely used dielectric for passivation of GaN-based lateral devices, amorphous silicon-nitride still faces many stability challenges, which arise from its complex bulk electronic and interface properties on the polar (Al)GaN surfaces. In this investigation, SiN has been applied as an ultra-thin interlayer (∼3–5 nm) in vertical contact structures on Ga-polar and N-polar GaN templates to study the metal–insulator–semiconductor- (MIS-) like system and better understand the interaction between the polar surface and its dielectric overlayer. We describe the role of amphoteric ≡Si centers in SiN in passivating and providing the polarization countercharge to Al/GaN of different polarities. The consequent requirements of the concentration profile of the amphoteric defects and the corresponding chemical profile of SiN is discussed. The importance of SiN surface termination and their influence on the interface potential on Al/GaN that determines device performance and reliability is also shown. Finally, a pathway to highly stable and reliable ohmic contacts to n-type Ga-polar GaN without instabilities associated with metal directly alloying with GaN as in the case of traditional contacts is proposed.

Keywords: SiN, AlGaN, GaN, passivation, polarity, polarization, interface

(Some figures may appear in colour only in the online journal)

1. Introduction

While, essentially all dielectrics used to passivate GaAs, Si and SiC devices were investigated for passivation of electronic GaN devices [1–4], silicon nitride (SiN), ideally Si_3N_4, became the most widely used dielectric [5–8]. Nevertheless, passivation of GaN is still a research topic of great interest as SiN seems not to have been an easy or straightforward solution. The cause may be that SiN, as essentially all other passivation materials, is amorphous, making the interface to the semiconductor a crystalline/amorphous heterojunction with a high degree of disorder and defect states. This subsequently leads to interface states, which are in general deep within the bandgap. Reports on AlGaN/GaN-based field-effect transistors (FETs) suffering from instabilities have focused on piezoelectric stresses at the interface due to lattice mismatch [9]. Lattice matched InAlN/GaN heterojunction based HEMTs have been proposed as a solution with higher currents and excellent thermal stability [10, 11]. However surface-related electrical instabilities may still exist, typically addressed by proprietary schemes with no general rules. Further, SiN is a highly trap loaded dielectric and with its charge storage characteristics, it has become a functional material in Si memory device structures [12–15]. Thus, the question to pose is: how deep is the present understanding of SiN as a passivation material on GaN and AlGaN surfaces

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and could it serve as functional material on GaN like it does in Si?

This contribution tries to shine some new light on this situation. It is in part historical, in part experimental, backed by first order theory. It presents new hypotheses based on a limited number of recent studies. It starts with a historical perspective of SiN deposition and GaN device development and then discusses recent findings.

2. The SiN historical perspective

The deposition of amorphous SiN thin films on Si started to be reported in the mid 1960s using two techniques (a) radio frequency (RF) discharge promoted chemical vapor deposition (CVD) (developed into plasma enhanced CVD (PECVD)) at temperatures above 200 °C and (b) by CVD at temperatures above 700 °C, developing into low pressure CVD (LPCVD) [16, 17]. In an early study on CVD, the temperature range was scanned from 600 °C to above 1200 °C, when crystallites appeared. Such amorphous SiN was used as a mask for thermal gate oxide growth in metal–oxide–semiconductor field-effect transistors (MOSFETs) and as a cap-layer in the high-temperature damage anneal of ion-implanted patterns. It showed exceptional stability and diffusion barrier characteristics. Crystalline Si_3N_4 phases, like α (trigonal) and β (hexagonal), formed only above 1327 °C [18].

This changed in the 1970s, in particular with the development of metal–oxide–semiconductor (MOS) storage transistors, where nm thin SiN charge storage layers were inserted into MOS structures with SiO_2 or Al_2O_3 tunneling barriers, like those reported at the IEDM 1974 by Van Overstraeten [19]. The entire materials structure was amorphous, and the intermediate SiN was used for charge storage and thus appeared heavily trap-loaded in that it did not only contain disorder-induced band edge tails, but a high density of deep levels up to the concentration when defect bands could form. In these structures, it became an electrically functional material in the active area of the FET device structure beyond that of electrical, chemical and mechanical surface passivation. This application triggered continuous efforts to identify and analyze defect structures in SiN both experimentally [20] and theoretically [14, 15, 21, 22] through density functional theory (DFT). However atomistic modeling was widely based on crystalline phases like the α-Si_3N_4 and β-Si_3N_4 and the correlation with amorphous film properties was, therefore, difficult. Nevertheless, these results gave important inputs for the SiN_x on GaN study discussed below.

III–V materials whose surface electronic properties and chemical reactivity were highly dependent on surface facets, polarization and counter charges, and oxidation states, all of which are interdependent and dependent on surface treatments appeared for high-speed applications [23–29]. High-temperature processing in such a material system was more challenging. Thus, as related to SiN_x, there were two mainstream deposition technologies: LPCVD at high temperatures (700–900 °C) and PECVD at moderate (mid) temperatures (250–350 °C). The mid-temperature techniques were quickly adopted for GaAs and InP; they included also remote plasma generation to minimize surface damage. PECVD Si-nitrides could, however, be rather different in their composition and electronic behavior, depending on the precursors and reactions involved. Usually, Si would be supplied by SiH_4 or $SiCl_2H_2$ and nitrogen by NH_3 or N_2. The equipment was usually designed to operate in a temperature range below 350 °C, limited by the thermal stability of the seals used in the deposition chambers. However, in this temperature regime, NH_3 may not totally crack into N^* (nitrogen free radicals) and H^* (hydrogen free radicals). Instead, intermediate reaction products may form in the gas phase as described by the following intermediate reactions [30]:

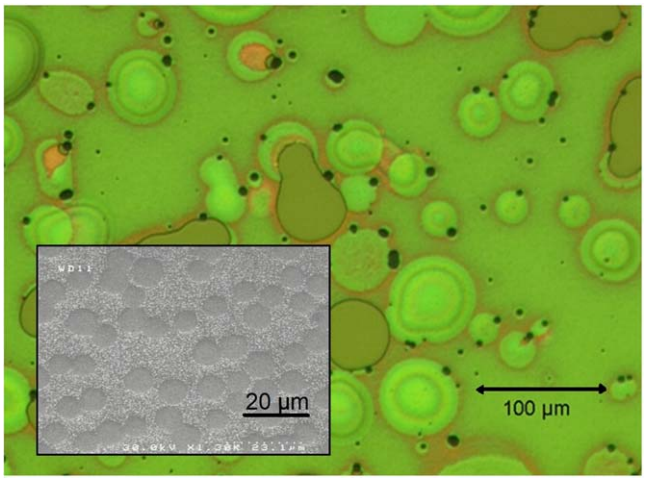

Figure 1. Optical and SEM (inset) micrograph of H-rich SiN capped with 50 nm of sputtered Si and then annealed at 650 °C. (courtesy M Alomari).

$$SiH_4 + NH_3 \rightleftharpoons SiNH + 3H_2, \quad (1)$$

$$2SiH_4 + N_2 \rightleftharpoons 2\,SiNH + 3H_2. \quad (2)$$

Thus, depending on the gas phase composition, chamber temperature and pressure, NH-radicals could be incorporated, resulting in the material usually labeled as 'H-rich'-SiN. On the other hand, not all of the Si-bonds in the Si_3N_4 matrix may become saturated and Si-related defects and clusters would remain. This material was usually labeled as 'Si-rich'-SiN. Over the last two decades, the mainstream technology for III-nitrides has also been RF-enhanced PECVD at mid-temperatures with SiH_4 or Si_2ClH_2 and NH_3 or N_2 as precursors. Recently, however, high-temperature LPCVD has become of interest.

In the case of LPCVD, which operates at temperatures above 700 °C, all NH_3 is expected to split and intermediate radicals are unlikely to be incorporated. Thus, LPCVD SiN should not be H-rich. H-rich PECVD SiN would densify during high-temperature treatments and H would outgas. If coated with a non-transparent cap (like sputtered Si or nano-diamond), this process can be observed as bubble formation and cracking (see figure 1). Thus, the H- (or rather NH-radical-) content could be substantial in PECVD grown SiN. In contrast, Si-rich SiN remains stable with temperature. However, if the material became excessively Si-rich, Si would

cluster and the appearance would become grainy. In contact with metals, a silicide could form, making the film slightly conductive. In contrast, LPCVD SiN would not suffer from H-outgassing or be excessively Si-rich.

3. The historical GaN perspective

The GaN-based materials platform was the first polar semiconductor materials platform extensively used in electronics. The Ga-polar surface of the wurtzite phase with a strong vertical polarization field is almost exclusively used in GaN high-electron mobility transistor (HEMT) technologies. In AlGaN/GaN heterostructures [31], the (differential) bound polarization charge density at the surface and interface is in the order of 10^{13} cm^{-2}, inducing surface countercharges of the same magnitude to maintain charge neutrality. The interfacial countercharge is the negative 2DEG (2D electron gas) used as the HEMT channel. The positive surface countercharge can be located in surface states, in the passivation dielectric, on the surface of the passivation dielectric or in adsorbates. In equilibrium (and as long as there is a field-effect transistor (FET) channel current present), the surface is charged [32]. A similar conclusion was arrived to by surface Fermi level measurements via x-ray photoelectron spectroscopy (XPS) studies [23].

The situation may be reflected on by the following two results published in 2000:

In the first result, the potential of the free surface on an $Al_{0.3}Ga_{0.7}$ N/GaN heterostructure was investigated by U. Mishra's group in 2000 [31], analyzing HEMTs with different AlGaN barrier layer thicknesses, and determined to be approximately 1.65 eV for an AlGaN barrier of 30% Al-content. The surface trap, labeled as a surface donor in their analysis, was ionized when the FET 2DEG channel was fully developed and would gradually be filled with electrons when the FET was driven into pinch-off. Switching the device on, electrons would be emitted, following their emission/capture dynamics. Thus, this region would act as a distributed second gate and essentially as current limiter and was thus labeled 'virtual gate' or 'slow gate', giving rise to current clipping and power slump effects.

The second result came from Lester Eastman's group also in 2000 [6]. The investigation showed that the deep surface donor trap and the related 2DEG depletion effect could actually be removed by SiN passivation, the SiN being deposited by PECVD. Depletion mode devices could be switched on without delay. It was thought that deep surface states were H-passivated. Unfortunately, H-passivation is not reliable on wide bandgap semiconductor surfaces with desorption occurring at relatively low processing temperatures of 300–400 °C [33, 34]. Many experiments with a large number of dielectrics including gadolinium and scandium oxides in addition to more 'traditional' choices such as SiO_2 and Al_2O_3, have followed, often claiming the removal of the current slump phenomenon, however, generally, only for the specific experiment discussed [1, 2, 4, 35–40]. If the picture of a deep surface donor state being the source of the 2DEG applies, GaN-based HEMT's have to generally cope with its charging/discharging characteristics and stable performance, in general, may remain out of reach.

Interestingly, SiN deposition by LPCVD was also already reported in 2003 by Shealy *et al* The deposition temperature was 700 °C [5]. The authors concluded that, applied to a HEMT structure, the depletion of the underlying 2DEG was virtually eliminated and that the surface polarization charge would reside as fixed charge in the SiN (and not in a surface donor). This was an important result, but ahead of its time. Not many details were given, and the technology did not mature to a mainstream technology in GaN based HEMT technologies.

4. Experimental

Ga-polar and N-polar GaN were grown by a rf heated vertical metalorganic chemical vapor deposition reactor (MOCVD) on c-plane sapphire. When intentionally doped, Si and Mg were employed as n- and p-type dopants, respectively. N-polar GaN was unintentionally doped with oxygen. Polarity of the epitaxially grown GaN was determined by inclusion of AlN nucleation layer (Ga-polar) or lack of it (N-polar). Further details on the GaN growth process are provided elsewhere [41, 42]. Si_3N_4 (slightly Si-rich) was deposited by LPCVD at 800 °C and 300 mTorr with dichlorosilane (40 sccm) and ammonia (120 sccm) with an *in situ* pre-cleaning step in the LPCVD deposition chamber at high temperature (above 700 °C) by NH_3. Metallization was performed by electron beam deposition. Atomic force microscopy (Asylum Research MFP-3D) was used to study the film morphology. Schottky contacts with Ni had a diameter of 70 μm for *I–V* characterization and 300 μm for *C–V* characterization. Woollam variable angle spectroscopic ellipsometer (WVASE) was used to determine the refractive index and thickness of silicon nitride. Electrical measurements were performed using a Keithley 4200 semiconductor characterization system connected to micromanipulators in a custom-built high temperature and high vacuum characterization system.

5. SiN on Al/GaN - properties, interface analysis and concept

As mentioned above, amorphous SiN is a heavily trap-loaded dielectric with defect centers well analyzed, characterized, and calibrated in Si-MOS memory device technologies [12, 13, 17, 43, 44]. Depending on the deposition parameters, Si-rich and H-rich compositions are obtained [30, 45–48]. Band tails and defect-related trap levels in the upper and lower half of the bandgap have been identified by electrical and optical analyses as well as by atomistic modeling [12–15, 17, 43, 44, 49]. In many cases, the Fermi level can be identified and located in the upper or lower half of the bandgap, making the material either n-type or p-type. Depending on stoichiometry, the electronic bandgap may not be sharply defined, can vary substantially and may deviate from the

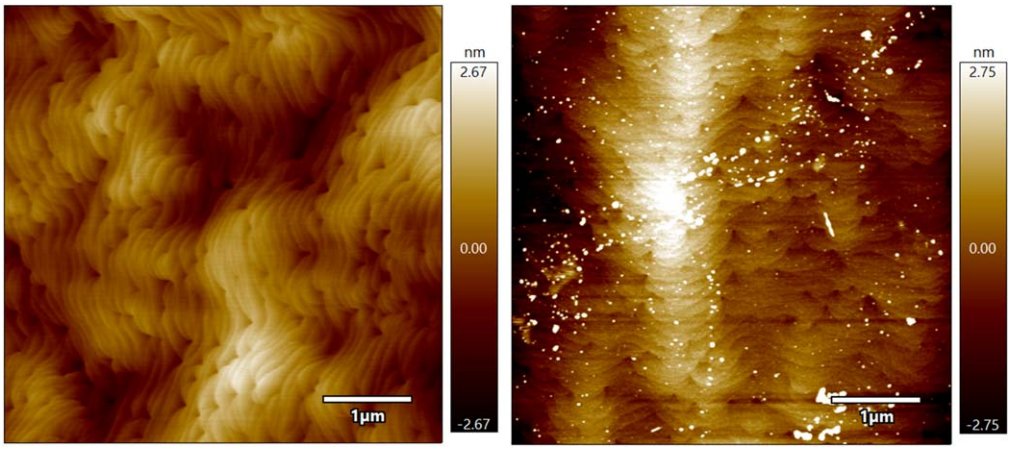

Figure 2. AFM micrographs (left): as grown Ga-polar GaN and (right): Ga-polar GaN with SiN interlayer.

optical one [50]. SiN has been incorporated, albeit with some success, in dielectric passivation schemes on AlGaN barrier layers in HEMTs and lateral power diodes [7, 51–54]. However the success is limited, may be due to the polar nature of the nitride heterostructure, which yields a charged surface and is the primary difference between GaN-based HEMTs and FET structures from other semiconductor materials. The surface charge is thought to be located in a surface defect donor state, where the energetic position and chemical structure of this state are technology dependent [23]. Accordingly, we elaborate on the above-discussed hypothesis of the surface donor configuration and alternative surface countercharge configurations that are possible when employing SiN. This hypothesis was hinted from the XPS studies of SiN/(Al)GaN interfaces on epitaxial layers deposited on sapphire (not involving a HEMT barrier layer) [24]. Here, the Fermi level lineup could be identified between SiN and the (Al)GaN conduction band edge over a wide range of compositions from GaN to AlN. To understand these results, it may be helpful to remember that SiN is a highly charge-compensated dielectric, where defect complexes could pin the Fermi level in the upper or lower half of its bandgap. In the investigation by Reddy *et al*, there was Fermi level lineup between the SiN overlayer and the (Al)GaN conduction band edge (for Al composition $<60\%$), and thus no deep donor state was observed [24]. *CV* measurements on p-type GaN showed a high barrier on the order of the bandgap, indicating no dominating additional deep surface state level in the lower half of the bandgap either. Thus, the AlGaN/SiN interface seemed (within the resolution limits of the measurement) a perfect, interface-state-free semiconductor/amorphous heterojunction.

In the experiment, the SiN layer was a 2–4 nm thin slightly Si-rich film deposited by LPCVD at 800 °C and 300 mTorr with dichlorosilane (40 sccm) and ammonia (120 sccm). The refractive index of silicon nitride is a function of stoichiometry (s = Si/N) [50]. The measured refractive index was ∼2.02 at 632 nm (a dielectric constant of $4.1\varepsilon_0$) indicating nearly stoichiometric Si_3N_4. Atomic force microscopy (AFM) surface morphology revealed a uniform conformal deposition of silicon nitride with step-flow growth mode as evidenced by the comparison of AFM micrographs of as grown GaN (RMS roughness ∼0.7 nm) and GaN with SiN (RMS roughness ∼1.4 nm) shown in figure 2. The thickness of silicon nitride was measured via ellipsometry. Its Fermi level was found at approx. 3.5 eV above its valence band edge [24], making this configuration appearing n-type. This position would indeed allow lineup with the conduction band edge of (Al)GaN. Si defects in various configurations are likely candidates, which are found in the upper half of the bandgap, to provide for the trap band configuration that would determine the Fermi level. Specifically, the ≡Si defect center could be the likely defect configuration. This defect has a $(0/-1)$ higher energy acceptor level and $(0/+1)$ lower energy donor level that are energetically close. These configurations were first calculated by J Robertson's group in 1984, using an early tight binding model [49], and reconfirmed by DFT calculations in 2001 [55]. If this were the dominating defect complex in a slightly Si-rich configuration, this could pin the Fermi level near the GaN conduction band edge [24]. Later, related to the SiN charge storage properties, more detailed atomistic calculations revealed a complex picture of the ≡Si center and double bond configurations with partially amphoteric characteristics [21, 22]. For the convenience of the reader, the two above-discussed results are shown combined in figure 3. Assuming this hypothesis applies, the necessary polarization countercharge could be located in the related defect band in close proximity to the interface. Furthermore, following the earlier analysis by Reddy *et al* [24], assuming a defect concentration of $\sim 5 \times 10^{19}\,\mathrm{cm}^{-3}$, a polarization countercharge density of $10^{13}\,\mathrm{cm}^{-2}$ could be deposited within 2 nm and could be charged/discharged by direct tunneling from the GaN or AlGaN conduction band or assisted by conduction with low activation energy within a related trap band (discussed below).

An equally important part of the SiN deposition process was an *in situ* pre-cleaning step in the LPCVD deposition chamber at high temperature (above 700 °C) by NH_3, with identical parameters as used in the pre-cleaning process of

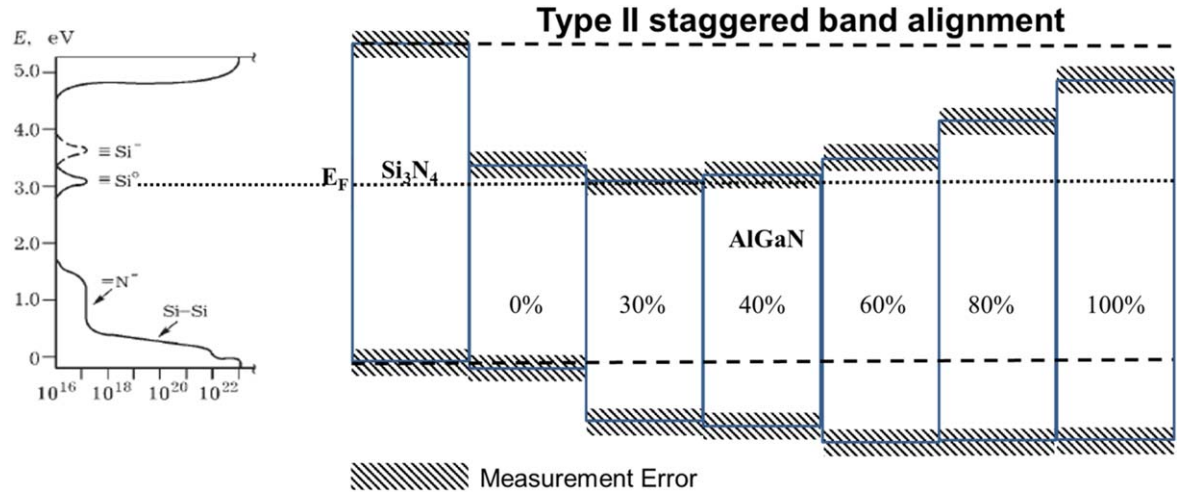

Figure 3. Left: trap distribution within the SiN bandgap, calculated by the tight binding recursion method in 1984 (reprinted from [49], with the permission of AIP Publishing). Right: Band structure lineup of LPCVD deposited SiN on AlGaN of various composition (reprinted from [24], with the permission of AIP Publishing).

GaN templates in the MOCVD chamber before further GaN growth [24]. When inserting a short *in situ* oxygen pulse between pre-cleaning and SiN deposition, the interfacial Fermi level was moved by approximately 1.4 eV into the GaN bandgap. The structure of the surface oxide was recently determined to be similar to β-Ga_2O_3 with three monolayers of oxygen [56], and is likely patchy, based on XPS results showing an average between 0.5 and 1 monolayer of oxygen [23]. This likely produces deep interface states and inhomogeneity in surface electronic properties, which lead to stability/reliability issues. It seemed, therefore, essential to reduce all of the Ga-oxide patches on the GaN surface and desorb all oxygen from this surface [24, 57].

With these experiments, the following picture emerged. It seems possible to produce a SiN/(Al)GaN amorphous/crystalline heterointerface free of deep donor interface states—in this case, by LPCVD deposition at high temperature in an oxygen-free environment. The polarization countercharge to the polarization charge was then located above this interface in a thin (several nm) SiN electron source/sink layer (hypothetically) consisting of activated $Si^{+/0}$ and $Si^{0/-1}$ defect centers within tunneling distance from the (Al)GaN interface.

However, with a defect density of this order, the defect level may start to be distributed and form a defect band. This would result in residual conduction with low activation energy, in essence representing a lossy dielectric with a resistivity still in the MΩcm range. Thus, these characteristics are in general not directly visible. In HEMTs, they will appear in the lateral gate/drain diode leakage behavior, their dynamic behavior causing current clipping or power slump effects. A lossy dielectric will be a conductor at low frequency and a capacitor above the dielectric cutoff frequency. Its signature is thus a sharp transition with a single RC-time constant. Such single RC-time constant signatures have been observed already at the beginning of the development of GaN-based HEMT technologies for a variety of heterostructure configurations as well as passivation schemes [31]. In one experiment, a spread of transition frequencies over 12 orders of magnitude was observed, indicating the difficulty to correlate such an electrical behavior with chemical/physical configurations [58]. Plotting such a dispersion curve as a function of temperature will allow the extraction of an activation energy for the conduction path. An example is discussed by Neuburger *et al*, where a transport-related activation energy of $E_{act} = 0.3$ eV was extracted (for a dielectric cutoff frequency in the MHz range) [59].

To verify the above concept, a series of experiments were designed, where thin SiN interlayers were inserted into standard metal contacts on GaN, making them dielectric assisted. In the first experiment, 2 and 4 nm thick SiN layers were inserted into Ni (70 nm) Schottky contacts on Ga-polar GaN. Figure 4 shows the forward *IV*-characteristics for 3 cases—a control sample without an interlayer, and with 2 nm and 4 nm interlayer—in the linear and semi-logarithmic scale. The control sample had near-ideal Schottky diode characteristics with a barrier height of 0.66 eV and an ideality factor close to 1.0. More details are found elsewhere [60]. After insertion of the 2 and 4 nm interlayer, the threshold voltage increased with interlayer thickness, as expected. A diode threshold voltage is a practical number used in electronic circuit design. It is not strictly defined, but rather an extrapolated number from the IV characteristic. Usually this extrapolation is performed from the linear branch (in the linear scale) representing the diode series resistance. Then, this voltage includes all voltage drops in the system except the series resistance itself. Here the expected voltage drops are across the interfacial junction itself and the interlayer lossy dielectric, raising the total apparent threshold voltage. Considering the semi-logarithmic scale, the picture is more differentiated. With 4 nm interlayer thickness, the *IV* characteristic consists of two distinct regions. At low current levels, the *IV* behavior is nearly identical to the one with 2 nm insert. At high current levels, the exponential behavior is softened, which is thought to reflect the current limiting

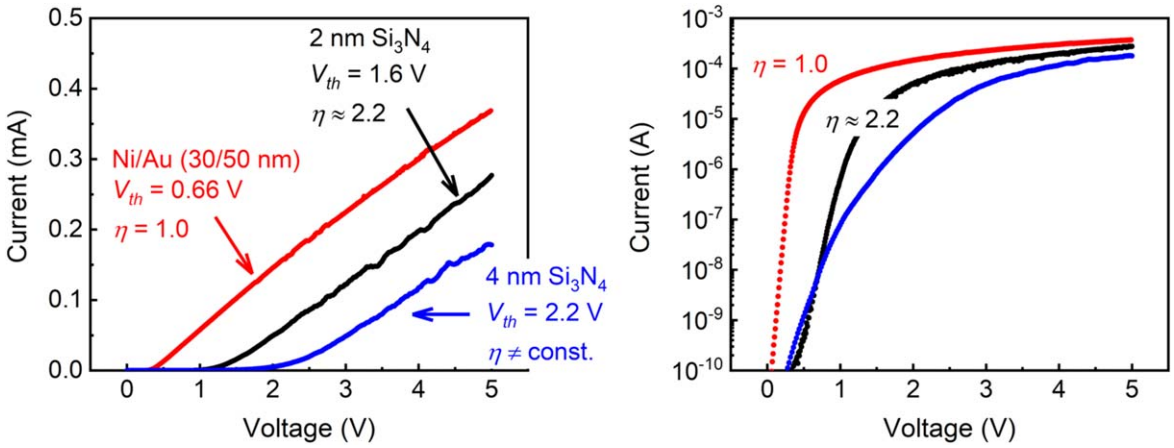

Figure 4. *IV* characteristics of dielectric assisted (Ga-polar GaN) Schottky diodes with SiN interlayer in the (left) linear and (right) semi-logarithmic scale as discussed in the text.

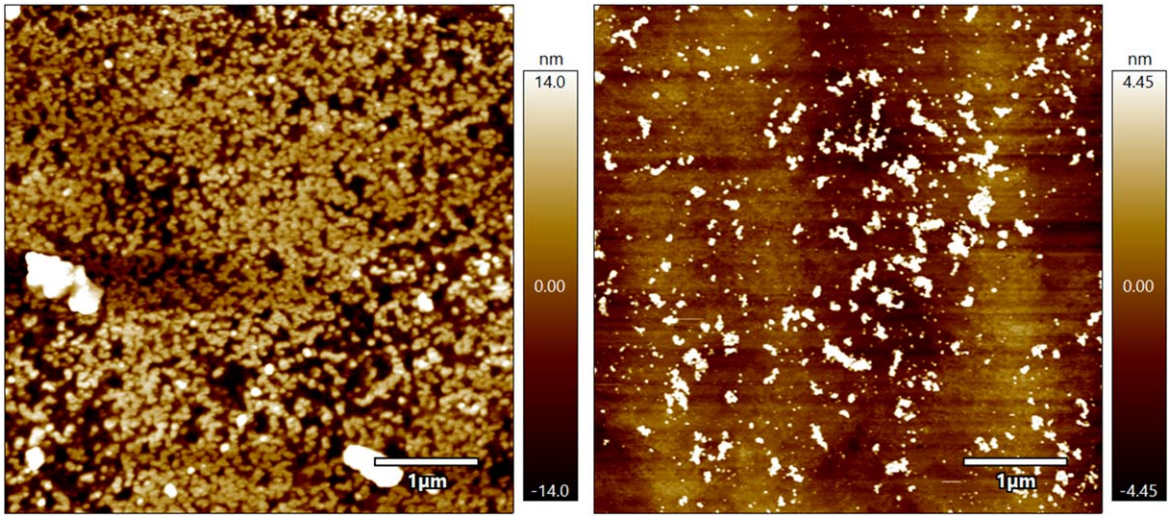

Figure 5. AFM micrographs of (left) control sample with metal alloyed without SiN interlayer and (right) sample with 4 nm SiN interlayer after metal deposition and subsequent metal removal.

influence of conduction through the interlayer. Assuming that the GaN/SiN barrier can be neglected, it appears that the barrier is moved from the GaN interface to that of the SiN/Ni interface and has become independent of the SiN interlayer thickness. The system could now be described as a metal–insulator–semiconductor (MIS) system, in-part surface barrier controlled, in-part bulk controlled. In this picture, the SiN interlayer hosts the GaN polarization countercharge and the depletion layer charge of the Ni/SiN junction interconnected by a thin n-type SiN lossy dielectric region with a defect-controlled Fermi level.

In a second group of experiments, a 4 nm SiN interlayer was inserted into a conventional Ti/Al/Ni (30/100/70 nm) ohmic contact metallization system (without Au overlayer) and compared to a control sample without interlayer. The surface of GaN and the surface of SiN deposited on GaN were similarly smooth, with the atomic steps shown in figure 2 indicating conformal deposition of SiN. After alloying at 850 °C by rapid thermal annealing (RTA) in N_2, followed by aqua regia etching for metal removal, the control experiment (without SiN interlayer) showed roughening of the GaN surface to ∼10 nm (RMS), indicative of metal/GaN inter-mixing (figure 5 (left)). Figure 5(right) shows the surface of the sample with the SiN interlayer after metal deposition, annealing and again aqua regia-based metal etching. The surface roughness remained similar to that of as-grown GaN, strongly indicating a lack of GaN/metal alloying due to SiN acting as a strong diffusion barrier.

The metal structure on SiN before annealing is still layered with Ti in contact with the SiN interlayer on the GaN surface. The *IV*-characteristic is rectifying, similar to that of the Ni contact with SiN interlayer, but with a lower threshold voltage (see figure 6 left). By contrast, annealing renders the *IV* characteristics linear (see figure 6 right), despite the SiN interlayer remaining in place and a lack of Ti-alloying with GaN (inferred from the lack of increased roughness). To understand this feature, two reactions are likely to have appeared. The metallization became an alloy with many phases, as usually observed. Secondly, the barrier materials between the multiphase metallization and the SiN interlayer

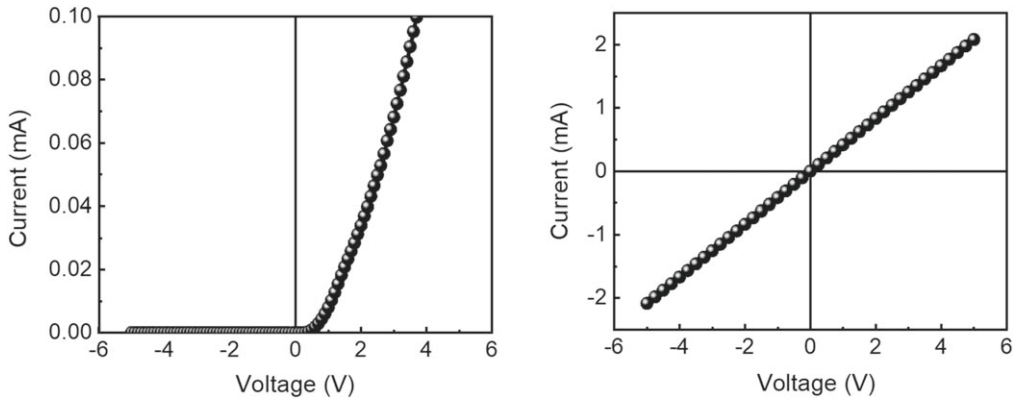

Figure 6. *IV* characteristics (left) before and (right) after contact alloying for Ga-polar GaN samples with 4 nm SiN interlayer.

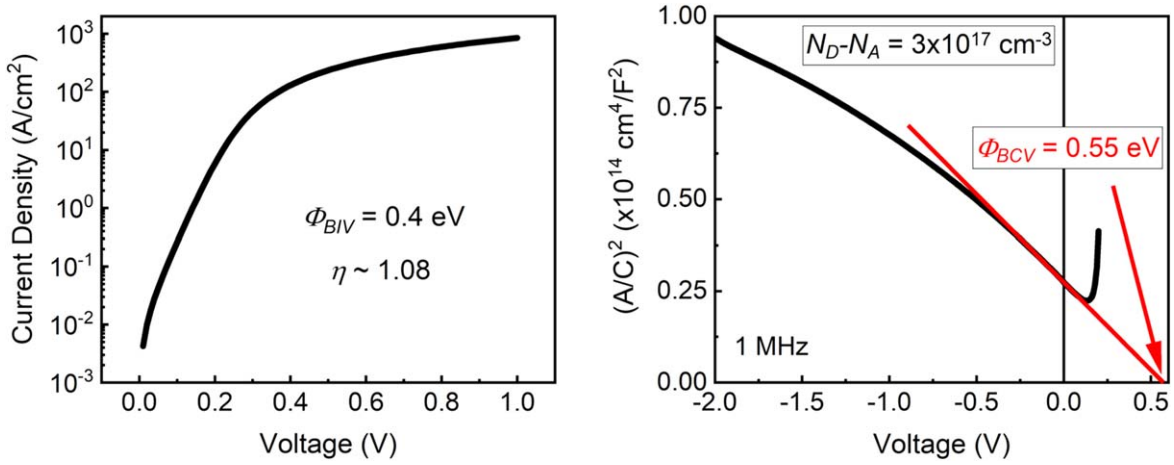

Figure 7. (left) *IV* and (right) *CV* characteristics of a Ni-diode on N-polar (2.6 μm n-type) MOCVD-grown GaN realized by e-beam evaporation and patterned using a shadow mask.

surface reacted. This lowers the barrier and introduces a partial tunneling junction with an electrochemical potential that is energetically aligned with the defect band in the SiN, which, in turn, is lined up with the GaN conduction band. More light is shed on this possibility by the experiments on the N-polar GaN surface discussed below. The results indicate that ohmic contacts to n-type Ga-polar GaN can be obtained without direct alloying into GaN. This may then open a possible path to form highly temperature-stable and, thus, highly reliable ohmic contacts on this surface.

In order to understand the relation between the polarization charge, storage of counter-charge and effective passivation, a third group of experiments based on the interlayer configuration has been applied to the n-type nitrogen-polar GaN. This N-polar surface is chemically more reactive than the Ga-polar surface and the polarization countercharge is negative, which lowers work function differences (i.e. barrier heights) to metals and makes stable Schottky barriers difficult to obtain. It is, therefore, the much less used surface. In spite of such a surface, we fabricated near-ideal Schottky-barrier diode structures. The layer was MOCVD grown on sapphire and n-type oxygen self-doped. The Schottky metal was Ni, evaporated by e-beam in ultra-high vacuum (UHV), patterned by a shadow mask. No surface treatments were performed prior to evaporation. The *IV* and *CV* plots are shown in figure 7. The diode *IV* characteristics showed an ideality factor of $\eta = 1.08$ and a barrier height of $\Phi_{BIV} = 0.4$ eV. The $1/C^2$ plot showed a doping level of N_D–$N_A \approx 3 \times 10^{17}\,\mathrm{cm}^{-3}$ and an extracted barrier height of $\Phi_{BCV} \approx 0.55$ eV, comparable with values for Ni contacts on N-polar surfaces without extrinsic dielectric interlayers published in the literature [61, 62].

In a following experiment, a 6 nm LPCVD SiN layer was deposited by a process similar to that employed on Ga-polar GaN described earlier, then the sample was split into two parts. The control sample (A) received a Ni-contact using the process as described earlier. The other half of the sample (B) was dipped into a 10% HF solution, followed by a water rinse. During this treatment the SiN layer was thinned by about 0.5 nm, determined by CV analysis. Then a Ni-contact was deposited using the same process as the sample A. The rationale for the modification was as follows: the amorphous SiN surface is chemically unstable and the surface will become oxygen-terminated and, eventually, hydroxides and a stable oxy-nitride layer will form [63]. It was expected that by the HF dip, the oxygen termination could be removed when immediately transferred into UHV. Thus, the experiment was designed to determine whether the SiN termination would change the metal/SiN barrier height (which is expected to be

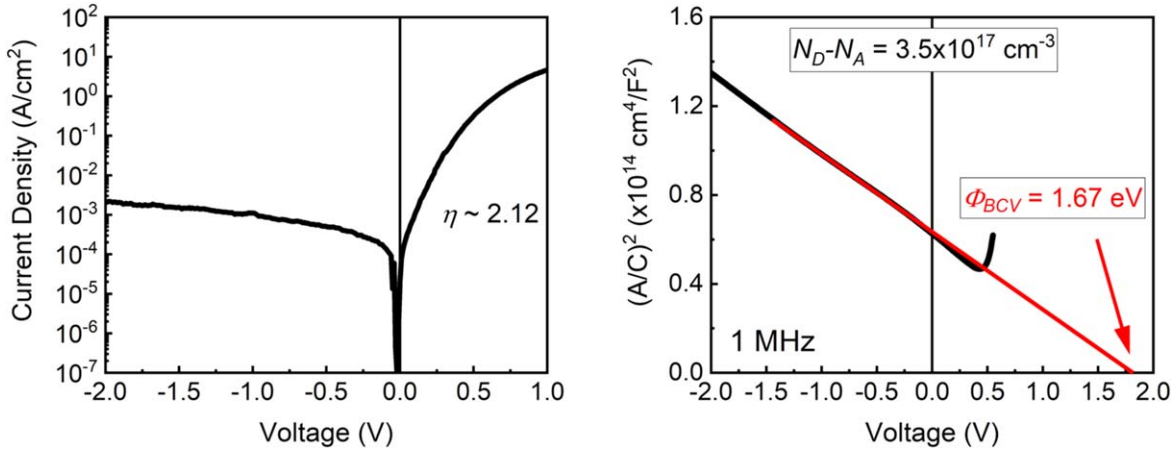

Figure 8. *IV* and *CV* Ni-diode characteristics (N-polar GaN) with 6 nm LPCVD SiN (on 2.6 μm n-type N-polar GaN) interlayer stored in air before metal deposition (sample A).

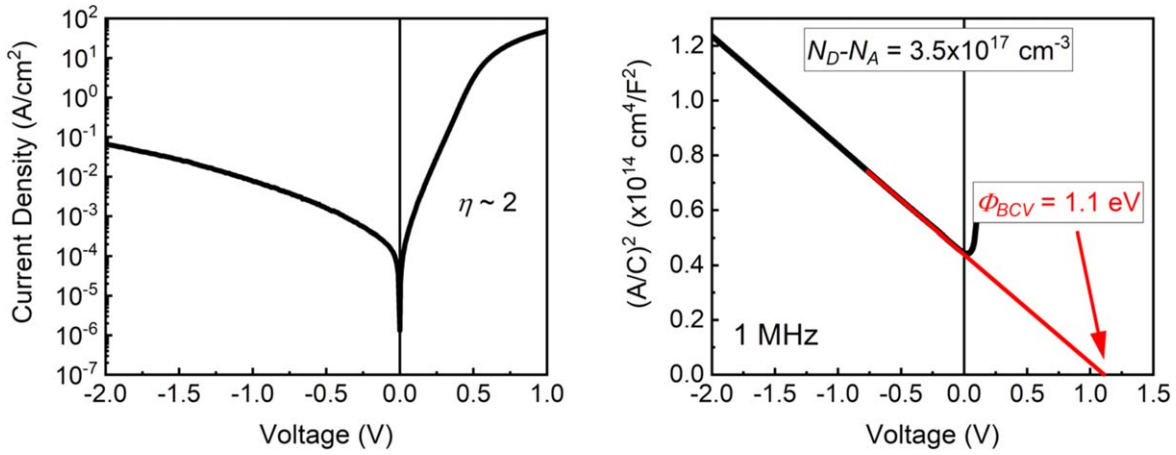

Figure 9. *IV* and *CV* Ni-diode characteristics (N-polar GaN) with 6 nm LPCVD SiN (on 2.6 μm n-type N-polar GaN) interlayer treated with a 10% HF dip before metal deposition (sample B).

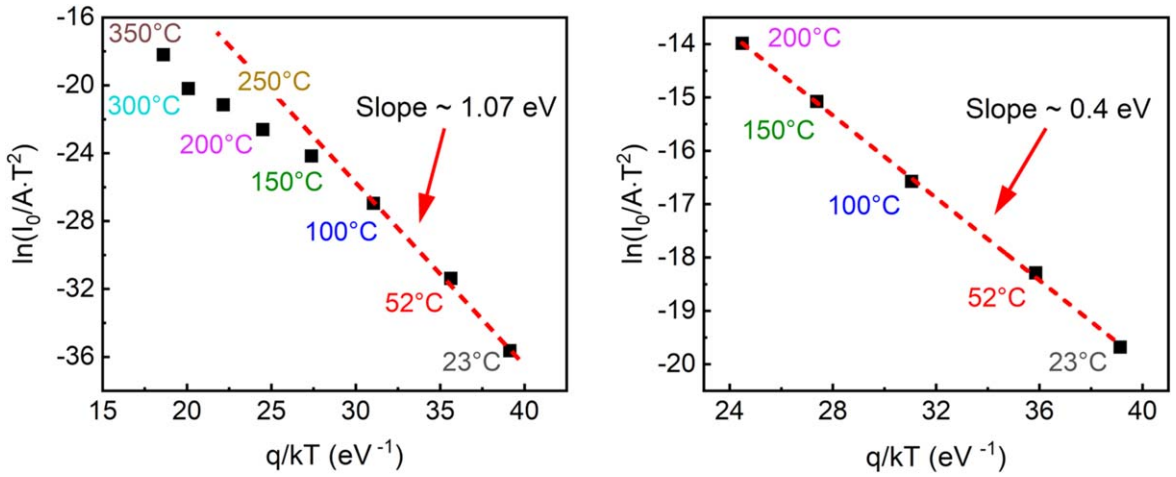

Figure 10. Barrier height extraction from temperature dependent *IV* characteristics for (N-polar GaN) sample A, (left) and B (right). The temperature was measured on the semiconductor surface by a thermocouple and calibrated to metal melting points.

the case) and whether this could be observed in this MIS system on the N-polar GaN surface. The results are summarized in figures 8–11. Figure 8 shows the *IV* and *CV* plots at room-temperature (RT). Due to the dielectric interlayer, the ideality factor was increased to $\eta = 2.12$ and the extracted *CV* barrier height was $\Phi_{BCV} = 1.67$ eV. The extraction of the barrier height and ideality factor is described elsewhere [24, 60]. The *CV* barrier height now includes the SiN

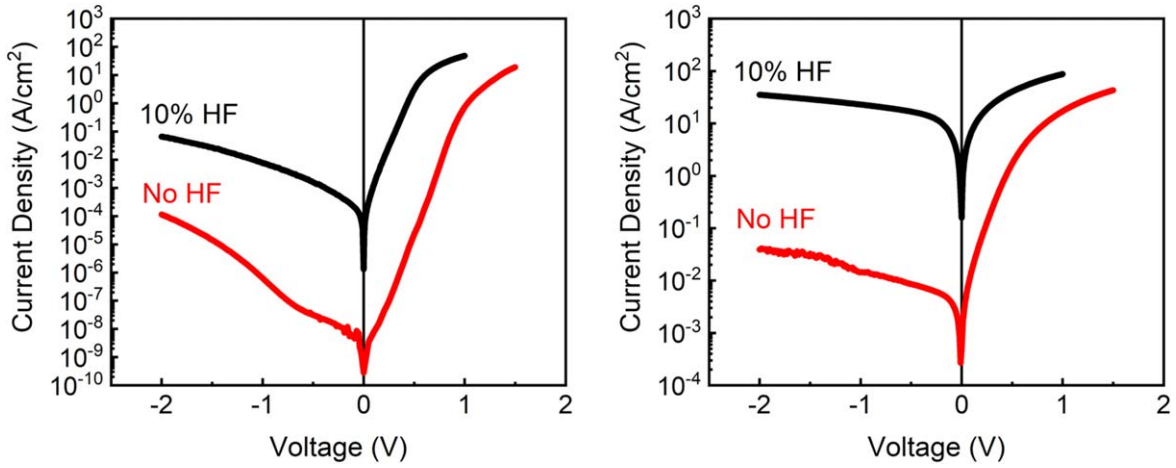

Figure 11. Forward and reverse *IV* plots of (N-polar GaN) diodes A (red solid line) and B (black solid line) tested in vacuum at RT (left) and 350 °C (right).

interlayer capacitance and should, therefore, be higher than the surface barrier alone.

In figure 9, comparable plots are shown for the sample B after the HF dip. The ideality factor in the *IV* characteristics is again increased to $\eta \approx 2.0$ and the extracted *CV* barrier height is now $\Phi_{BCV} = 1.1$ eV, including the 6 nm thick SiN interlayer capacitance. Thus, the total barrier, in this case, seems to be slightly lower. A more detailed picture can be developed considering the temperature dependent *IV* plots.

Figure 10 shows the extracted Richardson plot [64] from forward bias measurements performed in vacuum as a function of temperature up to 350 °C. Detailed procedure of the *IV* barrier height extraction using temperature dependent *IV* is provided elsewhere [60]. For the oxygen-terminated SiN (sample A), a linear slope is only seen in the lower temperature range, while it deviates significantly at higher temperatures. This indicates contributions of barrier inhomogeneity and defect assisted tunneling [64–69]. In the case of the HF-treated, sample B, the barrier height is constant with temperature ($\Phi_{BIV} \approx 0.4$ eV), indicating a homogeneous interface and a thermionic emission-dominated current [60, 64, 66, 70, 71]. The difference in the barrier height is also reflected in the forward as well as reverse *IV* characteristics as shown in figure 11 for RT and 350 °C operation (measured in vacuum). At RT, the ratio of forward bias current (I_{Forw}) to reverse bias current (I_{Rev}) at ±1 V is approx. 10^3 for the HF treated low barrier sample B and 10^9 for the high barrier sample exposed to the air (sample A). At 350 °C operation, the *IV* characteristics of the low barrier diode (sample B) becomes nearly linear, and the $I_{\mathrm{Forw}}/I_{\mathrm{Rev}}$ ratio of the high barrier diode (sample A) is reduced to approx. 10^4. In addition, the reverse current in the sample A increased by approx. 6 orders of magnitude by defect activation. Interestingly, irreversible changes were observed for operation above 450 °C in sample B and 750 °C in sample A, indicating better chemical stability for the oxygen terminated SiN in spite of the non-ideality in the temperature dependence of the barrier height.

Low barriers on SiN have also been observed in the case of LPCVD-deposited SiN-assisted Schottky barriers [24]. Here, the surface potential was associated with the location of the central neutral level in the ideal SiN. However, and quite obvious from the above experiments, the surface termination of the SiN interlayer had a significant influence on the diode barrier characteristics as well as the diode thermal stability. When the metal (Ni) is in a direct contact with the N-polar surface, a small barrier height is observed. Fairly identical values are measured for diodes with a SiN interlayer, when the surface oxygen termination was removed by an HF dip. This low value may now reflect a residual barrier between the N-polar GaN and the amorphous SiN overlayer and/or the SiN interface in contact with the Ni contact metallization (no Au overlayer). More detailed measurements are needed to identify the various contributions in this leaky dielectric MIS system. The low thermal chemical stability in this case may point towards an interaction between the Ni and Si-clusters in the Si-rich SiN materials matrix. Ni-silicides could indeed form at around 400 °C [72]. In case of the oxygen terminated surface, the extracted barrier is at a higher 1.07 eV. Thus, it seems that in this case, the diode barrier is indeed determined by the SiN/Ni interface and here by the SiN oxygen termination where, on the unprotected free surface in contact with atmosphere an adsorbate (such as moisture) related redox potential will develop with a barrier referenced against the ≡Si defect, and a related surface potential will appear.

6. Discussion and conclusion

For a long time, 'Si-rich' SiN has been recognized as a specific region in the amorphous SiN phase. Within this region, ≡Si defect center can pin its Fermi level, which makes it closely lined up with the GaN conduction band edge. It is thus n-type and it may be labeled as 'n-type SiN'. Despite being used in Si memory FETs for a long time, this region has not

yet been well specified, reproduced, or calibrated in respect to its application to the (Al)GaN materials system.

The lower limit of defect concentration will correspond to a case where a polarization counter charge density on the order of $10^{13}\,cm^{-2}$ can be deposited within the tunneling distance from the interface, where a defect band can form. On the other hand, an upper limit will be seen when Si starts to cluster into neutral agglomerates, compromising the electronic bandgap and chemical stability of the amorphous phase. Thus, this n-type SiN is heavily doped and behaves as a lossy dielectric with residual conduction. In MIS device structures, the band diagrams do not usually consider a Fermi level position and band bending in the dielectric layer, which is certainly an over-simplification for the case where wide bandgap—not narrow bandgap—semiconductors are used. However, the entire Si defect center complex is amphoteric and can thus balance positive polarization countercharges on the Ga-polar surfaces as well as negative polarization countercharges on the N-polar surfaces with a small energetic difference (∼0.4 eV, figure 3), which is close to the resolution limit of the XPS analysis. This value may thus still represent a residual barrier between (Al)GaN and n-type SiN.

If potential barriers are seen on an essentially barrier-free interface between GaN and n-type SiN, they need to appear at the SiN interface/surface, either to metals or the atmosphere. In the ideal case, barrier heights to metals will be practically identical for the Ga- and N-polar surfaces (they will be either low or high depending on the SiN surface termination). Clearly, SiN possesses a reactive surface, which needs to be stabilized to be reliable. This stabilization will occur naturally by substituting oxygen for nitrogen at a region near the surface. Then, the reactivity becomes comparable to that of a Si-oxide (with SiO, SiO_2, or hydroxide surface bonds) and barriers to metals become also similar to those on Si-oxide. In air, a Si-oxide related redox couple will develop (like the OH-related one), determining the free surface potential. To shield a GaN surface from the environment, it is important that the depletion layer in the n-type SiN can fully develop without reaching through to the rear side, where the polarization countercharge is also deposited at identical defect levels. Thus, defect concentration and defect band formation, nm thickness control, and SiN termination are critical parameters. Most experiments have thus far been rather rudimentary, aiming to verify the concepts first yet still lacking design rules for process optimization.

As we showed in this work, ohmic contacts can form in the presence of a SiN interlayer. After metal deposition, a barrier between the layered metal/Si-nitride formed, resulting in rectification. During these experiments, the SiN surface was exposed to air between the processing steps, which caused oxidation and the formation of the oxide-related barrier. This is consistent with the results obtained on the N-polar surface and the SiN surface termination model may be considered a unifying model for both cases. However, after alloying of the top metallization, the electronic barrier was reduced without direct alloying with the GaN substrate and the contact *IV* became linear i.e. the ohmic contact is formed by reducing the electronic barrier and not by alloying or tunneling as seen in typical ohmic contacts. Details of the reactions responsible for this change have, however, not yet been identified. It may be speculated, that at the alloying temperature of 850 °C, the oxygen termination on the SiN is (at least partially) removed and this interfacial oxygen may be consumed by one of the metals: Ti, Al, Ni, or Si. Also, metal-nitride phases, like TiN, are thought to have formed as part of this reaction. These N-containing phases (protrusions) could line up with the GaN conduction band edge, serving as tunneling paths now also containing an additional SiN tunneling layer. Thus, a higher contact resistance is expected. The results also indicate that ohmic contacts to n-type Ga-polar GaN can be obtained without direct alloying to GaN, opening the possibility of forming highly stable and reliable ohmic contacts on this surface.

The key lies in the concept of using a dielectric with a point-defect level of high density, above $10^{19}\,cm^{-3}$, forming a defect band aligned with the semiconductor conduction band edge, to deposit the polarization countercharge within the tunneling distance from the interface. This comes, however, with the consequence of a related defect band conduction with a low activation energy, and, thus, with a dynamic conduction signature of a lossy dielectric. The deposition technique in this work was LPCVD that included an *in situ* cleaning step. Similar LPCVD deposition schemes have recently been applied to GaN-based HEMTs and discussed in the literature. Unfortunately, no details are given on the specifics of the LPCVD process used, which makes a direct comparison with the data obtained here difficult. Nevertheless, a recent paper on HEMT technology on N-polar templates reports on stable gate contacts obtained by the insertion of a SiN interlayer deposited by MOCVD (the deposition temperature was not reported but may have been similar to temperature range used in LPCVD SiN deposition) between the GaN surface and Ti gate contact [54].

However, recently *in situ* MOCVD deposition of SiN in an AlGaN/GaN MISHEMT structure at 1100 °C was reported [51]. This temperature is already in the transition range for crystallite formation as observed already in one of the first experiments reported in 1967, mentioned above [17]. And indeed, here the formation of a monocrystalline interface could be identified by high-resolution transmission electron microscopy (HRTEM); thus a crystalline SiN/GaN junction had been formed.

Acknowledgments

The authors gratefully acknowledge many fruitful discussions on this difficult and complex subject over the many years with many colleagues in the field, especially Sylvain Delage of Thales, Mohammed Alomari of IMS (Stuttgart), and Clemens Ostermaier of Infineon. The authors also acknowledge funding in part from NSF (ECCS-1508854, ECCS-1610992, ECCS-1653383, ECCS-1916800), ARO (W911NF-15-2-0068, W911NF-16-C-0101, W911NF-18-1-0415, W911NF-14-C-0008), AFOSR (FA9550-17-1-0225).

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