Polylithic Integration for RF/MM-Wave Chiplets using Stitch-Chips: Modeling, Fabrication, and Characterization

Ting Zheng[#1], Paul K. Jo[#], Sreejith Kochupurackal Rajan[#], Muhannad S. Bakir[#2]
[#]School of Electrical and Computer Engineering, Georgia Institute of Technology, USA
[1]ting.zheng@gatech.edu, [2]mbakir@ece.gatech.edu

***Abstract*— A polylithic integration technology is demonstrated for seamless stitching of RF and digital chiplets. In this technology, stitch-chips with compressible microinterconnects (CMIs) are used for low-loss and dense interconnection between chiplets. A testbed using fused-silica stitch-chips with integrated CMIs is demonstrated including modeling, fabrication, assembly, and characterization. A 500 μm-long stitch-chip signal link is measured to have less than 0.4 dB insertion loss up to 30 GHz. A simulated eye diagram for 1000 μm-long stitch-chip signal link has a clear opening at 50 Gbps data rate. Moreover, the S-parameters of the CMIs are extracted from this testbed and show less than 0.17 dB insertion loss up to 30 GHz. Benchmarking to silicon interposer based interconnection is also reported.**

***Keywords*— RF measurements, de-embedding, transmission lines, flexible interconnects**

I. Introduction

3D monolithic integration is widely studied to overcome scaling limitations such as increased interconnect delays for digital applications [1]. Some of the challenges of such an integration technology for RF/mm-wave applications include high design complexity, poor thermal management, and poor heterogeneous integration flexibility in materials and devices [2]. In contrast to monolithic integration, polylithic integration has the potential to address these challenges while maintaining monolithic-like performance.

To meet the increasing data communication demand of RF/mm-wave applications, such as fifth-generation (5G) wireless and internet-of-things (IoT), any polylithic integration technology should fulfill the following requirements: first, signal interfaces between different chiplets (i.e. RF-to-RF, RF-to-digital, and digital-to-digital) must be low-loss, low-parasitic, and provide virtually no impedance discontinuities [3]. Second, it should be compatible with chiplets sourced from different materials, processes, and foundries. For example, an RF front-end of a multiple-input/multiple-output (MIMO) 5G system consists of antenna arrays, low noise amplifiers (LNAs), power amplifiers (PAs), variable gain amplifiers (VGAs), and etc. While LNAs and PAs are fabricated on gallium arsenide (GaAs) substrate commonly, other circuits are fabricated with different Si-based processes [4].

To meet these requirements, the polylithic integration technology shown in Fig. 1 is demonstrated. The key feature of the demonstrated technology is the concatenation of heterogeneous chiplets using stitch-chips. For this RF/mm-wave applications, the stitch-chips are formed

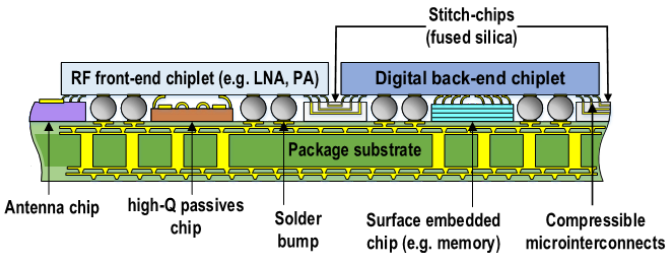


Fig. 1. Envisioned polylithic integration using stitch-chips for RF/mm-wave applications

using a low-loss dielectric material and consist of short transmission lines (approaching less than 100 μm) with compressible microinterconnects (CMIs) on both ends to interface with the chiplets. CMIs are 3D interconnects that provide pressure-based interconnections between chiplets and stitch-chips [5]. They possess several mechanical and electrical advantages over conventional solder bumps: first, CMIs do not form intermetallic compound (IMC), which increases with bump-pitch scaling and causes mechanical reliability issues (e.g. cracking) [6]. Moreover, while shorting becomes an issue for fine-pitch solder bumps during thermo-compression bonding, it is not a concern for CMIs. For system-level benefits, the proposed polylithic integration technology can provide means to separate passives from lossy silicon chiplets. By integrating these passives on low-loss surface embedded chips, the RF/mm-wave system performance, which depends on the performance of passives (e.g. Q factor of inductors) [3], can be boosted. In addition, more functionalities, such as antennas, can be integrated on the stitch-chips.

In this paper, for the first time, RF modeling and characterization of fused-silica stitch-chips with integrated CMIs are reported. The measured de-embedded S-parameters are used to evaluate signal integrity (SI) performance of the stitch-chips and the results are benchmarked to silicon interposer. In addition, due to the difficulty of directly probing the CMIs, which are 3D mechanically flexible interconnects, and to gain full insight into the performance of the stitch-chips and CMIs, this paper demonstrates a testbed with L-2L de-embedding method for the CMIs, or any other off-chip I/O technology, and validates it experimentally.

The organization of this paper is as follows. Section II describes modeling and de-embedding method of the testbed. Section III reports the fabrication of the CMIs and assembly process. In Section IV, the characterization and analysis of the

stitch-chips and the CMIs are discussed.

II. RF Modeling and De-Embedding Method

As shown in Fig. 2a, the testbed is designed in ANSYS HFSS and emulates a fully assembled stitch-chip system using flip-chip bonding. Fused-silica is selected as the substrate material for the stitch-chip and the CMI-chip due to its low-loss attributes (low dielectric constant ∼3.9 and low loss tangent ∼0.0002 for up to 30 GHz). Coplanar waveguides (CPWs) are formed on the stitch-chip, while two ground-signal-ground (G-S-G) pairs of gold-coated NiW CMIs with probing pads are formed on the CMI-chip. The CPWs and the CMIs are coated with electroless plated gold to prevent oxidation [7]. Note that this gold layer is also critical to reduce NiW CMI's loss due to gold's higher conductivity and larger skin depth at high frequencies. Fig. 2b shows the device under test (DUT) in this testbed consisting of probing pads, CPWs and CMIs. Fig. 2c shows a schematic of CMIs with obvious curved sidewalls, which enable their out-of-plane mechanical flexibility [5].

The procedure of de-embedding involves two steps and uses ABCD-parameters converted from S-parameters. The first step is to remove the probing pad parasitics as shown in Fig. 3a, which can be summarized using the following matrix computation:

$$[Thrupads] = [Pad][Pad] \tag{1}$$

$$[DUT] = [Pad][Link][Pad] \tag{2}$$

$$[Link] = \sqrt{[Thrupads]}^{-1}[DUT]\sqrt{[Thrupads]}^{-1} \tag{3}$$

The probing pad parasitics are removed for two DUTs, one with L-length CPW and the other with 2L-length CPW. The results are denoted as [Link1] and [Link2], as shown in Fig. 3b. In Fig. 3b, [CMI] and [L] are the ABCD-parameters of CMIs

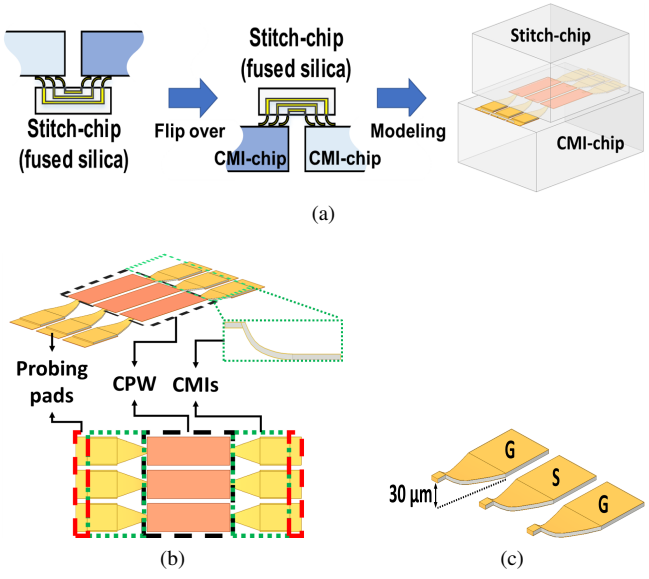


Fig. 2. HFSS model for the testbed: (a) modeling procedure, (b) schematic and top view of a device under test, and (c) schematic of G-S-G CMIs

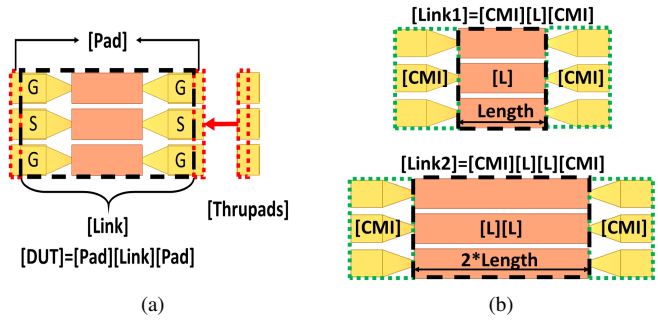


Fig. 3. L-2L de-embedding procedure: (a) top view of pad parasitics removal and (b) top view of L-2L de-embedding models

and L-length CPW, respectively. Next, L-2L de-embedding [8], [9] is utilized and can be described as follows:

$$[Link1] = [CMI][L][CMI] \tag{4}$$

$$[Link2] = [CMI][L][L][CMI] \tag{5}$$

$$[CMI] = \left(\sqrt{[Link1]^{-1}[Link2][Link1]^{-1}}\right)^{-1} \tag{6}$$

The CPW is 1.5 μm-thick copper with 0.5 μm-thick gold. Center signal conductor is 170 μm in width and is 30 μm spaced from adjacent ground traces. These dimensions result in 50 Ω characteristic impedance. The CPWs on the stitch-chips are 500 μm and 1000 μm in length to enable L-2L de-embedding. The size of probing pads is 170 μm×250 μm. Furthermore, 30 μm-high CMIs are used with 0.5 μm-thick gold coated on all surfaces.

III. Fabrication and Assembly of the Testbed

The fabrication process is described as follows. While a lift-off process is only needed for the CPWs on the stitch-chips, Fig. 4 shows the fabrication process of CMIs on the CMI-chips. The fabrication process begins with the pads' lift-off process and a sacrificial photoresist layer spin coating. Next, the photoresist layer is patterned to obtain a curved sidewall [5]. Next, after Ti/Cu/Ti seed layer sputtering, another photoresist layer is spray coated and patterned for CMI NiW electroplating. Following electroplating, the photoresist layers and the seed layer are removed to release the CMIs. Finally,

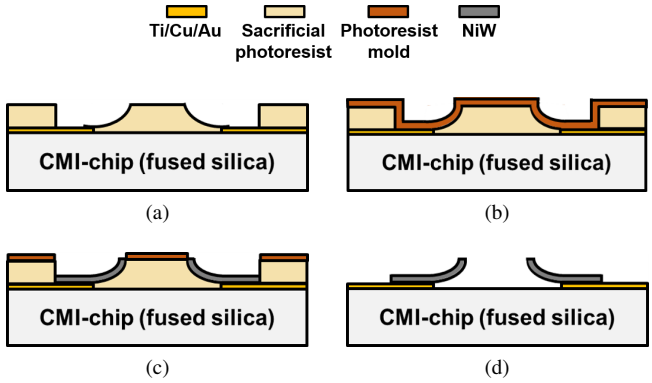
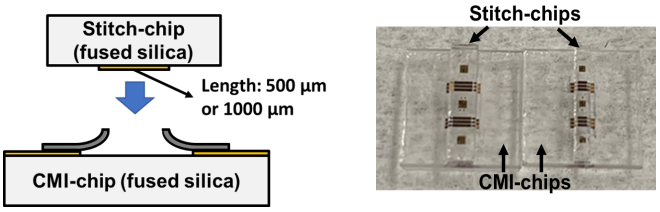


Fig. 4. CMI-chip fabrication process: (a) photoresist patterning after pad lift-off, (b) photoresist spray coating after seed layer sputtering, (c) photoresist molding and electroplating, and (d) CMI releasing



(a) (b)

Fig. 5. Assembly: (a) flip-chip bonding of the stitch-chip and the CMI-chip and (b) samples after assembly

electroless gold plating is performed to cover all conductive surfaces.

The stitch-chip and the CMI-chip are assembled using a flip-chip bonder (Finetech FINEPLACER lambda) and secured by epoxy at the edges of the chips (for demonstration purposes), as shown in Fig. 5. In Fig. 5a, a stitch-chip with 500 μm-long CPWs and a stitch-chip with 1000 μm-long CPWs are assembled and the resulting assembled testbeds are denoted as L-sample and 2L-sample, respectively. Fig. 5b shows these testbeds ready for RF measurements using a probe station.

IV. Characterization and Discussion

RF measurements up to 30 GHz were performed by Cascade Microtech 200 μm-pitch G-S-G |Z| probes and a Keysight N5245A PNA-X network analyzer, which is located in a Faraday cage. Short-open-load-thru (SOLT) calibration was used with Cascade Microtech CSR-8 calibration substrate before RF measurements of the testbeds. Next, L-sample, 2L-sample, and thru-pads structures were measured.

A. *Stitch-Chip Link after Removing Pads*

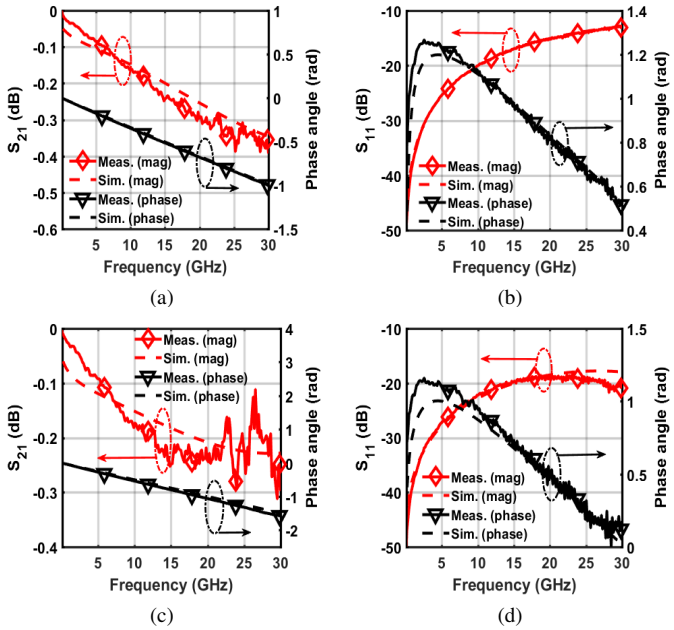


Fig. 6. Measured S-parameters of stitch-chip links (after removing probing pads, i.e. CPWs with CMIs at both ends): (a) insertion loss of 500 μm-long stitch-chip link, (b) return loss of 500 μm-long stitch-chip link, (c) insertion loss of 1000 μm-long stitch-chip link, and (d) return loss of 1000 μm-long stitch-chip link

Table 1. Comparison of signal links in silicon interposer and in this work.

Technology	Link length/wire pitch	Interconnect type/height	Insertion loss at 28 GHz
Silicon interposer	1 mm/200 μm	Solder bumps/30 μm	-3.78 dB
This work	1 mm/200 μm	CMIs/30 μm	-0.2 dB

Fig. 6 shows the S-parameters of the two different stitch-chip links (i.e. CPWs with CMIs on both ends) following the de-embedding of the probing pads using (1) to (3). As shown in Fig. 6, the measurement results are in good agreement with simulations. In Fig. 6c, the low-loss sample is observed to be susceptible to background noise at high frequencies. The data clearly suggests that the stitch-chip links provide ultra low-loss signal interfaces. The stitch-chip link with 500 μm-long CPW is measured to have less than 0.4 dB insertion loss up to 30 GHz.

To benchmark the stitching technology to silicon interposer technology, CPWs of similar characteristic impedance (50 Ω) are designed and simulated for silicon interposer firstly. Standard silicon (10 S/m conductivity) with 1 μm-thick silicon dioxide is selected as substrate material. Solder bumps, instead of CMIs, are implemented as off-chip interconnects at the ends of the CPWs. Table 1 shows the comparison between the silicon interposer links (i.e. CPWs with solder bumps on both ends) and the stitch-chip links in this work for 5G applications operated at 28 GHz.

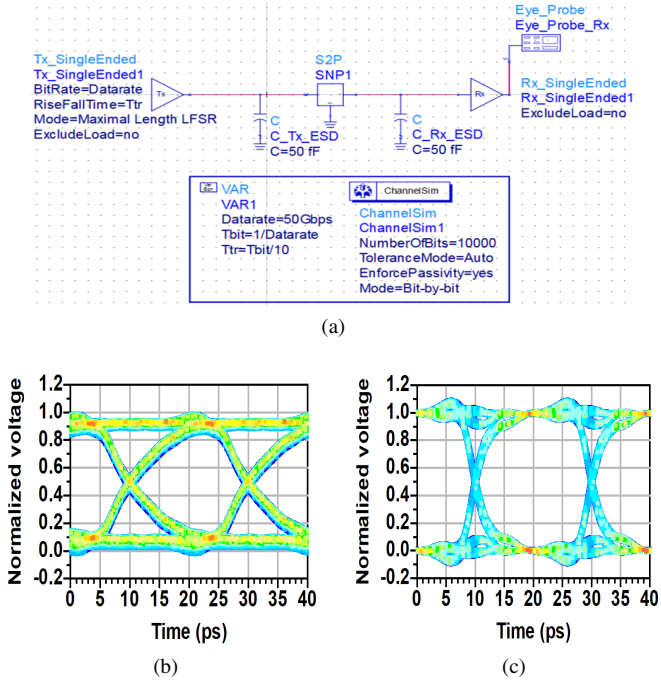
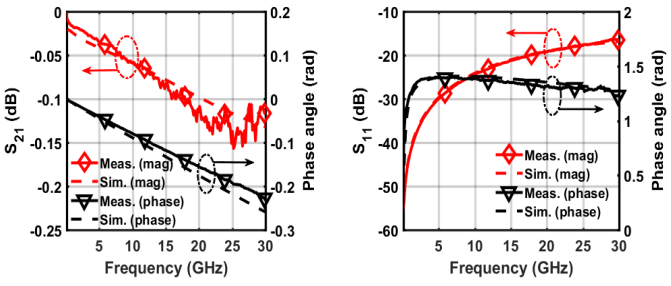


Fig. 7. Eye diagram simulation: (a) ADS simulation schematic, (b) silicon interposer link with 50 fF ESD capacitors at 50 Gbps data rate, and (c) stitch-chip link (this work) with 50 fF ESD capacitors at 50 Gbps data rate

For the digital back-end, in order to evaluate the SI performance, the S-parameters of these two types of signal links are imported into Keysight Advanced Design System (ADS) to perform eye diagram simulations, as shown in Fig. 7a. Using channel simulation function, a PRBS-11 data pattern is injected at the input, and rise/fall time is assumed as 10% of the unit interval (UI). An eye-probe is connected at the output to obtain eye diagram. The first case is a silicon interposer link with assumed 50 fF electrostatic discharge (ESD) capacitors at the input and output. The other case is a stitch-chip link with same ESD capacitors. Note that circuit jitter and crosstalk are not considered into these case studies.

Comparing the results from Fig. 7b and Fig. 7c, the stitch-chip link improves eye height by 49.4% because of the ultra low-loss signal propagation through the stitch-chip link. In addition, the stitch-chip link's shorter rise/fall time (∼3.3 ps vs. ∼8.3 ps for the silicon interposer link) implies lower signal latency and link parasitics. As shown in Fig. 7c, the eye diagram with 50 fF ESD capacitors has a clear opening (eye height: 94.1% of logic 1 voltage, eye width: 96.7% of UI) at 50 Gbps. Also note that this performance is achieved without any equalization, which can simplify transceiver circuit design in digital chiplets.

B. L-2L De-Embedding for CMI



(a) (b)

Fig. 8. CMI S-parameters after L-2L de-embedding: (a) insertion loss and (b) return loss

This paper, for the first time, reports the measured S-parameters of G-S-G CMIs using L-2L de-embedding. Fig. 8a and Fig. 8b show the S-parameters of G-S-G CMIs extracted from the testbeds using (1) to (6). The magnitude and the phase angle of the measured insertion loss and return loss are close to simulations (<10% differences). These mismatches may result from the measurement noise and the process variations of the samples. Because of the low return loss (-16.4 dB at 30 GHz), CMIs are electrically short within this frequency range and thus, their impedance discontinuities are difficult to observe. They are also low-loss (∼0.17 dB) structures up to 30 GHz. Solder bumps with 150 μm-pitch and 30 μm-height are reported to have less than 0.3 dB loss up to 30 GHz [10]. While maintaining similar loss, CMIs overcome solder bumps' shortcomings such as IMC formation, shorting as pitch scaling, and enable simple rework.

V. Conclusion

In this paper, modeling, fabrication, assembly, and characterization are performed on a polylithic testbed, which emulates a fully assembled stitch-chip system for RF/mm-wave applications. The measurements suggest that the stitch-chip links provide ultra low-loss signal interfaces. A 500 μm-long stitch-chip link provides less than 0.4 dB insertion loss up to 30 GHz. Moreover, for 5G applications operated at 28 GHz, a 1000 μm-long stitch-chip link has a lower loss (0.2 dB) compared to a similar link on a silicon interposer (3.78 dB). For the SI performance of a digital back-end, the stitch-chip link is superior to silicon interposer technologies as data shows 49.4% improvement in eye height and a clear eye-opening at 50 Gbps. Using an L-2L de-embedding method, the S-parameters of CMIs are extracted for the first time and show less than 0.17 dB insertion loss up to 30 GHz.

Acknowledgment

This work was performed in part at the Georgia Tech Institute for Electronics and Nanotechnology, a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (ECCS-1542174). This work was funded by the National Science Foundation Grant 1810081.

References

[1] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[2] K. K. Samanta, "Pushing the envelope for heterogeneity: multilayer and 3-D heterogeneous integrations for next generation millimeter- and submillimeter-wave circuits and systems," *IEEE Microw. Mag.*, vol. 18, no. 2, pp. 28–43, Mar. 2017.

[3] I. Ndip and K. Lang, "Roles and requirements of electronic packaging in 5G," in *Proc. 7th Electronic System-Integration Technology Conference (ESTC)*, Dresden, Germany, Sep. 2018, pp. 1–5.

[4] S. Shinjo, K. Nakatani, K. Tsutsumi, and H. Nakamizo, "Integrating the front end: a highly integrated RF front end for high-SHF wide-band massive MIMO in 5G," *IEEE Microw. Mag.*, vol. 18, no. 5, pp. 31–40, Jul. 2017.

[5] P. K. Jo, M. Zia, J. L. Gonzalez, H. Oh, and M. S. Bakir, "Design, fabrication, and characterization of dense compressible microinterconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 7, pp. 1003–1010, Jul. 2017.

[6] C. Zhan, C. Chuang, J. Juang, S. Lu, and T. Chang, "Assembly and reliability characterization of 3D chip stacking with 30μm pitch lead-free solder micro bump interconnection," in *Proc. 60th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, Jun. 2010, pp. 1043–1049.

[7] C. Zhang, H. S. Yang, and M. S. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632–1639, Oct. 2013.

[8] H. Yen, T. Yeh, and S. Liu, "A physical de-embedding method for silicon-based device applications," *PIERS online*, vol. 5, no. 4, pp. 301–305, 2009.

[9] H. Yen, Y. Lin, C. Hu, S. B. Jan, C. Hsieh, M. F. Chen, C. Kuo, H. Chen, and M. Jeng, "TSV RF de-embedding method and modeling for 3DIC," in *Proc. SEMI Advanced Semiconductor Manufacturing Conference*, Saratoga Springs, NY, May 2012, pp. 394–397.

[10] K. B. Unchwaniwala and M. F. Caggiano, "Electrical analysis of IC packaging with emphasis on different ball grid array packages," in *Proc. 51st Electronic Components and Technology Conference (ECTC)*, Orlando, FL, May 2001, pp. 1496–1501.