Integrated Self-Adaptive and Power-Scalable Wideband Interference Cancellation for Full-Duplex MIMO Wireless

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***Abstract*— A wideband analog/RF interference cancellation technique that is able to autonomously adapt itself to time-varying interference channels and to scale its dc power based on the number of multiple-input–multiple-output (MIMO) array elements is presented. Least-mean square (LMS) adaptive circuitry is co-designed with and partially embedded in a wideband RF/analog interference canceller and a gain-boosted mixer-first receiver (RX), significantly reducing the system complexity and dc power while achieving rapid (microsecond-scale) adaptation. In addition, the proposed canceller is able to digitally adjust its transconductance and coupling strength at the RX side, essentially trading its dc power with the element-level RX noise figure (NF). At the array level, the NF can be lowered by averaging uncorrelated noise across elements. A prototype 0.5-to-2.5-GHz full-duplex (FD) MIMO RX is designed and fabricated using a 65-nm CMOS process. With the adaptive circuitry fully integrated and consuming 14 mW, the cancellers adapt themselves to an unknown channel in 1 μs, providing >20-dB RF/analog interference cancellation across 20-MHz bandwidth (BW) with antenna voltage-standing-wave ratio (VSWR) up to 2:1. Simultaneous self- and cross-interference cancellation in our FD MIMO RX is also demonstrated using the integrated adaptation circuitry, achieving 24-dB overall interference cancellation across 20-MHz BW. The FD MIMO RX with self- and cross-interference cancellation is power-scalable—the NF-power scalability of the FD RX enables a nearly constant canceller dc power per element, despite a quadratic increase of cancellers.**

***Index Terms*— Adaptive filter, beamforming, CMOS, full duplex (FD), least-mean squares (LMSs), multiple-input–multiple-output (MIMO), self-interference (SI), interference cancellation.**

I. Introduction

RECENT advances in self-interference cancellation (SIC) technologies have demonstrated the feasibility of attaining high levels of cancellation, paving the way toward in-band full-duplex (FD) wireless that holds the potential to boost RF spectrum efficiency and to open up new possibilities beyond the physical layer [1]–[5].

Integrated FD radios with large amounts of SIC across wide signal bandwidths (BWs) have been demonstrated (see [6]–[13]). However, maintaining such SIC in dynamic wireless environments remains challenging [5], [14]. A time-varying wireless channel requires SIC to be reconfigured every 60 ms in moderate mobile environments (e.g., Wi-Fi hotspots) [15]. During the SIC adaptation, the desired signals cannot be received, and hence, how quickly SIC can tune itself is an important metric.

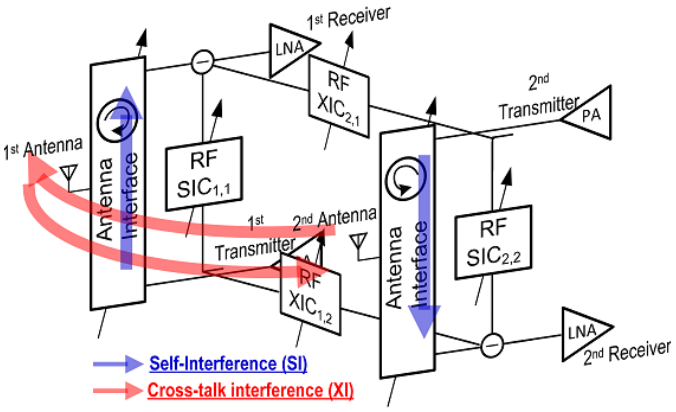

Fig. 1. SI and XI in a 2 × 2 FD MIMO radio.

Extending the existing SIC technologies to multiple-input–multiple-output (MIMO), FD radios has been demonstrated using off-the-shelf components (e.g., [15]) and has only recently been integrated on chip [16], [17]. The main challenge associated with FD MIMO radios is simultaneous SI and crosstalk-interference (XI) suppression. An MIMO FD radio creates XI due to the coupling among antennas in addition to self-interference (SI), as shown in Fig. 1. In a 2 × 2 FD MIMO radio shown in Fig. 1, two RF/analog SI cancellers ($SIC_{1,1}$ and $SIC_{2,2}$) and two XI cancellers ($XIC_{2,1}$ and $XIC_{1,2}$) are required for interference suppression. In general, an $N \times N$ FD MIMO radio requires N SI cancellers ($SIC_{k,k}$, $k = 1, \ldots, N$) and $N(N-1)$ XI cancellers ($XIC_{k,i}$, $k = 1, \ldots, N, i = 1, \ldots, N, k \neq i$). Therefore, the number of cancellers in an MIMO FD radio increases quadratically with the number of elements, resulting in formidable challenges associated with canceller adaptation, complexity, and power consumption.

In [17], we reported an integrated least-mean square (LMS) adaptive wideband RF/analog SIC for FD wireless. In contrast to the prior FD LMS adaptive RF SIC works (see [18]), the LMS adaptive circuitry is co-designed with and partially embedded in a wideband RF/analog SIC and a gain-boosted

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mixer-first receiver (RX). An N-path-filter-based down-converter is adopted at each canceller input and acts simultaneously as a delay generator, a Hilbert-transformer, and an LMS transmitter (TX)-side down-converter. Hilbert-transform-based SIC reduces the required number of canceller taps [13]. The transparency of the gain-boosted mixer-first RX is leveraged, allowing a single RX mixer to concurrently perform cancellation signal up-conversion, RX signal, and LMS RX-side down-conversion. This new RFIC-algorithm co-design method significantly reduces the adaptation overhead by minimizing the number of canceller taps and by fusing multiple functions into one circuit block. Enabled by the proposed self-adaptive SIC, a real-time CMOS FD 2×2 MIMO RX was reported in [17]. In addition to being self-adaptive, the FD MIMO RX is power-scalable. Each canceller can be reconfigured with lower dc power and stronger passive coupling to RX as the number of elements grows. While stronger coupling results in higher element-level noise, array-level noise can be reduced by averaging noise across elements [19].

In this article, we present the evolution of the self-adaptive RF/analog SIC proposed in [17], additional analyses and simulations of an interference-canceling gain-boosted mixer-first RX and a complex baseband (BB) LMS adaptation loop, and an in-depth discussion of the proposed FD MIMO power-scalable design. Also, circuit implementations and measurement details are presented. This article is organized as follows. The adaptation and low-power challenges associated with FD MIMO design are discussed in Section II. Section III describes the proposed FD MIMO self-adaptive and power-scalable wideband interference cancellation. The circuit implementation and measurements are presented in Sections IV and V, respectively. Section VI concludes this article.

II. Full-Duplex MIMO Design Challenges

The presence of XI and SI in an FD MIMO radio leads to a quadratic increase in analog/RF cancellers. In this section, we discuss the FD MIMO design challenges associated with real-time adaptation and energy-efficient canceller.

A. Real-Time Self-and-Cross-Interference Cancellation

While maintaining broadband and deep SIC in a changing electromagnetic (EM) environment remains challenging even for a single-in–single-out (SISO) FD radio [5], [20], dynamically adjusting many more SI and XI cancellers in an FD MIMO could be a formidable task.

Adaptive signal processing has been widely studied under the context of echo cancellation [21]. Using a mixed-signal architecture and a least-mean-square (LMS) algorithm, self-adaptive real-time echo cancellation has been demonstrated for Gigabit Ethernet on copper wire [22]. More recently, a similar mixed-signal SIC that uses a digital finite-impulse-response-filter-based canceller has been reported in [23] for wireless applications. Applying the LMS algorithm in this mixed-signal SIC architecture is relatively straightforward as the canceller internal states needed for the LMS algorithm are readily available in the digital domain. However, to suppress the TX distortion signals, this mixed-signal SIC approach requires a recreation of the nonlinearity characteristics of the entire TX chain [9]. Moreover, this approach is not able to cancel the noise from the TX [6], [7].

RF SIC that takes TX replica from PA output can suppress TX noise and nonlinear distortion and, hence, is adopted in many FD radios [6]–[8], [10]–[13]. Many existing real-time RF/analog SIC works adopt a gradient descent algorithm implemented in DSP (see [11], [24]). Gradient descent algorithms that do not access each canceller tap output or canceller internal state (e.g., the dithered linear search algorithm in [24]) have long adaptation times. Using power-hungry and sophisticated high-speed analog-to-digital converter (ADC) and DSP operating at 1 GHz, the SIC adaptation in [24] takes 500 μs, a large overhead in future highly dynamic wireless environments [15], to adapt its canceller weights.

With no RF canceller internal state access, an off-the-shelf-component-based FD radio in [15] demonstrates fast (24 μs) SIC adaptation based on the SI channel estimation in DSP. However, this algorithm relies on accurate knowledge of canceller S-parameters; it is hence questionable whether it can maintain microsecond-scale adaptation when applied to mass production using CMOS which is subject to process, voltage, and temperature variations, since canceller calibration is likely required in the field. Furthermore, this algorithm is standard dependent as it relies on Wi-Fi preamble for channel estimation [25].

FD self-adaptive RF SIC using LMS algorithms does not require canceller calibration, is agnostic to any air interface, and has shown fast adaptation in FD radios implemented using commercial off-the-shelf (COTS) components [3], [18], [26]. However, the LMS algorithm utilizes canceller internal states as mentioned earlier, and the prior works in [18] and [26] use many off-the-shelf down-converters to access the BB information at each RF canceller tap [see Fig. 1(b)]. Each LMS down-converter in [18] consumes 1.5-W dc power that is too high for battery-powered applications. In addition, these LMS down-converters would add significant complexity to FD MIMO systems [15]. Targeting at frequency-division duplexing (FDD) applications, a CMOS LMS adaptive RF SIC has been reported in [27] with 25-μs tuning time, but it has a narrow SIC BW due to the lack of on-chip delay generation and operates at a fixed frequency.

Table I summarizes the existing SIC adaptive control methods. Integrated analog/RF wideband SIC with efficient and frequency-agile adaptive control circuitry that is free of canceller calibration, agnostic to any air interface and exhibits microsecond-scale response time has not been reported yet.

B. Energy-Efficient Active Interference Cancellation in FD MIMO Radios

The majority of recently reported integrated FD radios adopts active analog/RF cancellation circuitry (see [10], [11], [17], [26], [28]) over its passive counterpart. This is because active cancellation circuitry has the advantages of being compact, flexible, and able to support low-to-moderate (15-to-25 dB) antenna interface isolation in many practical

TABLE I
SUMMARY OF EXISTING SELF-ADAPTIVE INTERFERENCE CANCELLATION METHODS

	Mixed-signal SIC with digital LMS [23]	RF/analog SIC with s-parameter-based digital optimization [1]	RF/analog SIC with pure DSP-based gradient descent adaptation [11], [24]	COTS RF/analog SIC with LMS [3],[18],[26]	CMOS RF/analog SIC with LMS [27]
Cancel PA noise and distortion?	NO	YES	YES	YES	YES
Agnostic to any air interface?	YES	NO	YES	YES	YES
Canceller calibration-free?	YES	NO	YES	YES	YES
Microsecond-scale adaptation?	YES	YES	NO	YES	YES
LMS down-converter-free?	YES	YES	YES	NO	YES
Wideband SIC?	YES	YES	YES	YES	NO
Adaptation circuitry frequency agile?	YES	YES	YES	YES	NO

scenarios [29]. The active interference canceller in an SISO FD RX is often energy efficient and consumes a dc power that is a fraction of the RX power. This is especially true if large isolation could be obtained from the antenna interface or the propagation domain [10], [11], [28].

In an MIMO FD radio, however, XI and SI cancellers dominate the system power consumption, especially with a large array size. The reason for this is twofold. First, the number of SI and XI cancellers grows quadratically with the number of antennas in an FD MIMO radio, making their power grows rapidly. Second, in an energy-efficient MIMO design that has been demonstrated in [19] and [30], the single-element RX power scales down with the array size and is approximately inversely proportional to the number of antennas.

Let us quantify the overall power consumption of an $N \times N$ FD MIMO radio that consists of RX power and canceller power as shown in the following equation:

$$\begin{aligned} P_{tot} &= N\left(P_{rx} + P_{rx,\mathrm{oh}}/M\right) + N^2\left(P_{cx} + P_{cx,\mathrm{oh}}/K\right) \\ &= \left(P_{rx,c} + P_{rx,\mathrm{oh}}\frac{N}{M}\right) + N^2\left(P_{cx} + P_{cx,\mathrm{oh}}/K\right). \quad (1) \end{aligned}$$

The RX power includes the power P_{rx} of a mixer, amplifiers, filters, and an ADC and the overhead power $P_{rx,\mathrm{oh}}$ from RX common blocks such as voltage regulators and frequency synthesizers that are shared among M array elements [30]. Similarly, the canceller power consists of the canceller amplifiers power P_{cx} and the overhead power $P_{cx,\mathrm{oh}}$ from canceller common blocks such as delay generators, voltage regulators, and frequency synthesizers that are shared among K cancellers. Let us assume that the RX is power-scalable, meaning that it can trade its noise figure (NF) for low power at the element level, while the array-level NF performance is preserved via averaging uncorrelated noise among elements [19]. Therefore, we can write $P_{rx} = P_{rx,c}/N$, where $P_{rx,c}$ can be approximated as a constant independent of the number of element N [19].

Assuming that $P_{rx,c} = 100$ mW, $P_{rx,\mathrm{oh}} = 40$ mW, $P_{cx} = 20$ mW, $P_{cx,\mathrm{oh}} = 10$ mW, and $M = K = 4$, the total FD MIMO RX power consumption is plotted based on (1) versus the number of array elements in Fig. 2. It can be seen that for an SISO FD (i.e., $N = 1$), the power consumption is dictated by the RX. However, as it moves to MIMO with $N \geq 2$, the canceller power quickly dominates. Therefore, energy-efficient SI-and-XI cancellers design is another unsolved challenge regarding FD MIMO radios.

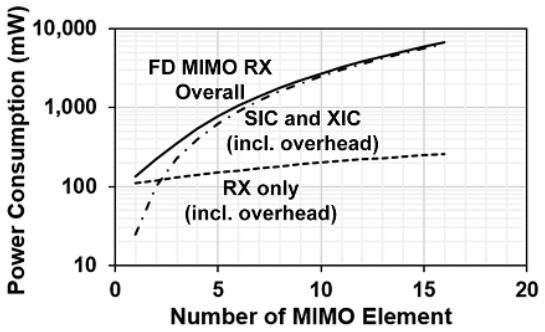


Fig. 2. SIC and XIC are projected to dominate FD MIMO RX power based on (1).

III. PROPOSED SELF-ADAPTIVE AND POWER-SCALABLE WIDEBAND INTERFERENCE CANCELLATION

Next, we describe our proposed techniques that address the two challenges mentioned in Section II.

A. Embedding LMS Down-Conversion in Wideband RF/Analog Interference Cancellation

Wideband SIC requires the generation of long delays inside the canceller [6]. Generating nanosecond-scale delay on chip requires bulky switched-capacitor circuits [6], [13]. Therefore, having fewer delay units allows compact on-chip canceller designs. In addition, each canceller tap needs one LMS adaptation loop, which includes TX- and RX-side down-converters, multipliers, and integrators [see Fig. 3(a)] [3], [18]. Reducing canceller taps, therefore, lowers the power and complexity overhead associated with the adaptation circuitry. In this work, a Hilbert-transform-based wideband RF SIC is utilized for fewer canceller taps given a fixed cancellation BW due to the introduction of complex (I/Q) canceller weights, as shown in Fig. 3(a) [3], [18]. An integrated Hilbert-transform-based wideband RF SIC has been reported recently in [13], but it uses exhaustive search to find the canceller weights, resulting in long adaptation time. In time domain, the Hilbert-transform or 90° phase shift has an impulse response of $h(t) = 1/(\pi t)$. When this response convolves with the RF delay, the canceller exhibits longer delay spread compared with that from a canceller without Hilbert-transform. This means that a fewer number of taps are needed, resulting in significantly less complexity and silicon area. For a more detailed discussion on the benefit of Hilbert-transform-based SIC, the readers are referred to [13].

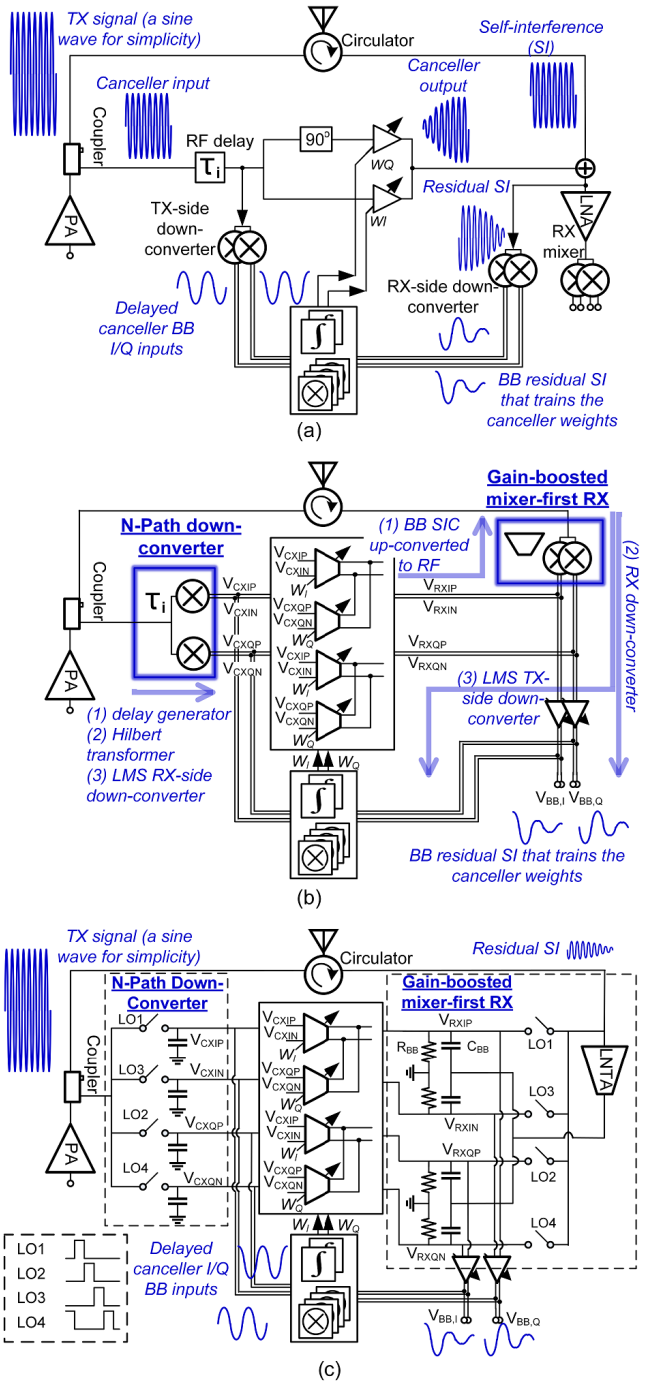


Fig. 3. Evolution of the proposed self-adaptive wideband RF/analog interference cancellation. (a) Self-adaptive Hilbert-transform-based wideband RF SIC reported in [3] and [18] using COTS components. (b) Proposed multi-functional blocks (an N-path down-converter and a gain-boosted mixer-first RX). (c) Details of the multi-functional blocks.

Nanosecond-scale RF delay for wideband SIC has been demonstrated on chip using N-path switched-capacitor circuits lately [6]. In this work, the down-conversion in the delay-generating N-path filter is repurposed to translate RF signals to analog BB for LMS self-adaptive operations. In addition, the I/Q down-converter in the N-path filter is essentially a Hilbert transformer with an LO-defined widely tunable operation frequency. Interestingly, a simple switched-capacitor

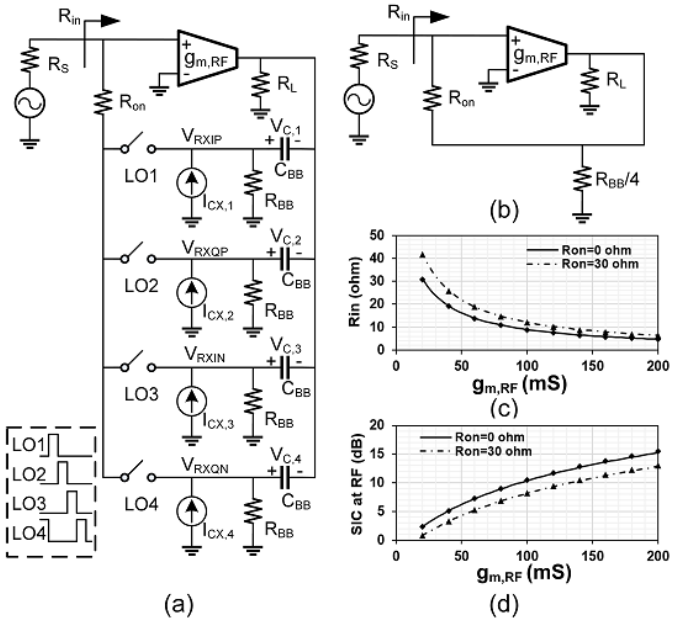


Fig. 4. Gain-boosted mixer-first RX with BB SIC. (a) Block diagram. (b) Equivalent circuit to calculate input impedance. (c) and (d) Simulation (lines) and calculation (markers) results at 1-GHz LO frequency using $R_S = 50\ \Omega$, $R_{BB} = 2\ \text{k}\Omega$, $R_L = 100\ \Omega$, and $C_{BB} = 10$ pF assuming perfect BB SIC.

N-path circuit, as shown in Fig. 3(b), simultaneously acts as a delay generator, a widely tunable Hilbert transformer, and an LMS TX-side down-converter.

In contrast to [6] and [13] where an up-conversion mixer is used in the canceller for SIC at RF, the BB cancellation signals in this work are directly injected at the RX BB, but the cancellation is transparent to RF by using a gain-boosted mixer-first RX. Furthermore, the mixer-first RX is repurposed as the LMS down-converter at the RX side. In essence, one passive mixer wrapping around an inverter-based low-noise transconductance amplifier (LNTA) [see Fig. 3(b)] replaces two mixers in [6] and [13]—one for the canceller up-conversion and one for RX down-conversion—while concurrently serves as the LMS RX-side down-converter. This is possible due to the transparency of the RX passive mixer, allowing it to act as a down-conversion and an up-conversion mixer at the same time.

BB SIC within the gain-boosted mixer-first RX is partially transparent to RF. This makes sense intuitively as the BB nodes [V_{RXIP}, V_{RXIN}, V_{RXQP}, and V_{RXQN} in Fig. 3(b) and (c)] and the RX input are shorted together when the switches are ON. A natural question that arises is that how much RF SIC can be obtained given perfect SIC (say $\geq$30 dB) at BB. A block diagram of a gain-boosted mixer-first RX with BB SIC is shown in Fig. 4(a) where all mixer switching transistors are modeled as ideal switches with their ON-resistance lumped into R_{ON}. Given an input signal at the LO frequency, the BB signals manifest themselves as different dc voltages across the BB capacitors. Assuming that the BB signals get suppressed perfectly upon BB SIC via the current-source cancellers, dc voltages across the BB capacitors become the same and all dc changes in the RX due to the input signal are negligible. Looking only at signals at the LO (input signal) frequency and

ignoring other harmonics, we arrive at an equivalent circuit shown in Fig. 4(b) where we have short-circuited all BB capacitors due to their low impedance at the LO frequency. Based on the memory-less equivalent circuit in Fig. 4(b), the input resistance and the resultant SIC at the RX input can be easily calculated as follows:

$$R_{\text{in}} = \left(\frac{1}{g_{m,\text{RF}}} \| R'_L\right) \cdot \left(1 + \frac{R_{\text{on}}}{R'_L}\right) \tag{2}$$

$$\text{SIC}_{\text{RF}} = \frac{R_{\text{in}}}{2(R_{\text{in}} + R_S)} \tag{3}$$

where $R'_L = R_L \| R_{\text{BB}}/4$. It should be noted that only the SI or XI, i.e., the signal that is correlated with cancellation signals $I_{\text{CX},i}$ $(i = 1, \ldots, 4)$ in Fig. 4(a), sees the input resistance R_{in} given in (2). For RX desired signal that is typically uncorrelated with the TX SI or XI, the RX input resistance is independent of BB SIC as the cancellation current sources have much larger impedance than RX BB resistance R_{BB} [see Fig. 4(a)], and can be written as (4) based on the derivation in [31], [32]

$$R_{\text{in,desired}} \approx \frac{\lambda R_{\text{BB}} + R'_L}{1 + g_{m,\text{RF}} R'_L} \| R_{sh} \tag{4}$$

where $\lambda = (\text{sinc}^2(\pi/4))/4$ and $R_{sh} = (\text{sinc}^2(\pi/4))/(1 - \text{sinc}^2(\pi/4))R_S$. In this work, $R_{\text{in,desired}}$ is designed to be around 50 Ω.

To verify the results given by (2) and (3), simulations at 1-GHz LO frequency using the circuit shown in Fig. 4(a) with $R_S = 50$ Ω, $R_{\text{BB}} = 2$ kΩ, $R_L = 100$ Ω, and $C_{\text{BB}} = 10$ pF have been conducted across different R_{on} and $g_{m,\text{RF}}$ values. As shown in Fig. 4(c) and (d), the simulated results match almost exactly with calculation. Large $g_{m,\text{RF}}$ and small R_{on} result in high SIC at RF but are at the expense of excessive parasitic capacitance and power consumption. Circuit design details are discussed in Section IV.

Finally, while a single-tap design supporting 20-MHz signal BW (see Section V) is adopted for each canceller in this work, our proposed self-adaptive wideband interference cancellation can be extended to a multi-tap design for even larger signal BW. One way to incorporate more canceller taps is to place multiple copies of the self-adaptive canceller in parallel with a splitting and a combining network at the TX and RX sides, respectively. The impedance looking into the multi-tap canceller from the TX and RX sides has to be preserved to prevent TX and RX performance degradation. This is similar to the multi-tap canceller design using COTS components reported in [3] and [18], essentially a time-domain equalizer using the Hilbert transform. In addition to the time-domain method, a frequency-domain-equalization-based multi-tap design has been published in [6] with an additional degree of freedom in canceller filter center frequency. A comparison between time- and frequency-domain canceller that both utilize N-path filters is of interest but beyond the scope of this article.

B. Design Considerations of a Complex BB LMS Loop

In contrast to the CMOS LMS adaptive narrowband RF SIC demonstrated in [27], in order to support broadband SIC in this work, an N-path down-converter is utilized for on-chip delay and I/Q generation. Furthermore, a frequency-translational analog/RF SIC is proposed so that the cancellation signals can be directly injected at the RX BB without additional up-conversion mixers used in [6] and [13] due to the transparency property of the RX passive mixer [33]. This results in a complex BB LMS adaptation loop in contrast to the real RF LMS loop in [27]. While a generalized LMS adaptation loop analysis (see [34]) with an arbitrary number of taps and using modulated (random) signals is involved and beyond the scope of this article, a relatively simple sine-wave-based analysis akin to that in [27] can be applied to a single-tap canceller to illustrate its operation principle and provides useful design guidelines. In contrast to an RF LMS loop analysis where the sine wave is at the RF carrier frequency [27], the sinusoid in our BB LMS analysis has a BB frequency of ω_s, which equals the symbol rate of the modulation waveform. Also, down-conversion of the TX RF signals to BB mitigates the stability issue in an RF LMS loop [27] as a given time delay generated by layout routing corresponds to a much smaller phase shift at BB than that at RF.

A block diagram of a complex BB LMS adaptation loop is shown in Fig. 5(a). For simplicity, we have removed the RF portions in Fig. 3(b). All connections in Fig. 5(a) are fully differential but shown using single-ended wires for simplicity. The adaptation loop internal nodes (in color blue) in Fig. 5 has been named consistently with those in Figs. 3, 4, 8, and 9. Assuming a sinusoidal TX signal and ignoring all the harmonics from the N-path down-converter, only BB canceller input signals $V_{\text{CXI}} = V_{\text{CX}}\cos(\omega_s t)$ and $V_{\text{CXQ}} = V_{\text{CX}}\sin(\omega_s t)$ are considered here. On the RX side, only fundamental components of SI are considered and modeled as current sources $I_{\text{RX},I}$ and $I_{\text{RX},Q}$ in Fig. 5(a). The in-band resistance looking into the frequency-translational mixer-first RX is modeled as R_{RX}. The canceller variable gain transconductance amplifiers (VGAs) are modeled as G_m. The RX BB output buffers have a voltage gain of A_V. Ideal unity gain multiplication operation is assumed for the LMS multiplier. Let us start with ideal integrators with unity gain frequency ω_{ugf} to derive the dynamic behavior of the complex BB LMS loop. The RX BB outputs can be calculated as

$$\begin{aligned} v_{\text{BB},I}(t) &= i_{\text{RX},I}(t) \cdot R_{\text{RX}} \cdot A_v \\ &\quad - \zeta\left[v_{\text{BB},I}(t) * \cos(\omega_s t) + v_{\text{BB},Q}(t) * \sin(\omega_s t)\right] \\ v_{\text{BB},Q}(t) &= i_{\text{RX},Q}(t) \cdot R_{\text{RX}} \cdot A_v \\ &\quad - \zeta\left[v_{\text{BB},Q}(t) * \cos(\omega_s t) + v_{\text{BB},I}(t) * \sin(\omega_s t)\right] \end{aligned} \tag{5}$$

where $\zeta = \omega_{\text{ugf}} R_{\text{RX}} A_v G_m V_{\text{CX}}^2$ and V_{CX} is the amplitude of the canceller N-path down-converter fundamental outputs. Applying Laplace transform to (5), the sum and difference transfer functions can be found approximately if $\omega_s \gg \zeta$ as

$$\frac{Y_S(s)}{X_S(s)} \approx \frac{Y_D(s)}{X_D(s)} \approx R_{\text{RX}} A_v \frac{s^2 + \omega_s^2}{s^2 + \zeta s + \omega_s^2} \tag{6}$$

where $Y_{S/D}(s) = V_{\text{BB},I}(s) \pm V_{\text{BB},Q}(s)$ and $X_{S/D}(s) = I_{\text{RX},I}(s) \pm I_{\text{RX},Q}(s)$. Assuming a sinusoidal TX signal and

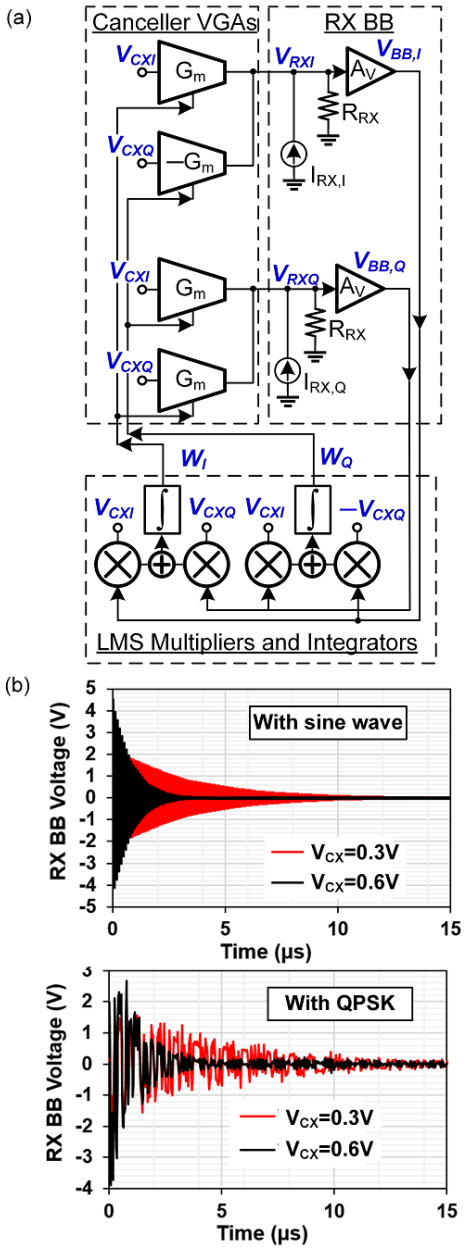


Fig. 5. Complex BB LMS adaptation loop. (a) Block diagram with RF portions in Fig. 3(b) removed for simplicity. (b) Simulated RX BB outputs with adaptive SIC starting at $t = 0$ s using the complete circuit in Fig. 3(c)—$R_S = 50\ \Omega$, $R_{ON} = 5\ \Omega$, $R_{BB} = 2$ kΩ, $C_{BB} = 10$ pF, RX LNTA $g_{m,RF} = 100$ mS, $R_L = 100\ \Omega$, RX BB gain $A_v = 2$, canceller VGA gain $G_m = 20$ mS, unity gain LMS multipliers, and integrators with $\omega_{ugf} = 314$k rad/s.

$\omega_s \gg \zeta$, the time-domain RX BB signals can be expressed as

$$v_{BB,I}(t) = R_{RX}A_v i_{RX,I}(t)\cdot e^{-\zeta t}$$
$$v_{BB,Q}(t) = R_{RX}A_v i_{RX,Q}(t)\cdot e^{-\zeta t}. \quad (7)$$

Since the SI decays exponentially as shown in (7), the settling time for reaching a given cancellation SIC can be calculated as

$$t_{settle} = \frac{\text{SIC}}{20\log_{10}(e)\zeta} \quad (8)$$

where we have assume that the canceller VGA gain controls have infinitely high resolution, and ζ is the unity-gain frequency of the entire adaptation loop. Since an ideal integrator is assumed, the dc loop gain is infinitely large, resulting in perfect SIC at $t \to \infty$ as indicated by (7). In practice, several factors limit the attainable SIC and are discussed later in this Section. It can be seen from (8), a rapid microsecond-scale settling response could be obtained via a large loop gain ζ. In order to adjust the loop gain and hence the adaptation time on-the-fly based on the symbol rate, the gain A_V of RX BB amplifiers (see Fig. 5) is made digitally programmable in this work.

Simulations using both a 10-MHz sinusoidal and a 10-MSymbol/s QPSK signals are utilized to validate the analytical results given by (7) and (8). Note that in our simulation, the complete circuit in Fig. 3(c) is used, which includes the mixer-first RX and the N-path canceller down-converter. The antenna interface is modeled by a single 5-ns delay with 26-dB isolation. Using $R_S = 50\ \Omega$, $R_{ON} = 5\ \Omega$, $R_{BB} = 2$ kΩ, $C_{BB} = 10$ pF, RX LNTA $g_{m,RF} = 100$ mS, $R_L = 100\ \Omega$, RX BB gain $A_v = 2$, canceller VGA gain $G_m = 20$ mS, and unity gain LMS multipliers and integrators with $\omega_{ugf} = 314$k rad/s, Fig. 5(b) shows our simulated RX BB outputs with self-adaptive SIC across a couple of TX power levels. Using the sine wave, the simulated 20-dB SIC settling time is 2 and 8 μs when V_{CX} is 0.6 and 0.3 V, respectively. The calculated settling time using (8) is 1.4 and 6.4 μs; the small error is likely due to the harmonic responses from the mixer-first RX and the canceller N-path down-converter that are excluded from the analysis. Using the 10-MSymbol/s QPSK signals, the settling behavior is almost identical to that when the sinusoidal signal is used. Also, it can be seen that the residual 10-MHz QPSK SI is stronger than that of a sinusoid SI. This is as expected as it is more difficult for a canceller to emulate the interference channel across a 10-MHz signal BW than at a single frequency.

From (8), a large unity-gain frequency ω_{ugf} results in fast settling. However, if the unity-gain frequency is too high (comparable or higher than the symbol rate), the loop will track the individual symbols, resulting in undesired ripples on the weights and a lower bound on the achievable overall SIC [34], [35]. To minimize the ripples and the lower bound on the overall SIC, the unity-gain frequency needs to be much less than the symbol rate. In this way, the LMS loop treats the TX signal as a stationary process to assess the overall loop performance [34]. In our design, the unity-gain frequency of the integrator is designed to be less than 10% of the symbol rate.

In practice, analog integrators often have a finite dc gain. Assuming that an analog integrator can be modeled as a first-order low-pass filter with its dc gain of G_{dc}, 3-dB BW of ω_p, and unity gain frequency of $\omega_{ugf} = G_{dc}\omega_p$, the sum and difference transfer functions can be rewritten as

$$\frac{Y_S(s)}{X_S(s)} \approx \frac{Y_D(s)}{X_D(s)} \approx R_{RX}A_v \frac{(s+\omega_p)^2+\omega_s^2}{(s+\omega_p)^2+\zeta(s+\omega_p)+\omega_s^2} \quad (9)$$

where $\zeta = \omega_{ugf}R_{RX}A_v G_m V_{CX}^2$. Assuming $\omega_s \gg \omega_p$ and $\zeta \gg \omega_p$, SIC can be calculated as [27]

$$\text{SIC}^{-1} = \left|\frac{Y_S(j\omega_s)}{X_S(j\omega_s)}\right| \frac{1}{R_{RX}A_v} \approx \frac{2}{G_{dc}R_{RX}A_v G_m V_{CX}^2}. \quad (10)$$

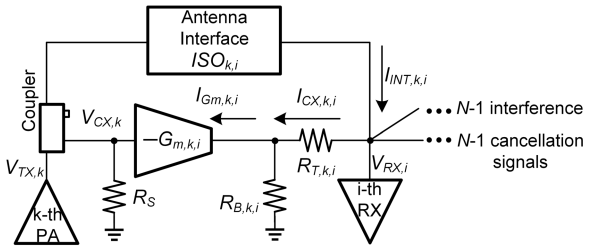


Fig. 6. $N \times N$ FD MIMO NF analysis at the ith ($1 < i < N$) RX element.

Based on (10), a dc gain of 33 dB is required for 30-dB SIC given $R_{\mathrm{RX}} = 100\ \Omega$, $A_V = 2$, $G_m = 20$ mS, and $V_{\mathrm{CX}} = 0.6$ V. LMS loop dynamic simulations using low-pass-filter-based integrator with a dc gain of 40 dB and 3-dB BW of $f_p =$ 1k Hz are examined and show similar results to that in Fig. 5 using ideal integrators. In addition to adaptation loop gain, there are other factors that limit the overall achievable SIC, including the resolution of canceller gain/phase shift/delay controls [7], the interference channel frequency selectivity or delay spread [6], and the adaptation loop multiplier and integrator dc offset [27]. Simulation-based optimization is needed to balance the impact of various factors.

To mitigate the impact of the multiplier and integrator dc offsets on SIC, the first multiplier is designed as a passive mixer where the reference signals drive the mixer switches. In this way, the dc offsets of the first multiplier itself get up-converted. Also, the first multiplier is designed to have a high gain to suppress the following stage offsets [27], [35]. More circuit design details are discussed in Section I-V.

C. Power-Scalable MIMO Interference Cancellation

In an $N \times N$ MIMO RX, the single-element NF is independent of array size N, and array-level noise averaging has been utilized for an energy-efficient power-scalable MIMO RX design [19]. In an FD MIMO, however, the number of XIC cancellers is proportional to N, resulting in an array-size-dependent single-element NF. Despite a degraded N-dependent single-element NF, we find that it is possible to reduce XIC and SIC cancellers power consumption via array-level noise averaging together with programmable canceller coupling strength. This can be accomplished due to the fact that FD MIMO single-element NF increases much slower compared with array-level noise averaging. Quantitative analyses are presented next in this section.

A block diagram for an $N \times N$ FD MIMO NF analysis at the ith ($1 < i < N$) RX element is shown in Fig. 6. While N SIC and XIC cancellers are needed for the RX, only one canceller tapping from the kth TX is considered for simplicity as we have assumed that all N cancellers have identical architecture as shown in Fig. 6 and have uncorrelated noise among themselves. Each canceller is modeled as an input matching resistor R_S and a transconductance amplifier $G_{m,k,i}$, taps from the coupling port of a TX-side coupler at the PA output, and injects the cancellation current at the RX input. The two resistors $R_{T,k,i}$ and $R_{B,k,i}$ at the transconductance amplifier output act as an RX-side coupler operated in the current domain. The sum of their resistance $R_{T,k,i} + R_{B,k,i}$ is kept as a constant and is much larger than R_S. In this way, the loading effect of $R_{T,k,i}$ and $R_{B,k,i}$ at the RX side is negligible and independent of the coupling setting. The canceller delay generation and phase shift operations are ignored in noise analysis for simplicity. Assuming cancellation at RF, i.e., $I_{\mathrm{INT},k,i}$=$I_{\mathrm{CX},k,i}$ and hence $V_{\mathrm{RX},i}$ is a virtual ground for the interference, it can be shown that the required canceller transconductance is

$$G_{m,k,i} = \frac{V_{\mathrm{TX},k}}{V_{\mathrm{CX},k}} \cdot \frac{I_{Gm,k,i}}{I_{\mathrm{CX},k,i}} \cdot \frac{2}{R_S \cdot \mathrm{ISO}_{k,i}} = \frac{2C_{\mathrm{TX}} \cdot C_{\mathrm{RX},k,i}}{R_S \cdot \mathrm{ISO}_{k,i}} \quad (11)$$

where $C_{\mathrm{RX},k,i} = I_{Gm,k,i}/I_{\mathrm{CX},k,i} = 1 + R_{T,k,i}/R_{B,k,i}$ is coupling strength at the RX side and $\mathrm{ISO}_{k,i} = 2V_{\mathrm{TX},k}/I_{\mathrm{INT},k,i} \cdot R_S$ is the antenna interface isolation, and we have assumed that the source resistance R_S and TX-side coupling $C_{\mathrm{TX}} = V_{\mathrm{TX},k}/V_{\mathrm{CX},k}$ are the same across all cancellers.

The RX input-referred kth canceller NF contribution in linear scale can be calculated as

$$F_{\mathrm{CX},k,i} = \left(\frac{\gamma}{G_{m,k,i} \cdot R_S} + 1\right)\left(\frac{2C_{\mathrm{TX}}}{\mathrm{ISO}_{k,i}}\right)^2 \quad (12)$$

where we have assumed that canceller transconductance output current noise power spectral density is modeled as $4kT\gamma\, G_{m,k,i}$/Hz. From (12), a larger $G_{m,k,i}$ value results in a smaller noise penalty as the amplifier output current increases with $G_{m,k,i}$, while output noise current is proportional to $(G_{m,k,i})^{1/2}$. The final cancellation current can be kept unchanged by increasing $C_{\mathrm{RX},k,i}$ or using a weaker RX-side coupling as in (11). This NF-power tradeoff is demonstrated in our measurement detailed in Section V.

Finally, the overall ith RX NF, at the array level and in the presence of N cancellers, can be written a:

$$\begin{aligned} F_{\mathrm{array},i} &= \frac{F_{\mathrm{RX}}}{N} + \frac{1}{N}\sum_{k=1}^{N} F_{\mathrm{CX},k,i} \\ &= F_{\mathrm{RX},C} + \frac{1}{N}\sum_{k=1}^{N}\left(\frac{2C_{\mathrm{TX}}}{\mathrm{ISO}_{k,i}}\right)^2 + \frac{1}{N}\sum_{k=1}^{N}\frac{2\gamma\, C_{\mathrm{TX}}}{C_{\mathrm{RX},k,i} \cdot \mathrm{ISO}_{k,i}} \\ &= F_{\mathrm{RX},C} + \frac{4C_{\mathrm{TX}}^2}{\mathrm{ISO}_{\mathrm{avg},i}^2} + \frac{1}{N}\sum_{k=1}^{N}\frac{2\gamma\, C_{\mathrm{TX}}}{C_{\mathrm{RX},k,i} \cdot \mathrm{ISO}_{k,i}} \end{aligned} \quad (13)$$

where we have made two assumptions: 1) the RX NF F_{RX} is scalable and is a constant $F_{\mathrm{RX},C}$ independent of array size as demonstrated in [19] and 2) the MIMO RX operates in a digital phased-array beamforming mode so that the single-element NF is reduced by N at the array level. In (13), we have defined an average antenna interface isolation for the ith RX as $\mathrm{ISO}_{\mathrm{avg},i}^2 = 1/1/N\sum_{k=1}^{N} ISO_{k,i}^{-2}$.

Interestingly, it has been shown that $\mathrm{ISO}_{\mathrm{avg},i}^2$ increases with the array size N in an FD MIMO RX [36]. Based on the array antenna crosstalk measurements in [36] and assuming an SI isolation of 25 dB, the average antenna interface isolation increases from 18 dB when $N = 2$ to 24 dB when $N = 8$. Intuitively, a larger array has more separated antennas, leading to a higher isolation on average.

From (13), an increasing $\mathrm{ISO}_{\mathrm{avg},i}^2$ value results in a lower array-level NF. This can be leveraged for reducing cancellers dc power via adjusting the RX-side coupling $C_{\mathrm{RX},k,i}$ without

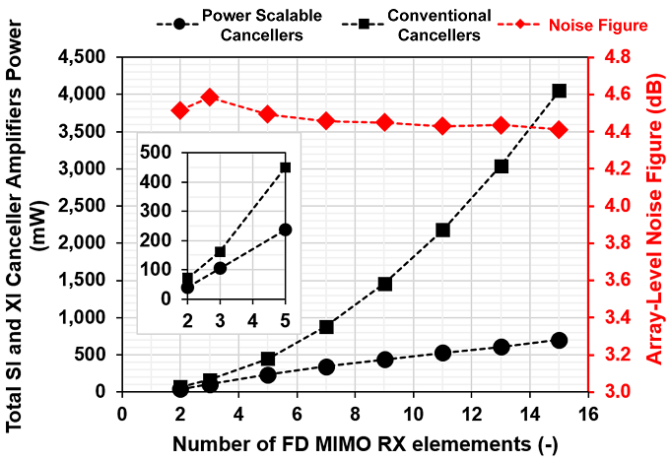


Fig. 7. Calculated FD MIMO canceller amplifier power consumption and array-level NF based on (11) and (13).

array-level NF penalty. Setting $C_{\mathrm{RX},k,i} \cdot \mathrm{ISO}_{k,i}$ to be a constant given an array size N and assuming an SI isolation of 25 dB, XI isolation of 20 dB for the first adjacent antennas, and 4 dB more XI isolation for the next adjacent antennas, RX-side coupling setting $C_{\mathrm{RX},k,i}$ can be calculated, given $NF_{\mathrm{RX},C} = 3$ dB, $C_{\mathrm{TX}} = 3.16$, $\gamma = 9$, and a constant about 1.5 dB array-level NF degradation based on (13). Using (11) and assuming a transconductance efficiency of 10 mS/mA from a 1.2-V supply voltage, we plot the power consumption of all cancellers in Fig. 7 together with the calculated array-level NF using (13). It is observed that the array-level NF remains almost constant, while the total power consumption is significantly reduced compared with a quadratically increased power. A comparison of FD MIMO array-level NF in measurement and using (13) is presented in Section V.

The power consumption benefit of the proposed design is limited by the canceller common blocks mentioned in Section-II as their dc power still grows quadratically. Assuming a common block consuming 20 mW sharing among every four cancellers, the total common blocks dissipate more power compared with the canceller amplifiers when $N \geq 12$, limiting the amount of energy-efficiency enhancement.

In this work, both the canceller VGA transconductance and the RX-side coupling strength are made digitally programmable (see Figs. 8 and 9). The VGA transconductance is configured by turning on and off VGA unit cells (see Fig. 9), and the RX-side coupling is adjusted by using current-splitting resistors R_T and R_B at the RX BB (see Fig. 8). In addition, on-the-fly reconfiguration of SIC and XIC power consumption and, consequently, the RX element-level NF is desirable as MIMO signal processing methods (e.g., maximum ratio and zero forcing) have different array-level signal-to-noise (SNR) performance [37].

IV. Circuit Implementation

Fig. 8 shows the block diagram and schematic of the proposed 2×2 FD MIMO RX implemented in 65-nm CMOS. There are four cancellers to suppress SI and XI. Each canceller consists of an N-path filter, BB VGAs, and VGA weights

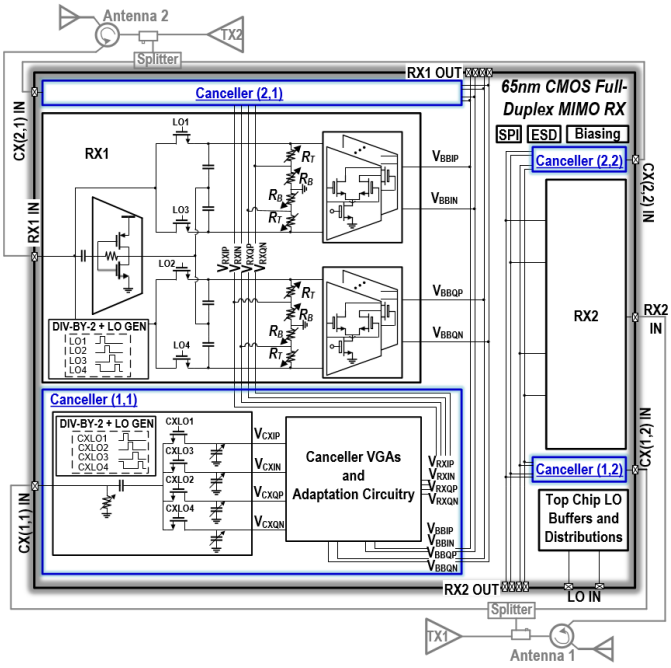


Fig. 8. Block diagram and schematic of the proposed 2×2 FD MIMO RX implemented in a 65-nm CMOS technology. The canceller VGA and adaptation circuitry diagram and schematic are shown in Figs. 5 and 9.

adaptation circuitry. The cancellation currents are injected at the BB nodes of a gain-boosted mixer-first RX via current-splitting-based RX-side couplers (R_B and R_T in Fig. 8).

The RF transconductance of the mixer-first RX is designed to be 100 mS, which is a tradeoff among RX NF, SIC at RF, operation frequency, and power consumption. A larger RF transconductance would result in more SIC at RF as shown in Section II-A at the expense of power consumption, operation frequency, and RX NF. A channel length of 85 nm is chosen for RF transconductance transistors in order to obtain a large intrinsic gain and RF SIC. The switching transistors of the passive mixer have ON-resistance of 10 Ω.

The cancellation signal coming from the TX is first down-converted by a four-phase N-path filter, as illustrated in Fig. 8. Via four switched-capacitor banks, the N-path filter is designed to have a digitally programmable RF-to-BB delay range from 0.3 to 10 ns. This on-chip delay generation allows broadband SIC, as discussed in [6]. The canceller BB VGAs are split into eight digitally controlled unit cells (see Fig. 9) for MIMO power-NF scalability, as detailed in Section III. BB VGAs dominate the canceller linearity performance, and hence, a 2.5-V power supply is used together with thick oxide transistors for weight inputs and PMOS loads. Resistive source degeneration further enhances the VGA linearity. The source degeneration of the PMOS loads results in a relatively large effective noise factor γ as used in (12) and Fig. 6. A complimentary design would further reduce its noise.

The self-adaptive circuitry includes analog multipliers (see Fig. 9) and integrators (see Fig. 9). To reduce the dc offsets of the adaptation circuitry, the analog multiplier is designed with a large gain and is implemented as a chopper where the reference data drive a passive mixer. As shown in Fig. 9,

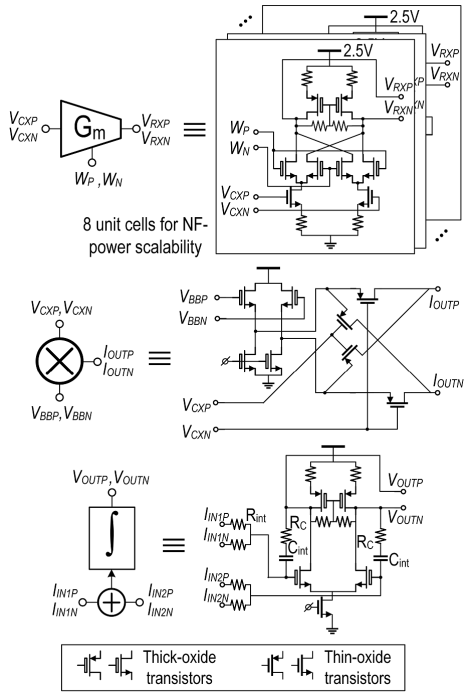


Fig. 9. Schematic of cancellation adaptation circuitry shown in Fig. 5: canceller VGA (top), multiplier (middle), and integrator (bottom).

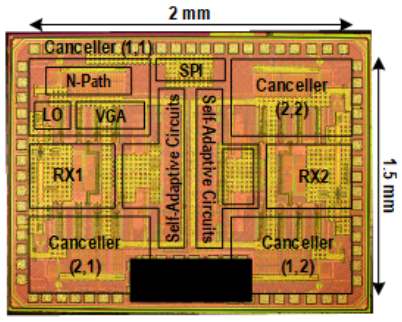


Fig. 10. Chip microphotograph of the 65-nm CMOS FD MIMO RX prototype.

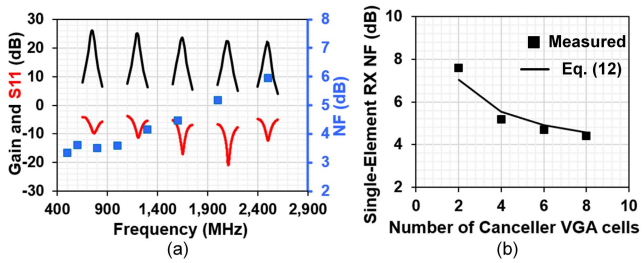


Fig. 11. RX small-signal measurements. (a) gain, NF, and input matching across different LO frequencies with all cancellers disabled. (b) RF SIC power-NF scalability when one canceller is ON.

the feedback SI signal (IN1) is applied to the input of a source follower that has a unity gain, whereas the canceller input signal (IN2) drives the passive mixer. So long as the canceller input signal is large enough to drive the passive mixer, the multiplier output is unchanged. Therefore, the multiplier gain is inversely proportional to canceller input signal amplitude $V_{\rm CX}$, resulting in a linear relation, rather than a quadratic relation indicated by (8), between the adaptive SIC settling time and $V_{\rm CX}$. A large dc gain from integrators is needed for a sufficient SIC as indicated by (10). Therefore, the integrator is implemented using thick oxide transistors with a long channel length (5 μm) to have a dc gain of 40 dB. The 3-dB bandwidth of the integrator is designed to be 1 kHz using a default setting with $C_{\rm int} = 10$ pF and $R_{\rm int} = 160$ kΩ to minimize the ripples on the weights as well as the lower bound on the overall SIC, as discussed in Section II-B. Both $C_{\rm int}$ and $R_{\rm int}$ are made digitally programmable to accommodate different BW options. A compensation resistor R_C with programmable resistance is utilized to cancel a right-half-plane zero introduced by the integrator.

V. Measurement Results

A 65-nm CMOS FD MIMO RX prototype is shown in Fig. 10 and has an active area of 3 mm^2. The chip is packaged and then mounted on a PCB for all measurements.

A. Receiver

Each RX element has a measured gain of 26 dB, an NF of 3.1 dB, and an in-band IIP3 of -10.6 dBm with cancellation circuitry disabled. The gain, NF, and input matching measurements across different LO frequencies are shown in Fig. 11(a). At 2.5 GHz, the NF degrades to 6 dB due to the parasitic capacitance associated with the mixer switches inside the RX. The NF degradation at high frequencies (typically $>$2.5 GHz) is commonly seen for N-path-filter-based circuits and mixer-first RXs (see [16], [32]). The use of an advanced silicon technology would lower the NF at high frequencies.

The power-NF scalability of the SI-canceling RX is measured using a single canceller, and the results are shown in Fig. 11(b). The RX NF is measured to be 4.4 dB, a 1.3-dB NF degradation, with the weakest 12-dB RX-side coupling and all eight canceller VGA unit cells on consuming 53 mW from a 2.5-V supply. Lower power could be obtained using a reduced supply voltage at the expense of linearity performance. Alternatively, larger antenna interface isolation could be leveraged for smaller G_m and, hence, lower power based on (11), but it could lead to a bulky and/or complex antenna interface design. NF of 8.2 dB is measured with the strongest 0-dB RX-side coupling and two canceller VGA unit cells consume 16 mW—corresponding to 8/2 = 12 dB reduction in G_m due to the 12-dB stronger coupling strength. The calculated NF based on (12) is also plotted on top of the measurement results in Fig. 11(b), showing a reasonable match.

The canceller down-converter LO-path has a measured power consumption of 11 mW/GHz from a 1.2-V supply. This power is not scalable with the array size and increases quadratically with the array size.

B. Self-Adaptive Interference Cancellation

The canceller LMS self-adaptive operation is first measured with a single canceller enabled and a fixed antenna interface ISO of 24 dB. Using a +18-dBm single-tone TX signal at 1-GHz carrier frequency and at +10-MHz offset, the canceller

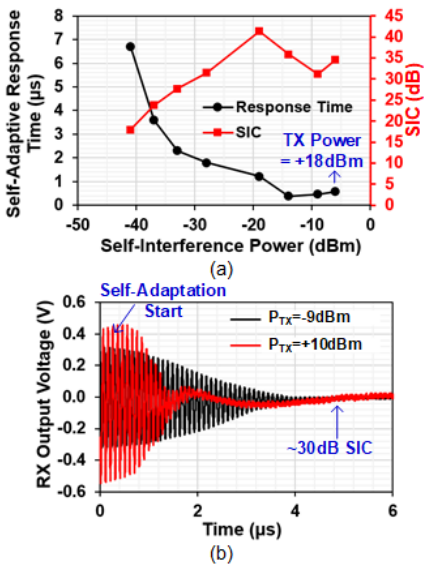


Fig. 12. (a) LMS adaptive RF/analog SIC and (b) its response time measurement.

adapts itself to 35-dB SIC in 0.6 μs in measurement, as shown in Fig. 12(a). As predicted by (8) and the implementation detailed in Section IV, the SIC settling time generally increases as we lower the TX signal power levels. The 30–35-dB SIC settling time does not increase until the TX power reduces to +5 dBm. This is likely due to the compression of the canceller. A weaker TX-side coupling strength would relieve this compression. The SIC settling time measured at +5 dBm TX is 1 μs. Based on (8) and the implementation detailed in Section IV, the expected SIC settling time with a −17-dBm TX signal can be calculated as 1 μs × 10lg[(5−(−17))/20] = 11 μs. In measurement, the SIC settling time of 6.7 μs is measured with a TX power of −17 dBm that is faster than expected. This is due to a reduced achievable SIC that is only about 20 dB. This is 15 dB less compared with the SIC obtained with +18-dBm TX power as the SIC is limited by the adaptation circuitry offset at low TX power level [27]. At weak TX power levels, the adaptive circuitry dc offsets limit the achievable SIC. Measured at the RX BB output, self-adaptive SIC transient responses with a strong and a weak SI are shown in Fig. 12(b). LMS multipliers, integrators, and buffers consume 14 mW in total for each canceller. All subsequent cancellation measurements use self-adaptation without any manual weights tuning.

FD radio linearity tests are shown in Fig. 13. SIC of up to −5 dBm of SI power results in small gain compression (2 dB) of the desired signal, as opposed to nearly 15 dB of compression in the absence of SIC [see Fig. 13(a)]. In a two-tone test, the fundamental and third-order inter-modulation (IM3) tones are measured first with the canceller disabled (i.e., without SIC as in Fig. 13). After that, using the same measurement setup, the fundamental and IM3 tones are measured again with SIC enabled. As shown in Fig. 13(b), it can be seen that the IM3 products become much weaker when SIC is applied. This is as expected because strong SI signals in RX have been suppressed significantly by the SI canceller. The

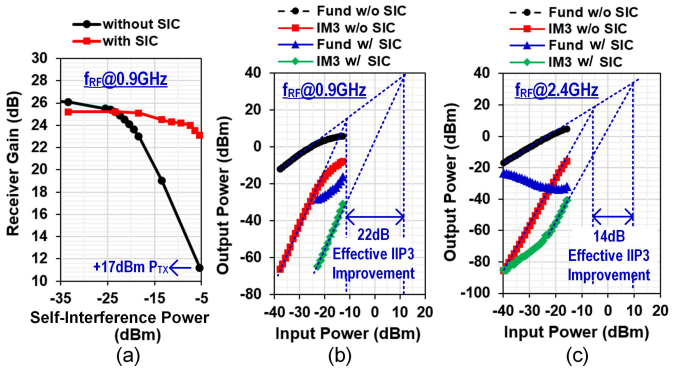


Fig. 13. SIC linearity measurements. (a) Gain compression at 0.9-GHz RF. Two-tone tests at (b) 0.9- and (c) 2.4-GHz RFs.

IM3 products with SIC on include contributions from both the SI canceller and the RX itself.[1] The reduction of IM3 products effectively enhances the RX IIP3 (see Fig. 13) when the two-tone signal is a known SI or XI coming from a co-located TX. Meanwhile, the RX IIP3 in the presence of a general two-tone signal remains the same as the RX linearity is one of its intrinsic properties. When the two-tone signal is centered around 0.9 GHz, the SIC improves the effective in-band RX IIP3 from −11 to +11 dBm. This 22-dB improvement in IIP3 is similar to those in other works using SIC directly at RF, indicating that the BB SIC in this work is transparent to RF and enhances the RF input-side linearity. A two-tone test with and without SIC at 2.4 GHz is also performed and has a 14-dB IIP3 improvement [see Fig. 13(c)].

Joint SI suppression across the antenna and RF domains using an RFCI 0.79-to-0.96-GHz SMA circulator, a custom-made PCB impedance tuner similar to that in [38], and our self-adaptive SIC RX is shown in Fig. 14. The impedance tuner shown in Fig. 14(a) is configured to ensure the best overall SI suppression rather than the highest circulator ISO. Without an antenna-tuner-and-SIC joint optimization, 35-dB ISO from the circulator is achieved by configuring the tuner. However, this high ISO results in a frequency-selective residual SI, limiting the next-stage on-chip SIC to be only 14 dB [see Fig. 14(b)]. Using a joint optimization, the tuner ensures a relatively flat residual SI after ISO. While a relatively low ISO of 27 dB is obtained from the circulator, the overall SI suppression is 27 (ISO) + 29 (RF/analog SIC) = 56 dB, which is an order-of-magnitude higher [see Fig. 14(b)]. Using this joint optimization, the measured amounts of SIC across different antenna terminator voltage-standing-wave ratios (VSWRs) are shown in Fig. 14(c).

We measured overall SI suppression using the setup in Fig. 14 across different antenna VSWRs. Different antenna VSWRs typically correspond to various interference channel delay spreads, affecting obtainable interference cancellation integrated across a wide signal BW [6], [13]. In addition, non-ideal antenna VSWR could result in extra phase shift (replacing R_{RX} in Fig. 5 with Z_{RX}) in the adaptation loop, disturbing the loop dynamics and the resultant cancellation. A study of the LMS loop dynamics in the presence of different

[1]For a more detailed discussion on this, the reader is referred to [29].

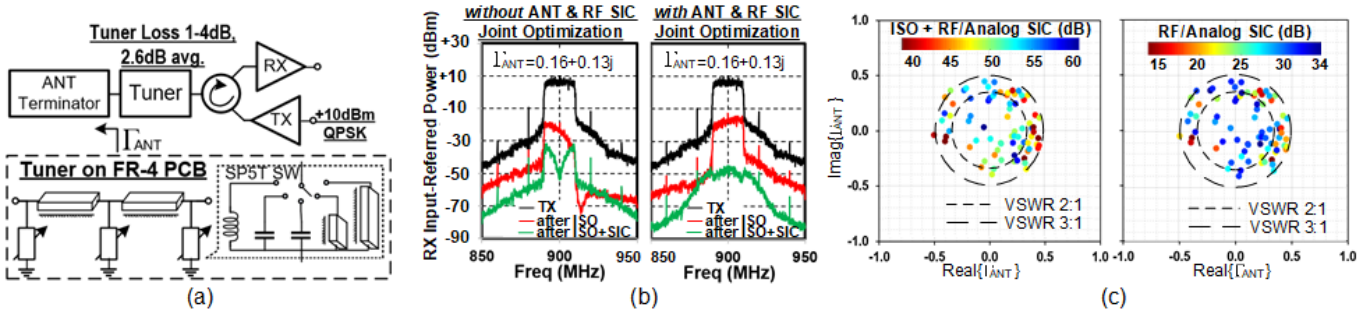


Fig. 14. Joint SI suppression. (a) Setup block diagram. (b) SI suppression with and without joint optimization. (c) Measured SI suppression across VSWRs.

TABLE II
MEASUREMENT SUMMARY AND COMPARISON WITH STATE-OF-THE-ART CMOS RF SIC WORK

	# of input/ output	Freq. range (GHz)	NF w/o SIC (dB)	Wired Antenna interface ISO(dB)/delay	RF/analog SIC(dB)	RF/analog SIC BW (MHz)	NF degra-dation (dB)	Eff. RX IB IIP3 (dBm)	Max. SI power (dBm)	SIC DC power (mW)	SIC NF-power scalable	RF SIC Adapt. Algorithm	RF SIC Adapt. time (μs)
[10]	1/1	1.7 to 2.2	2.5	30-35/ 0.3 ns	30 (RF) +20 (BB)	40	1.55	+17	–10	11.5	No	Gradient descent	N.R.
[13]	1/1	0.9	9.6	50 / 1.4 ns	23	80	1.4	+3.9^	N.R.	13	No	Exhaustive search	N.R.
[27]	1/1	0.8	1.4+	56 / 132 ns	14	1	1.3	N.A.	–30	30.5	No	LMS	25
[16]	2/2	2.2	9.5@	30	15 (RF) +8 (BB)#	20	2.1	N.R.	–15	90	No	Channel estimation	N.R.
This work	1/1	0.5 to 2.5	3.1 to 6	22 / 3 ns	29 or 35 w/ sinusoid SI	20	1.2	+11	–5	16-52$	Yes	LMS	1
	2/2			24 / 6 ns	24 or 18 (OTA)	20	1.3			32-104$			

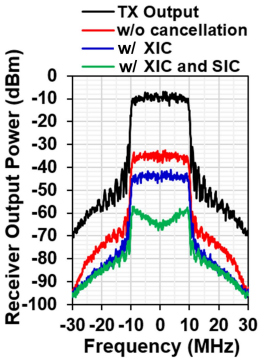
^: simulated. +: LNA only. @ include an integrated circulator #: estimated from the figure $: at 1GHz and not including 14mW LMS power.
N.R.: not reported. N.A.: not applicable.

antenna VSWRs could be an interesting topic for future work; 45-dB worst case overall SI suppression, 51 dB average, across 20 MHz is measured at 30 different antenna impedance values with VSWR up to 2:1. With larger VSWR up to 3:1, 39 dB worst case suppression, 46 dB average, is obtained. The number of antenna impedance points is limited by the number of tuner control bits. Subsequent analog/digital BB SIC is often performed without joint optimization with RF SIC due to the much greater flexibility available at BB than that at RF [6], [11], [13], [18]. Nevertheless, the canceller group delay is made digitally programmable and can be used to perform joint SI suppression with the subsequent BB SIC if needed.

C. Power-Scalable Self- and Cross-Interference Cancellation

A test of simultaneous cancellation of SI and XI is shown in Fig. 15(a). The SI channel exhibits a group delay of 2.5-ns and 30-dB ISO from a circulator, whereas the XI channel is mimicked by 24-dB fixed attention with 5.5-ns delay. The XIC is enabled first and provides 6-dB suppression, and the SIC further suppresses the total interference by another 18 dB.

Compared to the SIC measurement with one canceller on, we used 6-dB stronger RX-side coupling in the FD MIMO SIC and XIC measurement shown in Fig. 15. This allows us to halve the number of active canceller VGA cells based on



Number of FD MIMO elements	1	2
Number of cancellers per element	1	2
Number of canceller VGA cells on	8	4
Canceller RX-side Coupling	12dB	6dB
Array-level NF* [calc. using (13)]	4.4dB [4.5dB]	2.8dB [2.9dB]
Total canceller VGA power per element	53mW	58mW

*Array-level NF = Single-element NF – 10lg*N*

Fig. 15. FD MIMO SIC and XIC measurement as well as its power scalability.

our discussion in Section III, maintaining almost a constant canceller VGA power per element. While this stronger coupling degrades the element-level NF to 5.8 dB, an MIMO operation allows uncorrelated noise averaging across array elements, resulting in a 3-dB reduction in array-level NF when the MIMO is used as a digital phased array. The resultant array-level NF is also calculated using (13), showing a good match between the measurement and the theory. In contrast to the power-scalable RX with a constant array-level NF $F_{\mathrm{RX},C}$ assumed in Section III, our RX power is independent of array size, and hence, its array-level NF reduces. Because of this, the FD MIMO array-level NF in our work is also lowered as in Fig. 15.

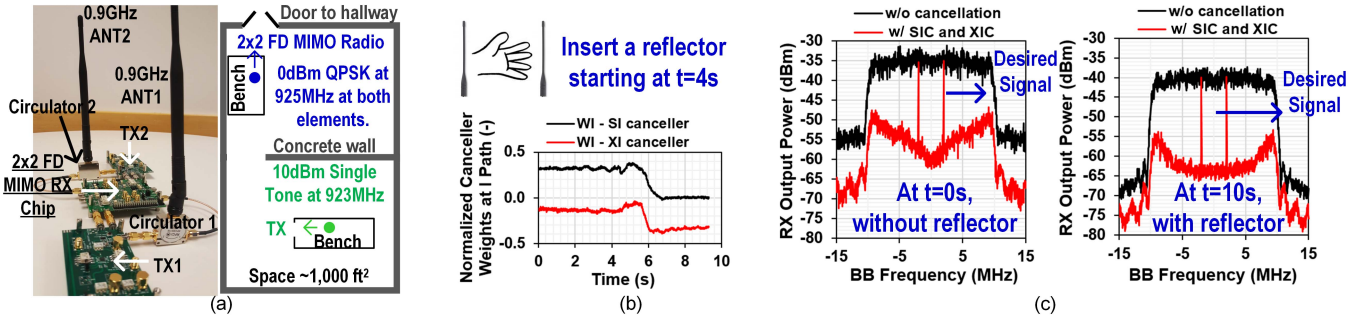


Fig. 16. Demonstration of real-time FD MIMO self-adaptive interference cancellation using low-cost off-the-shelf antennas in a dynamic wireless environment. (a) setup, (b) real-time XIC and SIC weights on cancellers I-paths, and (c) interference suppression before and after having a reflector.

D. Over-the-Air (OTA) FD MIMO Demonstration and Comparison

Real-time interference cancellation using PulseLarsen's 925 MHz portable SMA antennas is demonstrated. The demonstration setup is shown in Fig. 16(a). Fig. 16(b) shows the real-time XIC and SIC weights on cancellers I-paths before and after inserting a reflector. With the presence of both SI and XI, the FD MIMO RX cancellers adapt themselves in real time and provide a robust 18-to-20-dB integrated suppression across the 20-MHz SI and XI BW in a dynamic wireless environment, as shown in Fig. 16(c).

When compared with the state of the art (Table II), our work is the first FD radio with integrated LMS adaptive wideband RF/analog SIC demonstrating microsecond-scale response time and is also widely tunable. In addition, it is the first integrated FD MIMO beamforming RX whose dc power scales almost linearly with the number of antennas due to the canceller power-NF scalability.

VI. Conclusion

While an FD LMS adaptive RF SIC has been demonstrated using off-the-shelf components, it is fully integrated with a 2×2 FD MIMO RX in this work for the first time. A new RFIC-algorithm co-design method is presented, which significantly reduces the adaptation overhead by minimizing the number of canceller taps and by fusing multiple functions into one circuit block. A power-NF scalability makes our design the first FD MIMO beamforming RX whose dc power scales almost linearly with the number of antennas. Topics for future research include further increasing the cancellation BW using a multi-tap design, enhancing the SI canceller dynamic range via both circuit- and system-level innovations, integration of antenna interfaces, and investigation of digitally assisted architectures for flexible and compact large-array designs.

References

[1] S. Katti, "Full duplex radios," in *Proc. 9th ACM Conf. Emerg. Netw. Exp. Technol. (CoNEXT)*, Oct. 2013, pp. 375–386.

[2] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, "In-band full-duplex wireless: Challenges and opportunities," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 9, pp. 1637–1652, Sep. 2014.

[3] Y.-S. Choi and H. Shirani-Mehr, "Simultaneous transmission and reception: Algorithm, design and system level performance," *IEEE Trans. Wireless Commun.*, vol. 12, no. 12, pp. 5992–6010, Dec. 2013.

[4] B. Debaillie *et al.*, "Analog/RF solutions enabling compact full-duplex radios," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 9, pp. 1662–1673, Sep. 2014.

[5] J. Zhou *et al.*, "Integrated full-duplex radios," *IEEE Commun. Mag.*, vol. 55, no. 4, pp. 142–151, Apr. 2017.

[6] J. Zhou, T.-H. Chuang, T. Dinc, and H. Krishnaswamy, "Integrated wideband self-interference cancellation in the RF domain for FDD and full-duplex wireless," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3015–3031, Dec. 2015.

[7] D.-J. van den Broek, E. A. M. Klumperink, and B. Nauta, "An in-band full-duplex radio receiver with a passive vector modulator downmixer for self-interference cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3003–3014, Dec. 2015.

[8] D. Yang, H. Yuksel, and A. Molnar, "A wideband highly integrated and widely tunable transceiver for in-band full-duplex communication," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1189–1202, May 2015.

[9] S. Ramakrishnan, L. Calderin, A. Niknejad, and B. Nikolić, "An FD/FDD transceiver with RX band thermal, quantization, and phase noise rejection and >64dB TX signal cancellation," in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig.*, Jun. 2017, pp. 352–355.

[10] T. Zhang, C. Su, A. Najafi, and J. C. Rudell, "Wideband dual-injection path self-interference cancellation architecture for full-duplex transceivers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1563–1576, Jun. 2018.

[11] K.-D. Chu, M. Katanbaf, T. Zhang, C. Su, and J. C. Rudell, "A broadband and deep-TX self-interference cancellation technique for full-duplex and frequency-domain-duplex transceiver applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 170–172.

[12] N. Reiskarimian, M. B. Dastjerdi, J. Zhou, and H. Krishnaswamy, "Analysis and design of commutation-based circulator-receivers for integrated full-duplex wireless," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2190–2201, Aug. 2018.

[13] A. El Sayed *et al.*, "A Hilbert transform equalizer enabling 80 MHz RF self-interference cancellation for full-duplex receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 1153–1165, Mar. 2019.

[14] M. Katanbaf, K.-D. Chu, T. Zhang, C. Su, and J. C. Rudell, "Two-way traffic ahead: RFAnalog self-interference cancellation techniques and the challenges for future integrated full-duplex transceivers," *IEEE Microw. Mag.*, vol. 20, no. 2, pp. 22–35, Feb. 2019.

[15] D. Bharadia and S. Katti, "Full duplex MIMO radios," in *Proc. USENIX NSDI*, 2014, pp. 359–372.

[16] M. B. Dastjerdi, S. Jain, N. Reiskarimian, A. Natarajan, and H. Krishnaswamy, "Full-duplex 2×2 MIMO circulator-receiver with high TX power handling exploiting MIMO RF and shared-delay baseband self-interference cancellation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 448–450.

[17] Y. Cao and J. Zhou, "A CMOS 0.5-2.5GHz full-duplex MIMO receiver with self-adaptive and power-scalable RF/analog wideband interference cancellation," in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig.*, Jun. 2019, pp. 147–150.

[18] D. Korpi *et al.*, "Full-duplex mobile device: Pushing the limits," *IEEE Commun. Mag.*, vol. 54, no. 9, pp. 80–87, Sep. 2016.

[19] K. Trotskovsky *et al.*, "A 0.25-1.7-GHz, 3.9-13.7-mW power-scalable, −10-dBm harmonic blocker-tolerant mixer-first RF-to-digital receiver for massive MIMO applications," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 2, pp. 38–41, Feb. 2018.
[20] N. Reiskarimian *et al.*, "One-way ramp to a two-way highway: Integrated magnetic-free nonreciprocal antenna interfaces for full-duplex wireless," *IEEE Microw. Mag.*, vol. 20, no. 2, pp. 56–75, Feb. 2019.
[21] A. Carusone and D. A. Johns, "Analogue adaptive filters: Past and present," *IEE Proc.-Circuits, Devices Syst.*, vol. 147, no. 1, pp. 82–90, Feb. 2000.
[22] T.-C. Lee and B. Razavi, "A 125-MHz mixed-signal echo canceller for gigabit Ethernet on copper wire," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 366–373, Mar. 2001.
[23] L. Calderin, S. Ramakrishnan, A. Puglielli, E. Alon, B. Nikolic, and A. M. Niknejad, "Analysis and design of integrated active cancellation transceiver for frequency division duplex systems," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2038–2054, Aug. 2017.
[24] K. E. Kolodziej, J. G. Mcmichael, and B. T. Perry, "Multitap RF canceller for in-band full-duplex wireless communications," *IEEE Trans. Wireless Commun.*, vol. 15, no. 6, pp. 4321–4334, Jun. 2016.
[25] V. Ilderem, "1.4 5G wireless communication: An inflection point," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 35–39.
[26] S. Kim, Y. Jeon, G. Noh, Y.-O. Park, I. Kim, and H. Shin, "A 2.59-GHz RF self-interference cancellation circuit with wide dynamic range for in-band full-duplex radio," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.
[27] V. Aparin, G. J. Ballantyne, C. J. Persico, and A. Cicalini, "An integrated LMS adaptive filter of TX leakage for CDMA receiver front ends," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1171–1182, May 2006.
[28] A. Ershadi and K. Entesari, "A 0.5-to-3.5 GHz self-interference-canceling receiver for in-band full-duplex wireless," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 151–154.
[29] J. Zhou, A. Chakrabarti, P. R. Kinget, and H. Krishnaswamy, "Low-noise active cancellation of transmitter leakage and transmitter noise in broadband wireless receivers for FDD/Co-existence," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3046–3062, Dec. 2014.
[30] A. Puglielli *et al.*, "Design of Energy- and cost-efficient massive MIMO arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 586–606, Mar. 2016.
[31] Z. Lin, P. Mak, and R. P. Martins, "2.4 A 0.028mm^2 11mW single-mixing blocker-tolerant receiver with double-RF N-path filtering, S11 centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
[32] L. Zhang, A. Natarajan, and H. Krishnaswamy, "Scalable spatial notch suppression in Spatio-Spectral-Filtering MIMO receiver arrays for digital beamforming," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3152–3166, Dec. 2016.
[33] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.
[34] X. Huang and Y. J. Guo, "Radio frequency self-interference cancellation with analog least mean-square loop," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3336–3350, Sep. 2017.
[35] A. Medra *et al.*, "An 80 GHz low-noise amplifier resilient to the TX spillover in phase-modulated continuous-wave radars," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1141–1153, May 2016.
[36] E. Everett, C. Shepard, L. Zhong, and A. Sabharwal, "SoftNull: Many-antenna full-duplex wireless via digital beamforming," *IEEE Trans. Wireless Commun.*, vol. 15, no. 12, pp. 8077–8092, Dec. 2016.
[37] T. L. Marzetta, E. G. Larsson, H. Yang, and H. Q. Ngo, *Fundamentals of Massive MIMO*. Cambridge, U.K.: Cambridge Univ. Press, 2016.
[38] S. Kousai, K. Onizuka, J. Wadatsumi, T. Yamaguchi, Y. Kuriyama, and M. Nagaoka, "Polar antenna impedance detection and tuning for efficiency improvement in a 3G/4G CMOS power amplifier," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2902–2914, Dec. 2014.

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