Balanced-to-Doherty Mode-Reconfigurable Power Amplifier With High Efficiency and Linearity Against Load Mismatch

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***Abstract*— A balanced-to-Doherty (B2D) mode-reconfigurable power amplifier (PA) is presented in this article, which is endowed with a unique capability of maintaining high linearity and high efficiency against load mismatch. The Doherty operation of this PA is based on a new Doherty PA (DPA) architecture configured from an ideal balanced amplifier, named quasi-balanced DPA (QB-DPA). This article, for the first time, analytically proves that the QB-DPA is functionally equivalent to a standard DPA. Most importantly, this new discovery enables PA reconfiguration between the Doherty and balanced modes. With the tunability implemented using a silicon-on-insulator (SOI)-based single-pole-double-throw (SPDT) switch, a reconfigurable B2D PA prototype using GaN technology is demonstrated at 3.5 GHz, exhibiting the state-of-the-art linear DPA performance in the nominal 50-Ω load condition. Specifically, the Doherty mode achieves a continuous-wave measurement efficiency of 70% and 54.5% at the maximum output power of 41.9 dBm and 6-dB power back-off, respectively. In the modulated long-term evolution (LTE) evaluation, the DPA exhibits −37-dB adjacent channel power leakage (ACPR) and 2.36% error vector magnitude (EVM) at the maximum rated power of 34.5 dBm while achieving a 42.4% efficiency. It is experimentally demonstrated that the Doherty (QB-DPA) mode is well resistant to load mismatch with high efficiency across a majority portion of the 2:1 voltage standing wave ratio (VSWR) circle, while the combination of Doherty and balanced modes can ensure a constantly linear performance of the B2D PA (e.g., 2.2% − 5% of EVM) under the entire mismatch condition.**

***Index Terms*— Balanced amplifier, Doherty power amplifier (DPA), linearity, load mismatch, reconfigurable.**

I. Introduction

THE evolution of wireless communications has triggered ever-increasing demands for higher data rate and enhanced spectral efficiency, which are typically realized through widened modulation bandwidths and advanced modulation techniques, such as orthogonal frequency-division multiplexing (OFDM) and high-order quadrature amplitude modulation (e.g., 1024 QAM). These modulation schemes introduce large peak-to-average power ratio (PAPR) that not only substantially degrade the power amplifier (PA) efficiency but also impose stringent linearity requirements on PAs. Consequently, the PA's capability of efficiently and linearly transmitting high-PAPR signals is critical to modern communication systems toward ultrafast speed and high energy efficiency.

In the past two decades, the Doherty PA (DPA) architecture has been widely employed in wireless communications infrastructures (e.g., base stations) due to its enhanced efficiency at significant power back-offs. Until now, numerous DPA techniques and demonstrations have been reported, exhibiting significant progress toward realizing highly efficient DPAs in various semiconductor technologies [1]–[7] together with extended application horizons, e.g., from single band to multiband [8]–[13] and from microwave frequencies to millimeter-wave frequencies [14]–[20].

In realistic communications, due to the nonlinear nature of DPAs, external linearization using digital predistortion (DPD) is usually applied to DPAs to maintain the transmission signal's fidelity and to comply with specific communications standards. In the future generations of wireless communications, e.g., 5G, the cell size is expected to be reduced significantly (e.g., from marco cell to micro/femto cell), leading to much higher base-station densities and considerably lower power levels. Since DPD is quite energy consuming, especially when accommodating wide modulation bandwidths of signals [21], PAs at lowered power level are strongly desired to be intrinsically linear. Recently, several linear DPAs have been presented in terms of both theoretical analysis and practical design demonstrating enhanced linearity as well as high efficiency [22]–[25].

On the other hand, the spatial multiplexing/combining techniques, such as multi-input–multioutput (MIMO) antennas and active antenna array, have been widely applied in the 5G communications to further increase the data rate, radiation distance, and overall system capacity. However, the mutual coupling between different antennas under concurrent MIMO transmissions and/or beam steering can lead to ongoing variation of antenna impedance at very fast time scales [26]–[29]. As a result, the current solution of discrete antenna tuners based on phase detection and feedback control will in-all-likelihood not be able to seamlessly respond to such a rapid impedance variation [30]. Although the circulators/isolators can be placed between PA and antenna element, they introduce extra loss and are too costly and bulky for massive

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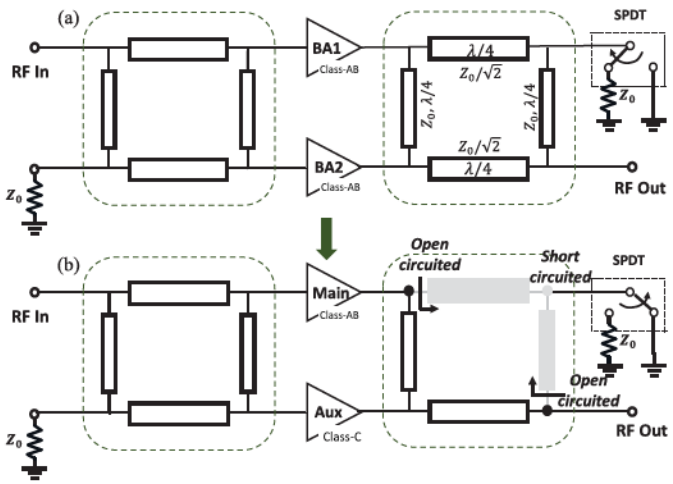

Fig. 1. Conceptual architecture of the proposed B2D mode-reconfigurable PA. A silicon-on-insulator (SOI)-based SPDT switch terminates the isolation port of the output coupler to 50-Ω load and ground alternatively. (a) Balanced mode. (b) Doherty mode.

array applications [27], [29]. Therefore, the PAs in future communication systems are expected to maintain efficient and linear operations against substantial load mismatch by themselves. Different from the conventional impedance tuning method, new paradigms of mismatch recovery at the PA stage have been investigated, such as specialized control of digital DPAs against load variation [31] and direct impedance measurement using distributed sensors [32]. Until now, there has not been a solid solution that is able to cover a large impedance variation range and is readily compatible with the existing systems as a "drop-in" module.

To solve the aforementioned challenges, a balanced-to-Doherty (B2D) mode-reconfigurable PA is proposed in this article, as conceptually shown in Fig. 1. The isolation port of the output coupler is alternatively terminated to 50-Ω load and ground to enable the balanced and Doherty modes, as shown in the Fig. 1(a) and (b), respectively, which can be physically realized by a single-pole double-throw (SPDT) switch. In our related conference article [33], we have preliminarily presented a proof-of-concept demonstration of the B2D reconfigurable PA. This article significantly expands our previous works [33], [34] in the following aspects. First, a generalized theory of the quasi-balanced DPA (QB-DPA) (Doherty mode of the B2D reconfigurable PA) is analyzed based on the ideal mathematical model of quadrature coupler, and it is analytically proved that the load modulation behavior of QB-DPA is equivalent to the conventional DPA. This generalization inclusively explains and verifies the designs using branch-line hybrids [33] and [34]. Second, a systematical design methodology of the B2D PA is presented, targeting for high linearity and efficiency at both the balanced and Doherty modes. Based on the QB-DPA theory and the proposed design methodology, a prototype is developed using the GaN technology at 3.5 GHz, demonstrating the state-of-the-art DPA performance in terms of linearity and efficiency at the nominal 50-Ω load condition. Third, a comprehensive mismatch evaluation using modulated signals is experimentally presented. It is remarkably discovered that the linear and efficient PA performance can be well maintained up to 2 : 1 (predicted in typical MIMO operations [26], [35]) of voltage standing wave ratio (VSWR) by using the B2D reconfiguration.

In actual MIMO systems [29], [36], the transmitter system performance [e.g., ALCR and error vector magnitude (EVM)] is monitored in real time, and the PA can be adapted from the QB-DPA mode to balanced mode when an abnormal linearity is detected. In phased-array applications, the impedance of each antenna element could be precharacterized as a function of scan angle [29]. For a particular antenna element, the associated PA can be adapted according to scan angle. Envisioning these scenarios, the B2D adaption can be applied seamlessly without having to detect the phase and amplitude of mismatch.

II. Quasi-Balanced DPA Theory

In this section, based on the new QB-DPA configuration, the operation of active load modulation is theoretically analyzed. In this circuit topology, the essential Doherty combining network is implemented using a specially configured quadrature coupler in a balanced amplifier topology, as shown in Fig. 1. In [37] and [38], by leaving the isolation port of the branch-line coupler as open circuit, the possibility of implementation hybrid coupler as a output combining network for the DPAs is introduced. In this section, a new methodology of quadrature hybrid modularization is theoretically analyzed.

Assuming a system impedance of Z_0, the voltage and current relationship of the four-port coupler network can be expressed using an impedance matrix constructed with Z-parameters, given by

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}. \quad (1)$$

To theoretically model this new type of DPA, a simplified output combining network is constructed based on an ideal 3-dB quadrature hybrid coupler model, as shown in Fig. 2, including the excitation and loading. The isolation port (Port 2) is terminated to ground, and the output port (Port 1) is loaded to a 50-Ω terminal. Two ideal current sources I_M and I_A, which represent the main and auxiliary amplifiers, are connected to the two excitation ports (Ports 4 and 3) of the coupler, respectively.

As the isolation port is grounded, the associated port voltage is thus zero. By applying this condition ($V_2 = V_{\text{Iso}} = 0$) on the first row expansion of the matrix operation in 1, the dependence of the main amplifier current and load current can be determined by

$$I_M = \frac{\sqrt{2}}{2} I_0 \quad (2)$$

where $I_M = I_4$ and $I_0 = I_1$. Meanwhile, the load current and voltage of the RF-output port can be expressed by

$$V_0 = -Z_0 I_0. \quad (3)$$

In this design, to ensure reconfiguration between the Doherty and balanced modes, the main and auxiliary PAs

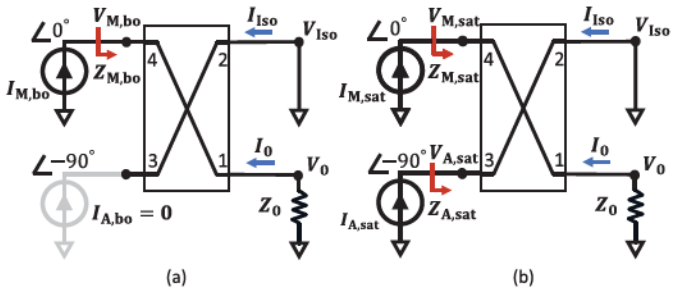

Fig. 2. Generalized schematic of the output combining network for analyzing the proposed QB-DPA architecture at (a) 6-dB power back-off and below and (b) power saturation.

in the Doherty mode are identical in terms of the current/voltage scaling because this symmetry has to be enforced in the balanced mode. Nevertheless, the main and auxiliary PAs can be asymmetrical in Doherty-only designs based on this quasi-balanced configuration. The theoretical analysis on the QB-DPA operation is performed at both back-off and saturation.

A. QB-DPA Operation at 6-dB Power Back-Off and Below

In the power region at 6-dB back-off and below, the equivalent circuit can be modeled, as shown Fig. 2(a). As the auxiliary amplifier is turned off, it presents an ideal open circuit to Port 3 with no current injection from the auxiliary path ($I_A = I_3 = 0$). With this boundary condition, the matrix operation in (1) can be rewritten as

$$\begin{bmatrix} V_0 \\ 0 \\ V_A, \text{bo} \\ V_M, \text{bo} \end{bmatrix} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \begin{bmatrix} I_0 \\ I_{\text{Iso}} \\ 0 \\ I_M, \text{bo} \end{bmatrix} \tag{4}$$

where $V_{M,\text{bo}}$ and $I_{M,\text{bo}}$ denote the back-off voltage and current of the main amplifier, respectively, and $V_{A,\text{bo}}$ represents the voltage swing at the floating auxiliary amplifier port. By substituting the condition of $I_A = 0$ into the abovementioned matrix operation in (4), it leads to the following dependences:

$$V_{M,\text{bo}} = -j\sqrt{2} I_{\text{Iso}} Z_0 \;\&\; I_{\text{Iso}} = j I_0. \tag{5}$$

Together with (2), the impedance seen by the main and auxiliary amplifiers can be expressed as

$$\begin{aligned} Z_{M,\text{bo}} &= \frac{V_{M,\text{bo}}}{I_{M,\text{bo}}} \\ &= \frac{-j\sqrt{2} I_{\text{Iso}}}{I_{M,\text{bo}}} Z_0 \\ &= 2Z_0 \\ Z_{A,\text{bo}} &= \infty. \end{aligned} \tag{6}$$

From (6), it is interesting to note that this QB-DPA is functionally equivalent to the standard DPA at the power back-off condition.

B. QB-DPA Operation at Power Saturation

At the saturated power level, both the main and auxiliary amplifiers are fully operating toward saturation of voltage and current so that the impedance matrix can be rearranged as

$$\begin{bmatrix} V_0 \\ 0 \\ V_A, \text{sat} \\ V_M, \text{sat} \end{bmatrix} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \begin{bmatrix} I_0 \\ I_{\text{Iso}} \\ I_A, \text{sat} \\ I_M, \text{sat} \end{bmatrix}. \tag{7}$$

Since the two amplifiers are identically designed, the saturation voltages and currents between the main and auxiliary paths have the same magnitude. By conducting the matrix operation using 7, the following dependences are formed:

$$I_{M,\text{sat}} = j I_{A,\text{sat}} \;\&\; I_{\text{Iso}} = 0. \tag{8}$$

The 90° phase difference between I_M and I_A is due to the ideal 3-dB quadrature-coupler divider at the input. It is also interesting to note that the isolation port becomes an electrical "null" in this condition since it has zero voltage and zero current simultaneously. Based on (3) and (8), the load impedance seen by the main amplifier, i.e., $Z_{M,\text{sat}}$, can thus be calculated using the associated saturation voltage $V_{M,\text{sat}}$ and current $I_{M,\text{sat}}$ given by

$$\begin{aligned} Z_{M,\text{sat}} &= \frac{V_{M,\text{sat}}}{I_{M,\text{sat}}} \\ &= \frac{j I_{A,\text{sat}} - j\sqrt{2} I_{\text{Iso}}}{I_{M,\text{sat}}} Z_0 \\ &= Z_0. \end{aligned} \tag{9}$$

For the auxiliary path, the exhibited load $Z_{A,\text{sat}}$ can be derived as

$$\begin{aligned} Z_{A,\text{sat}} &= \frac{V_{A,\text{sat}}}{I_{A,\text{sat}}} \\ &= \frac{j I_{M,\text{sat}} - j2 I_{M,\text{sat}}}{I_{A,\text{sat}}} Z_0 \\ &= Z_0. \end{aligned} \tag{10}$$

Equations (9) and (10) underline that the QB-DPA operation at the saturation level is again equivalent to a standard DPA.

The load modulation behaviors of the main and auxiliary PAs at both power back-off and power saturation reveal a remarkable discovery; when loading the isolation port of the output quadrature coupler to ground, the balanced PA can be fully converted into an ideal DPA. This finding not only enables the PA reconfiguration between the Doherty and balanced modes but also exhibits promising potential of the QB-DPA for extension to wideband implementations since the balanced amplifier configuration is considered bandwidth-friendly by nature [39], [40].

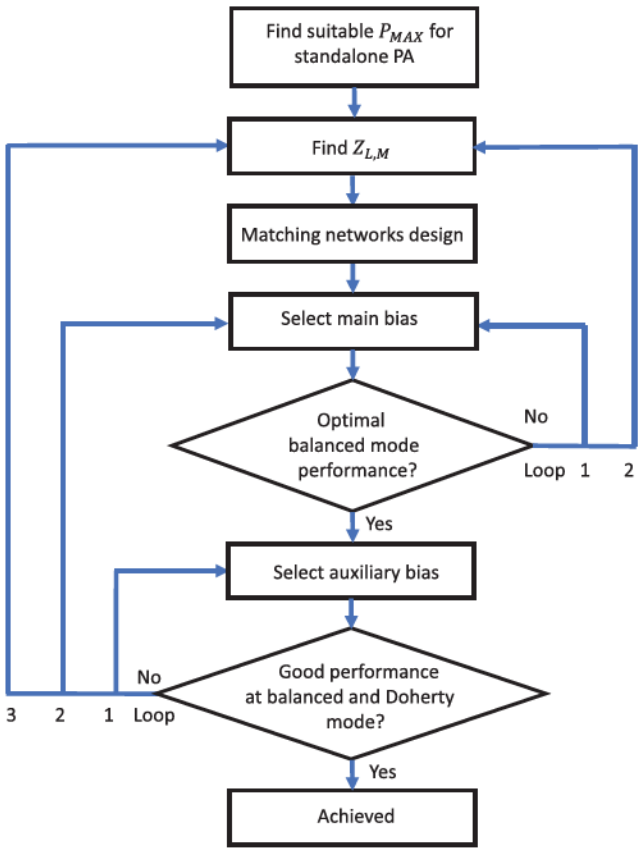

Fig. 3. Systematic design flow of the B2D mode-reconfigurable PA.

III. Practical Design Methodology of Linear B2D Mode-Reconfigurable PA

The derivation described in Section II shows the possibility of converting a balanced PA into an ideal DPA by terminating the isolation port of the output coupler to ground. Based on the proposed theory, the design methodology of linear B2D mode-reconfigurable PA is presented in this section. It is worth noting that the two standalone PAs in the QB-DPA architecture should be identically designed and, thus, the device periphery ratio is equalized between the main and auxiliary transistors. The flowchart in Fig. 3 describes the detailed design procedure, which includes the following key steps.

1) *Step 1 (Determination of P_{Max}):* The maximum power is usually determined by the target application in which the maximum rated power (P_{Rated}) is specified by the particular communications standard. P_{Rated} can be approximately expressed as

$$P_{\text{Rated}} = P_{1\,\text{dB}} - \text{PAPR}. \tag{11}$$

where $P_{1\,\text{dB}}$ is the 1-dB compression point, and PAPR represents the peak-to-average ratio of the modulated signal. In this linear PA design, P_{Max} is selected to allow sufficient headroom for linear amplification of modulated signals. In real-world implementations, this P_{Max} is physically realized by properly selecting semiconductor technology and transistor size.

2) *Step 2 (Loadline Selection):* Since the balanced mode requires two amplifier branches to be fully symmetrical, the loadlines of main and auxiliary amplifiers are identically selected ($Z_{\text{M}} = Z_{\text{A}}$). A full power utilization transistor designed in **Step 1** is ideally associated with a unique load impedance for a particular class of PA which generates optimized power and efficiency, which can be determined using load–pull at the operation frequency. However, the linearity is usually not optimal following the conventional load–pull evaluation. Given the fact that PA linearity is the key factor in determining whether a system is compliant to a certain communication standard, the possible impedance selection (at both fundamental and harmonic frequencies) in this design is prioritized for linearity with a meanwhile balance for efficiency, gain, and power.

3) *Step 3 (Matching Networks Design):* After determining the optimal loadline, the output matching network (OMN) is designed to physically realize the target impedance at both fundamental and harmonic frequencies. It is important to note that the OMN also plays an important role in determining the load modulation behaviors of main and auxiliary PAs in the Doherty mode [22], which needs to be codesigned with the coupler-based combiner for achieving efficient and linear performance in the Doherty mode. The source impedance can also affect the PA gain and linearity. A conjugate match is desired for maximized gain, while a slight mismatch (if properly designed) can lead to optimized linearity [41]. Therefore, the input matching network design should consider both aspects, and a compromise is necessary. To enforce the symmetry of balanced mode, the input matching network (IMN) and OMN are identically designed for the two amplifiers.

4) *Step 4 (Bias Selection for Balanced Mode):* In the balanced mode, the two PAs are biased identically for both gate and drain. Therefore, the behavior of the entire balanced amplifier can be treated the same as a standalone PA. In addition to the loadline impedance, the PA linearity profile across the entire power range is also strongly influenced by the gate bias level of the main transistor. Empirically, the PA is biased at Class-AB mode to yield a good balance between efficiency and linearity, and a bias sweep can be performed to eventually determine the value.

5) *Step 5 (Bias Selection for Doherty Mode):* In the Doherty mode, the main and auxiliary amplifiers are biased in Class-AB and Class-C, respectively. The linearity and efficiency are highly dependent on the combination of these two bias voltages because the turn-on point of the auxiliary PA determines the back-off efficiency, while the interaction (i.e., load modulation) between the main and auxiliary PAs dominates the AM–AM and AM–PM profiles. Therefore, the bias voltages are carefully selected based on a nearly exhaustive search to identify an optimal combination. If the linearity requirement cannot be met, we need to revisit the loadline selection and conduct the process from **Step2**.

Overall, the design method considers the PA performance of both Doherty and balanced modes in terms of linearity,

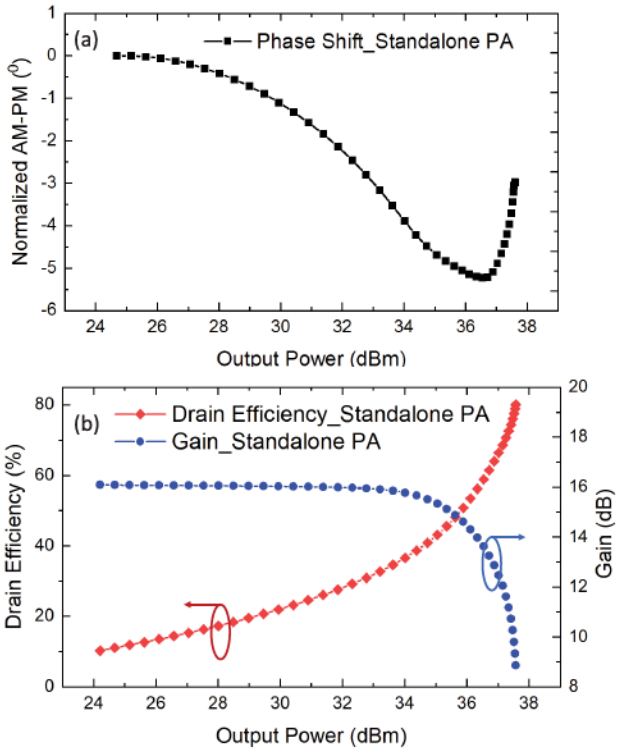

Fig. 4. Simulation results of the standalone PA at 3.5 GHz. (a) Normalized AM–PM. (b) DE and gain.

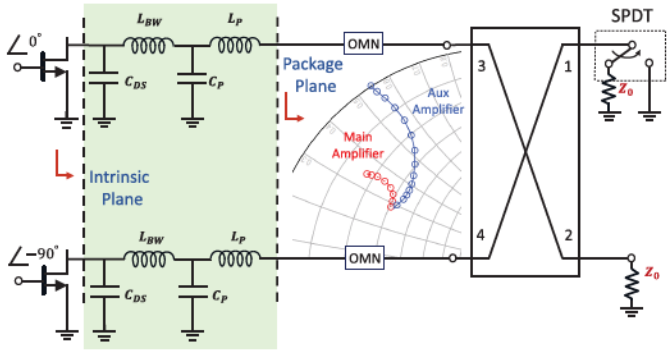

Fig. 5. Designed output combiner network with device parasitics. The inset Smith chart illustrates the desired dynamic load trajectories at package plane for the main and auxiliary amplifiers.

efficiency, power, gain, and so on. It is important to emphasize that if the linearity can be maintained in both modes, the B2D reconfiguration can greatly extend the operation space of the PA into a large variation of load impedance, as the balanced amplifier has been well proved to be insensitive to load mismatch [39], [40].

IV. Prototype Design and Demonstration

The methodology presented in Section III is implemented to design and realize a prototype of the proposed B2D mode-reconfigurable PA with high efficiency and enhanced linearity at both balanced and Doherty modes. In this design, two 6-W GaN packaged transistors CGH40006P from Wolfspeed are utilized as the power device of a PA operating at a center frequency of 3.5 GHz.

A. Design of the Standalone GaN PA

A load–pull simulation was conducted using the selected transistor model with ADS for the standalone PA, in which the device parasitics have been considered. At the device package plane, the optimal load impedances for fundamental and second harmonic for this design were chosen to be $13+j9$ and $j65\ \Omega$, respectively, in order to allow for an optimal linearity to meet the communication standard mentioned in Section III. To physically realize the target fundamental and harmonic terminations, a second-harmonic trap is properly designed together with synthesized fundamental matching using a stepped multisection transmission-line (TL) matching network that also absorbs the drain bias line.

The design of IMN for the standalone PA is targeted for perfecting the linearity performance without considerably compromising the gain capability. Practically, the desired source impedance of the transistor is extracted from the source-pull simulation, while a slight mismatch is carefully conducted in the IMN design in order to achieve an enhanced AM–PM. Meanwhile, a Class-AB mode of gate bias was selected for achieving a balance of linearity and efficiency consideration. The linearity profile of the designed standalone PA is shown in Fig. 4, including a linearized AM–PM profile that is normalized with respect to the small-signal value in Fig. 4(a) and a flat AM–AM profile (gain versus output power) in Fig. 4(b). The complete design of the standalone PA exhibits an efficient performance at 3.5 GHz with a simulated maximal drain efficiency (DE) of 80% toward power saturation, as shown in Fig. 4(b).

B. Design of B2D Reconfigurable PA With Optimized Efficiency and Linearity

Based on the initial design of the standalone PA, a linear and high efficiency balanced amplifier is formed by coupling two such PAs with 90° of phase offset through two quadrature couplers as the input power splitter and output combiner, respectively. Due to its highly symmetrical characteristics, a balanced PA presents the same linearity characteristic as a single standalone PA with doubled output power.

As the isolation port is short circuited to ground, the operation of the B2D PA is reconfigured to the Doherty mode by enabling of the switch. Due to the parasitics of the transistors resulting from the GaN chip and package as shown in Fig. 5, the desired load trajectory can deviate from the optimal path, which could be exacerbated, especially when the effect of OMN and output combiner are taken into consideration. This may eventually lead to a degradation of linearity and efficiency. In order to perfect the load modulation behavior, a codesign of the OMN and combiner is essential, and a global optimization is performed with the overall circuit schematic following the procedure depicted in Section III. The finalized schematic of B2D reconfigurable PA is shown in Fig. 6, including the parameters of all the circuit components.

Moreover, an optimal biasing combination of the main and auxiliary PAs is carefully chosen for perfecting linearity, as shown in Fig. 7. In this linearity optimized mode, a linear AM–PM can be achieved with $< 2°$ of variation from low

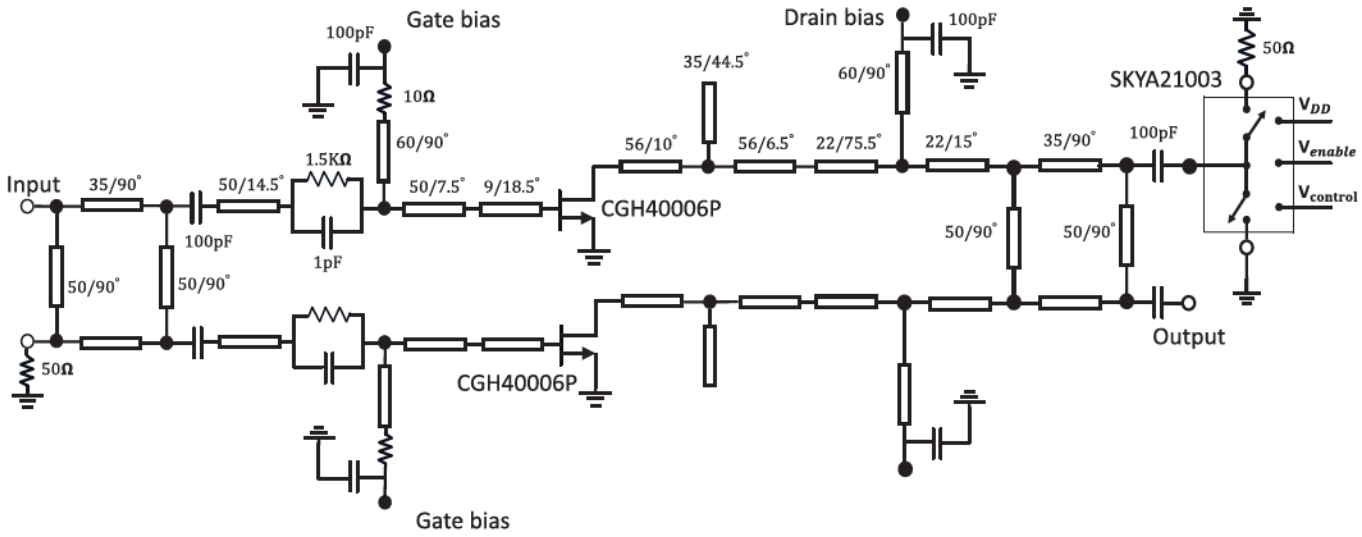

Fig. 6. Overall schematic of the designed B2D mode-reconfigurable PA with an implemented SOI-based SPDT switch.

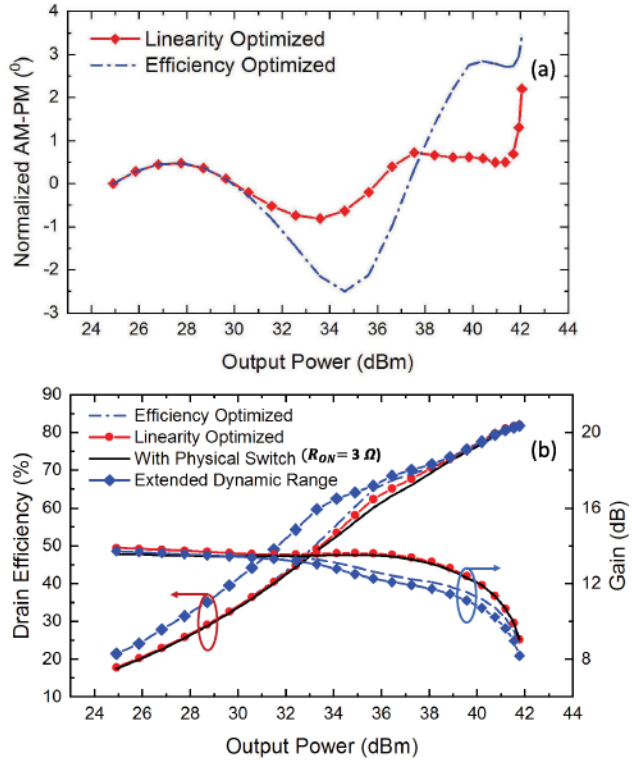

Fig. 7. Linearity- and efficiency-optimized designs of QB-DPA (Doherty mode of B2D PA). (a) Normalized AM–PM. (b) DE and gain.

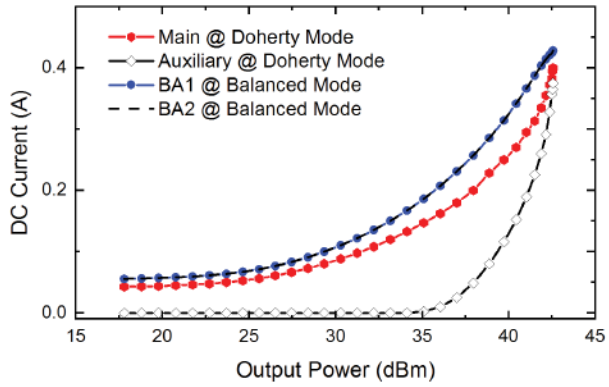

Fig. 8. Comparison of simulated drain dc currents between the balanced and Doherty modes.

power to $P_{1\,\mathrm{dB}}$ shown in Fig. 7(a). Meanwhile, a flat AM–AM is also realized, as shown in Fig. 7(b) while achieving a saturation efficiency as high as 80% and a 62% efficiency at 6-dB power back-off. The back-off efficiency can be further improved with a different bias setting oriented for optimized efficiency while slightly compromising the linearity. This mode can be applied when DPD is available. Meanwhile, an extended 9-dB power back-off dynamic range can be achieved with a properly adjusted drain biases of the main and auxiliary amplifiers in the QB-DPA mode.

The power-dependent dc currents of the main and auxiliary amplifiers are shown in Fig. 8. It is observed that the auxiliary current rises sharply after turning on, and it reaches to the same level as the main amplifier current in the saturation region. This is mainly due to the strong expansion behavior of GaN device under Class-C bias condition. This is achieved with an equal input power split ratio using the quadrature coupler. In comparison with balanced mode, the saturation currents are the nearly the same due to the saturation of two subamplifier, while the QB-DPA mode significantly reduces the current consumption at power back-off.

C. Qudrature Coupler and RF Switch Implementations

The reconfigurability of this B2D PA is realized with the implementation of a quadrature coupler and an RF switch. For the single-section branch-line hybrid coupler used in this design, there is an alternative topology to realize the switchable B2D combiner, as shown in Fig. 9(a), in which a single switch is placed between the main amplifier node and the top quarter-wave branch line. An open circuit needs to be created by the switch to enable the Doherty mode. This open circuit can be converted into short circuit at the isolation node

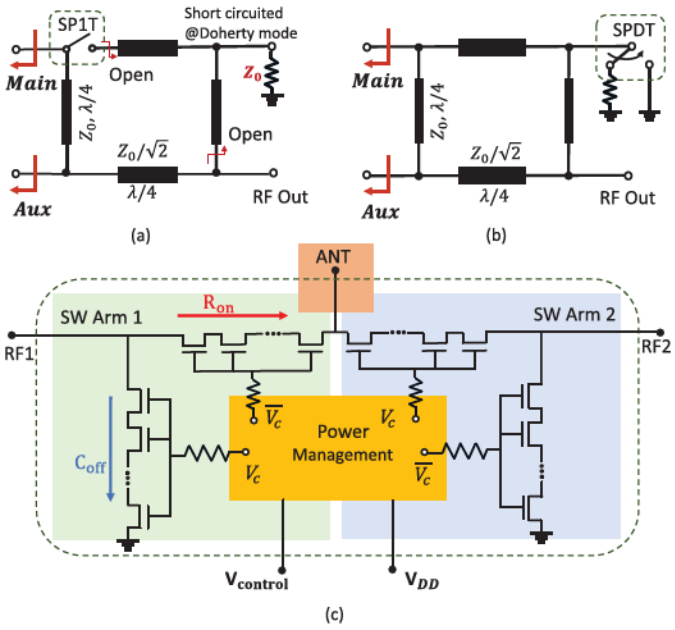

Fig. 9. Realization of reconfigurability using RF switch(es). (a) Alternative circuit topology with a single switch. (b) Design using an SPDT switch. (c) Schematic of the SOI-COMS SPDT switch.

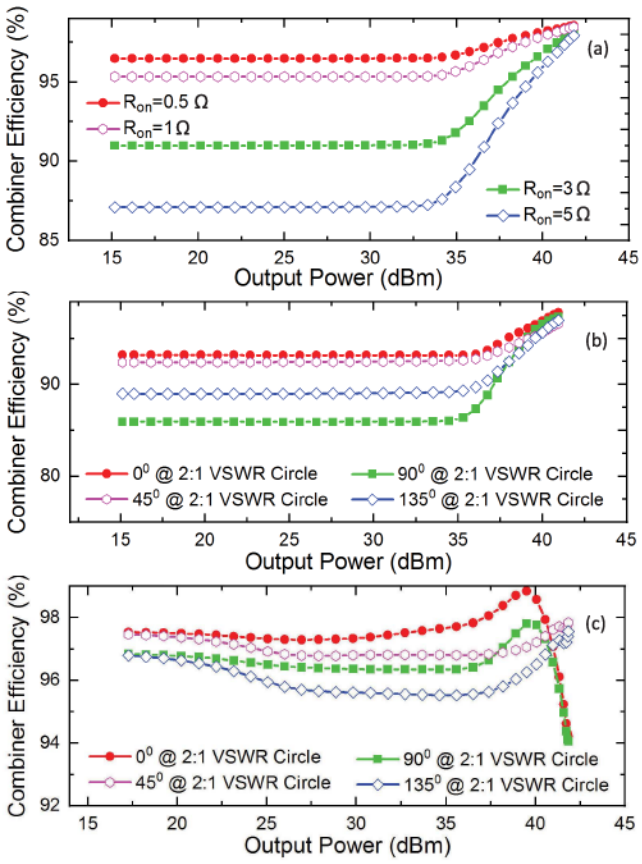

Fig. 10. Investigation on output combiner efficiency (insertion loss). (a) Effect of switch R_{ON} resistance for shorting the isolation port in the Doherty mode. (b) Over 2:1 VSWR circle in the Doherty mode $R_{ON} = 3\ \Omega$. (c) Over 2:1 VSWR circle in the balanced mode.

through the top $\lambda/4$ TL, bypassing the 50-Ω resistor and eventually presenting an open circuit toward the RF output port. However, among commercially available switch devices

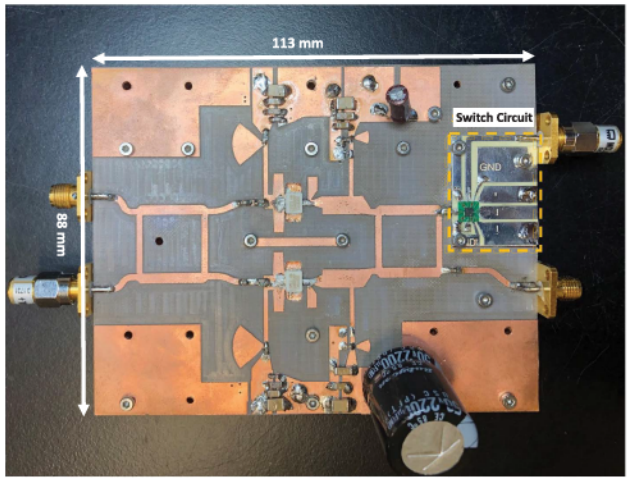

Fig. 11. Top view of the fabricated circuit board.

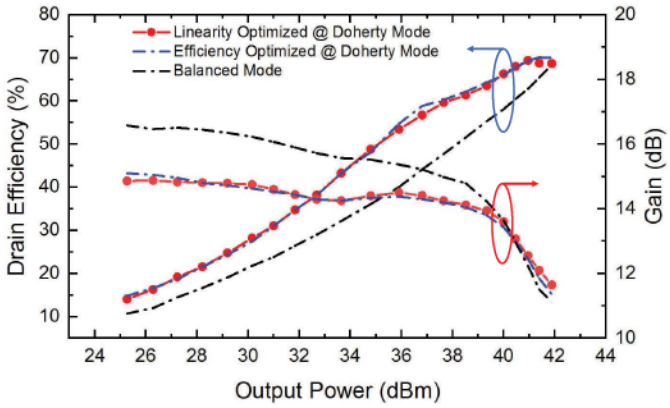

Fig. 12. Measured DE and gain of Doherty and balanced modes.

including MEMS, SOI, and p-i-n diode, such a "pure" open circuit can only be realized using MEMS switch that is not widely available now, and the power handling of MEMS devices is a general concern for high-power applications, especially under high load mismatch.

Therefore, this demonstration design follows the default topology [see Fig. 9(b)] where an SPDT switch is placed at the isolation port to alternately enable connection to the 50-Ω loading and ground. A commercial SOI-based RF switch (SKYA21003) is utilized as the SPDT, which consists of three ports: antenna (ANT), RF1, and RF2. As the switch topology shown in Fig. 9(c), the ANT port is connected to the isolation port of the output coupler, while the RF1 and RF2 ports are terminated to the 50-Ω loading and ground, respectively. Between ANT and RF ports, two switch arms are connected and controlled by a management unit. In the "ON" state, the switch introduces certain series resistance, i.e., R_{ON}. To model this effect, a switch model with 3-Ω R_{ON} is established based on [42], and the switch is cosimulated with the QB-DPA. It is interesting to note that such an R_{ON} does not lead to considerable impact on the QB-DPA performance, as shown in Fig. 7(b). The simulation results verify the feasibility of this default switch design topology. It is interesting to note that, for a typical multithrow SOI switch, there is typically a shunt arm at each switch port,

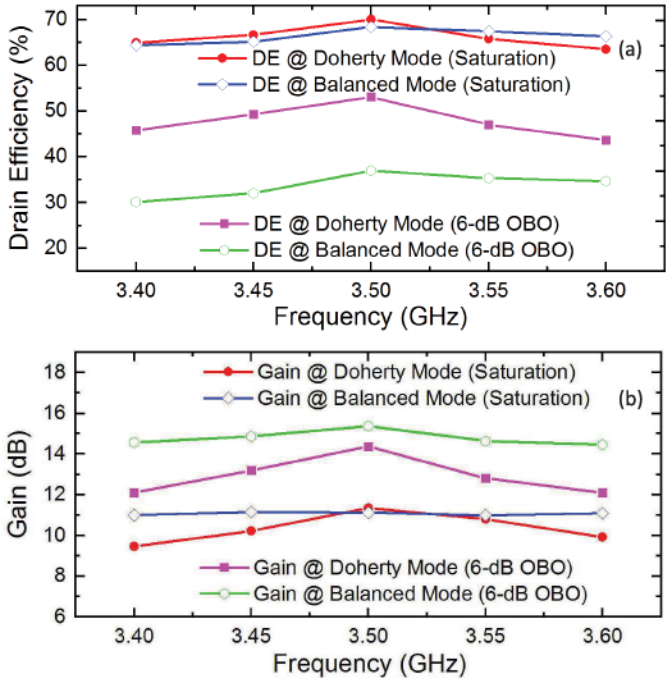

Fig. 13. Measured frequency response of (a) DE and (b) gain at saturation and 6-dB OBO for both Doherty and balanced modes.

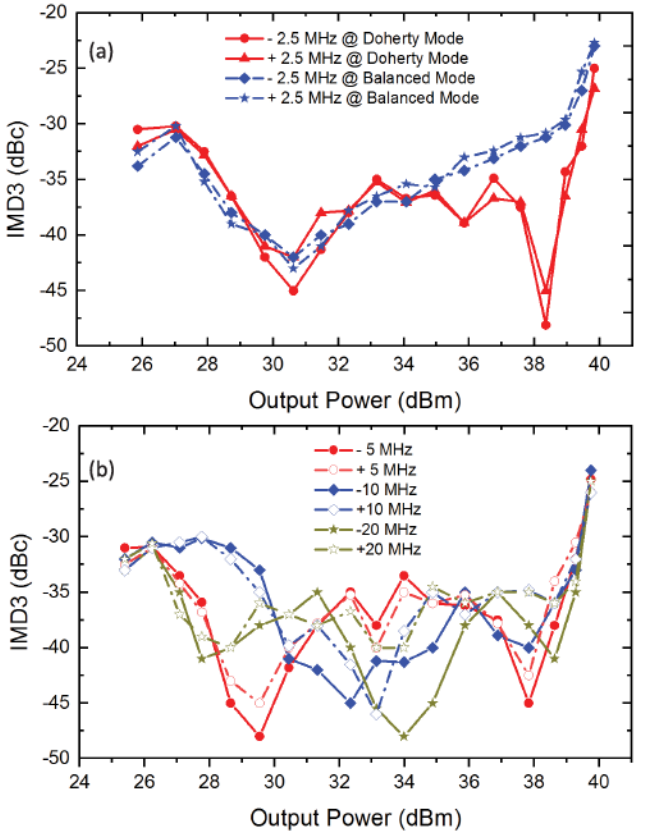

Fig. 14. Two-tone measurement centered at 3.5 GHz. (a) IMD3 of Doherty and balanced modes with 5-MHz tone spacing. (b) IMD3 of Doherty mode with variable tone spacing.

which shorts the node to ground at "OFF" state leading to an improved isolation. Thus, this type of switch cannot offer a complete open circuit at "OFF" state, which cannot be used in the first switchable combiner topology in Fig. 9(a).

The overall insertion loss of the quadrature coupler under the dynamic PA operation is further studied, as shown in Fig. 10. To fully evaluate the switch effect on insertion loss, the combiner loss in the form of passive efficiency is extracted from large-signal harmonic balanced simulation. The passive combiner efficiency versus output power of the Doherty mode is shown in Fig. 10(a). At saturation power, the value of switch R_{ON} has negligible impact on insertion loss since the isolation port is an electrical "null" as mathematically proved in Section II-B. Meanwhile, the increase in R_{ON} leads to higher loss at power back-off. In the mismatch condition as shown in Fig. 10(b) and (c), the balanced mode leads to better combiner efficiency compared with the Doherty mode.

D. Fabrication

The overall layout is generated from circuit schematic, and it is modeled using 3-D electromagnetic simulator. The EM model is then cosimulated with active components, and the layout is optimized until the cosimulation results match the schematic-only case. The fabricated B2D PA is shown in Fig. 11, which is developed on the Rogers 5880 substrate, and the entire PCB is mounted on a copper substrate and fastened using screws. The RF switch module is placed on another small PCB board, and it is mounted on the same copper substrate with RF connection to the isolation node of the output quadrature coupler. By applying different bias settings of the switch control, the ANT port of the SPDT switch can be routed to RF1 (ground) and RF2 (50-Ω termination) alternatively.

V. Measurement Results and Analysis

A. Continuous-Wave Measurement

In the Doherty mode measurement, the gate bias of the main device is primarily set to −2.6 V in Class-AB in order to improve the linearity at low power range. The auxiliary gate bias voltage is set to −4.5 V for linearity-optimized operation. A proper combination of bias setting can generate complimentary nonlinear behaviors of the main and auxiliary amplifiers that cancel each other leading to enhanced linearity of the overall DPA, as reported in [43]. In the balanced mode measurement, the two PAs are identically biased in Class AB with $V_{GS} = -2.5$ V for primarily optimized linearity.

B. Modulated Measurement for Nominal 50-Ω Termination

Fig. 12 shows the measured DE and gain versus the output power at different operation frequencies of the B2D reconfigurable PA, driven by a power-swept continuous-wave (CW) stimulus at the balanced and Doherty modes, respectively. A desired Doherty profile is experimentally obtained in the Doherty mode. The measured gain at a center frequency of 3.5 GHz is around 14 dB at low-power range, and it remains almost flat up to $P_{1\,dB}$. Such an AM–AM behavior ensures a good linearity of the Doherty mode. The efficiency

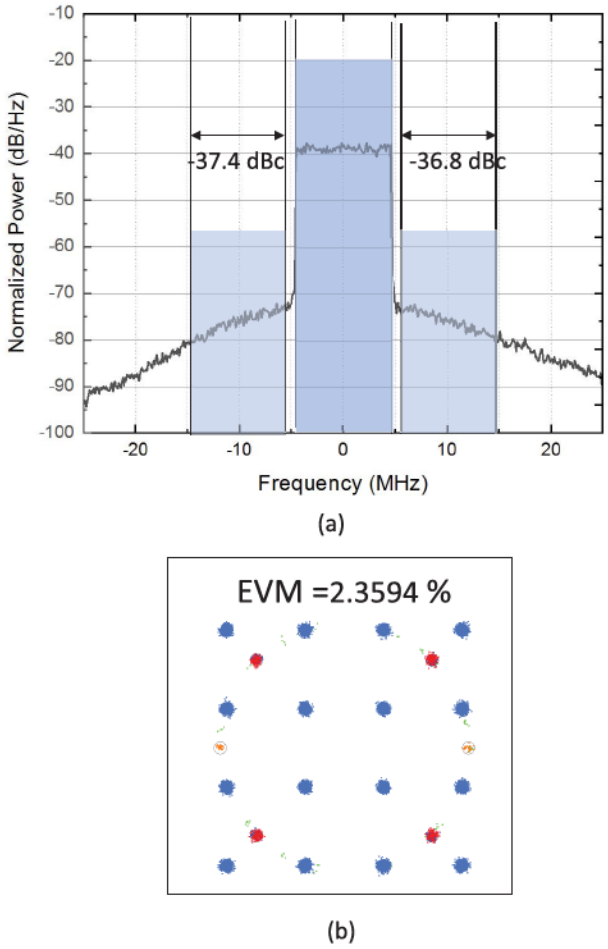

Fig. 15. Measured modulated signal at P_{out} = 34.5 dBm without DPD. (a) Normalized PSD for a 10-MHz LTE signal at 3.5 GHz. (b) 16-QAM constellation diagram corresponding to an efficiency of 42.4%.

and gain of the balanced mode are also plotted in Fig. 12. A higher gain is achieved in the balanced mode, given the fact that there is no turn-off of auxiliary PA wasting half of the input power at low-power region, which also leads to a better backoff-efficiency behavior at the Doherty mode. The measured efficiency at P_{Max} is almost the same for both Doherty and balanced modes at the operating center frequency due to the identical loadline at saturation region. Fig. 13 shows the frequency response of the B2D across 3.4–3.6 GHz. In the Doherty mode, at peak output power, the measured DE is 64%–70% and the gain is 9.5–11.35 dB, whereas, at 6-dB OBO, the measured gain and DE are 12.1–14.4 dB and 46%–55%, respectively. The balanced mode experiences a decent performance in terms of DE and gain as well.

C. Two-Tone Measurement

The third-order intermodulation (IMD3) is measured with two-tone stimulus at a center frequency of 3.5 GHz to evaluate the linearity of the designed B2D PA. Due to the innate characteristic of soft saturation, the balanced mode presents a slight IMD3 degradation compared with the Doherty mode near the saturation region, where the DPA experiences a clear gain expansion (see Fig. 12). Nevertheless, the overall IMD3 of balanced mode remains below −30 dBc with a frequency

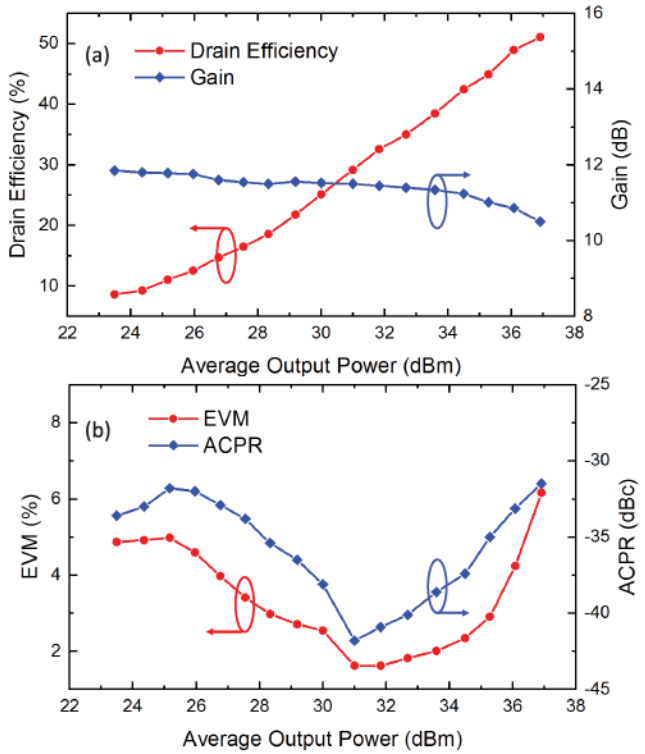

Fig. 16. Measured modulated signal versus average output power. (a) DE and Gain. (b) EVM and ACPR.

spacing of 5 MHz for output power lower than 39 dBm, as shown in Fig. 14(a). Meanwhile, the Doherty mode PA maintains a low IMD3 (i.e., < −35 dBc) across a large power range from saturation to 10-dB back-off, which is crucial to achieve linear amplification of high-PAPR modulated signals. As the frequency spacing increases to 10, 20, and 40 MHz, according to Fig. 14(b), a low IMD3 of Doherty mode is maintained with minimum deviation of lower and upper IMD3 components. This indicates that the memory effect is well suppressed when amplifying high-bandwidth signals.

To evaluate the efficiency and linearity performance of the B2D PA in realistic communication scenarios, a modulated measurement using a long-term evolution (LTE) signal with 10-MHz bandwidth and 8.4-dB PAPR is performed. A Keysight PXIe vector transceiver (VXT M9421) is used as modulated signal generator and analyzer. The generic LTE signal is then boosted by a preamplifier (ZHL-5W-422+) to a sufficient level for driving the PA. The measured power spectral density (PSD) and EVM are presented in Fig. 15(a) and (b), respectively. The designed B2D PA presents an average efficiency of 42.4% and adjacent channel power leakage (ACPR) around −37 dBc at a rated average output power of 34.5 dBm without any DPD applied. A low corresponding EVM of 2.36% is measured in this condition, as shown in Fig. 15(b).

The PA is further tested using a power-swept LTE signal with the same modulation, and the DE and gain versus the average output power are plotted in Fig. 16(a). The profiles of EVM and ACPR are presented as well in Fig. 16(b). It can be seen that the EVM versus P_{out} profile agrees well with the two-tone measurement when tone spacing is at 10 MHz.

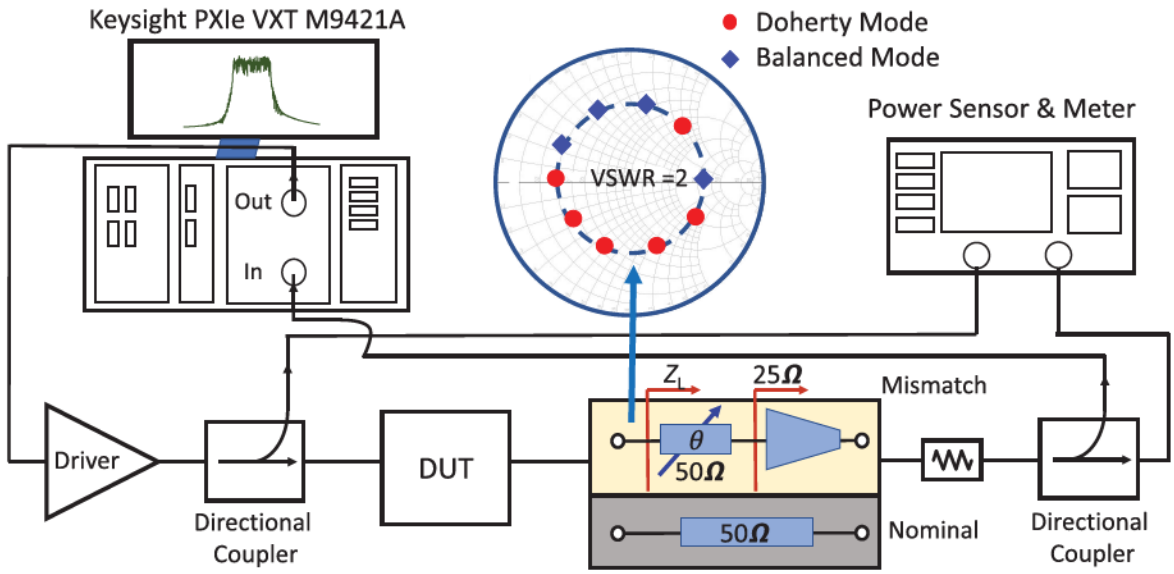

Fig. 17. Illustrative measurement setup for the characterization of the B2D mode-reconfigurable PA under nominal 50-Ω and mismatch (2:1 VSWR) loading conditions. Inset Smith chart presents a system-level operation scenario when the B2D PA switches between the Doherty and balanced modes to maintain the optimized performance over load variation.

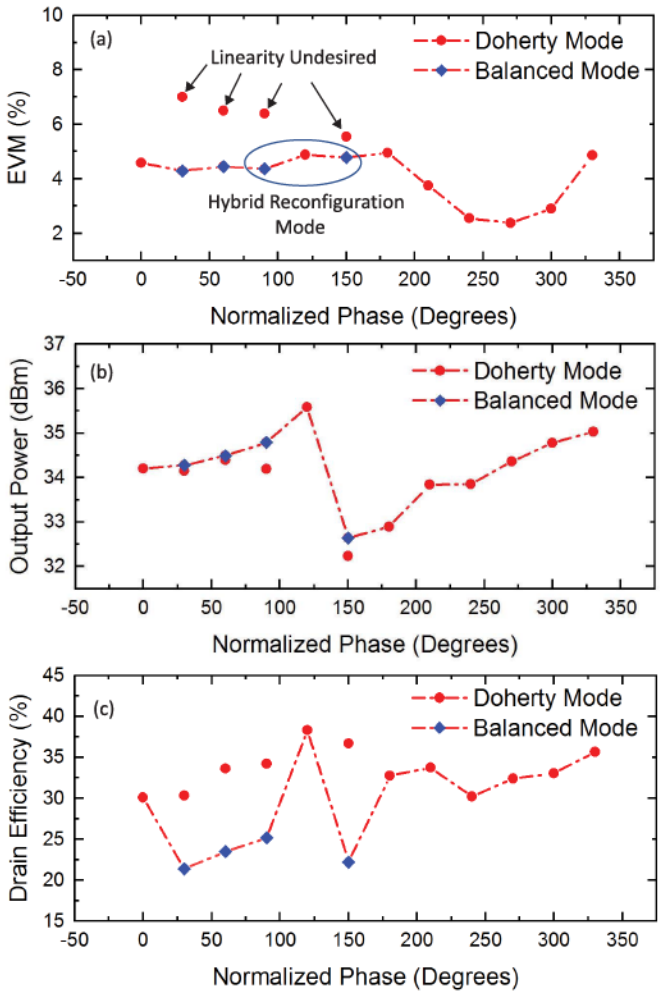

Fig. 18. Measurement of reconfigurable mode B2D PA under 2:1 VSWR over entire phase range. (a) EVM. (b) Output power. (c) Average DE.

Based on the measurement in Fig. 16, the designed Doherty mode PA maintains a low EVM below 3.5% and a raw ACPR between −33.8 and −41.8 dBc over a large power range from 27.5 to 35.6 dBm, while the corresponding average efficiency is between 20% and 45%.

This design exhibits a state-of-the-art PA performance compared with other contemporary linear GaN-based PAs published recently, as listed in Table I. The Doherty mode of the proposed B2D PA offers a very competitive efficiency and linearity at the maximum rated output power, which well verifies the effectiveness of the proposed QB-DPA theory.

D. Reconfigurable Mode Measurement Under Load Mismatch

To experimentally demonstrate the reconfigurable operation, the designed B2D PA is evaluated with the same LTE modulated signal (used in Section V-B) under load mismatch at a constant VSWR of 2:1. Using the measurement system setup in Fig. 17, the PA output is connected to a mismatched load, which covers the 2:1 VSWR circle on Smith chart with the phase swept at 30° step. This is physically realized using a 2:1 transformer in series with a series of transmission lines with different electrical lengths.

The Doherty mode PA is first tested with a constant input driving power of 21 dBm. Fig. 18 shown the EVM, output power, and efficiency versus the varying phase along the 2:1 VSWR circle. In Fig. 18(a), a low EVM ($<5\%$) can be achieved for the majority of phases on the 2:1 VSWR circle with the corresponding output power between $32.5-35.1$ dBm. In this prototype demonstration, a $<5\%$ of EVM is set as the target, while this system benchmark can be redefined according to specific communication standards. For the rest of phases not meeting the linearity spec, the balanced mode is activated through adjusting the control voltage of SPDT to connect RF2 to a 50-Ω load. As shown in Fig. 18(b), the balanced mode recovers the linearity of those phases, exhibiting a $<5\%$ EVM with a slightly higher maximum linear power compared with the Doherty mode. In terms of the efficiency performance presented in Fig. 18(c), the efficiency of Doherty mode slightly degrades compared

TABLE I
COMPARISON WITH STATE-OF-THE-ART OF RECENTLY REPORTED LINEAR GAN PAS

Ref.	f_0 (GHz)	Architecture	Technology	P_{avg} (dBm)	Mod. BW (MHz)	Average DE (%)	ACPR w/o DPD (dBc)
[22]	5	2-Way Doherty	GaN/Hybrid	32	40/80/120	42	−43.8/ − 44.1/ − 43.1
[23]	0.8	DPA w Linearizer	GaN/Hybrid	33	20/30/40	33.2/30.9/29.6	−42.5/ − 42.3/ − 40.7
[24]	2.14	2-Way Doherty	GaN/Hybrid	35.5	5/10/20	44	−41.5/ − 40.8/ − 40.5
[44]	7	2-Way Doherty	GaN/MMIC	32	56	41	−36
[45]	2.3	2-Way Doherty	GaN/MMIC	35.2	10	46	−35.6
[46]	3.5	2-Way Doherty	GaN/Hybrid	35.8	20	62	−27.9
[47]†	5	2-Way Doherty	GaN/Hybrid	36	5	57.8*	−30
[48]	2.0	2-Way Doherty	GaN/Hybrid	33	5	54	−30
[2]	7	2-Way Doherty	GaN/MMIC	27.7	20	43	−41
This Work	3.5	B2D PA**	GaN/Hybrid	34.5	10	42.4	−37

† Measured using two-tone signal with 5-MHz tone spacing. ∗ Maximum CW PAE at an IMD3 of -30 dBc.
∗∗ QB-DPA mode.

to nominal 50-Ω condition, while the efficiency is further compromised for linearity when reconfigured to balanced mode. It is important to point out that a failure in linearity usually overwhelms the failure of a communication link so that a slight compromise of efficiency can be well justified for ensuring the overall quality of service (QoS).

In summary, when a practical transmitter system is subject to antenna mismatch, this B2D mode reconfiguration is able to maintain a high PA linearity consistently complying with the particular communication standard while maintaining a stable output power and decent efficiency. More importantly, this mode reconfiguration can be seamlessly implemented without having to physically detect the actual mismatch impedance. This feature is expected to be highly desirable for MIMO and active array applications where the antenna impedance variation is anticipated to be in very rapid time-scale.

VI. CONCLUSION

In this article, a novel B2D mode-reconfigurable PA is proposed and analyzed, which is targeted to maintain high linearity and high efficiency overcoming the load mismatch. It is for the first time theoretically derived that a QB-DPA mode can function equivalently to a standard DPA. Moreover, with an SOI-based SPDT switch, a reconfigurable B2D PA prototype is implemented to verify the proposed concept at 3.5 GHz. In the nominal case where the B2D PA is driven by an LTE modulated signal with 10-MHz bandwidth, the measured PA exhibits −37-dBc ACPR, allowing it to achieve 2.36% EVM at the maximum $P_{rated} = 34.5$ dBm without any additional linearization techniques. Meanwhile, when suffering from the load mismatch, the designed B2D PA also demonstrates its resilience and capability of maintaining high linearity and high efficiency over entire Smith chart at VSWR 2 : 1. It is worth mentioning that this switchable B2D PA shows promising potential to extend to broadband implementations due to naturally bandwidth-friendly feature of balanced PA. Furthermore, the unique characteristic of the seamless reconfigurable operation when handling rapid load mismatch makes the proposed technique very suitable for use in the 5G micro cell and compatible with MIMO antennas and active antenna arrays.

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