A 100 kW SiC Switched Tank Converter for Transportation Electrification

Ze Ni, *Student Member, IEEE*, Yanchao Li, *Student Member, IEEE*, Chengkun Liu, *Student Member, IEEE*, Mengxuan Wei, *Student Member, IEEE*, and Dong Cao, *Member, IEEE*

***Abstract*- This paper presents a 100 kW switched tank converter (STC) using SiC MOSFETs for transportation power electronic systems. This bidirectional dc-dc converter targets 300 V - 600 V voltage conversion. Total semiconductor loss index (TSLI) has been proposed to evaluate topology and device technologies. The boost converter and one-cell STC have been fairly compared by utilizing this index. The detailed STC design procedures including SiC MOSFET, heatsink, resonant tank components, and DC capacitors are explained in detail. The simulation results of a 100 kW one-cell STC working at zero current switching (ZCS) mode have been provided. A 100 kW 1st generation hardware prototype using 1200 V 600 A SiC power module has been built and tested. The power density of the main circuits is about 42 kW/L. The desirable thermal performance of the hardware prototype is demonstrated, which is consistent with the theoretical design. The measured efficiency reaches peak 98.7% at around 30 kW, and is about 98.5% at 50 kW, 97.4% at 100 kW full load.**

***Indexed Terms*—dc-dc converter, SiC MOSFET, switched tank converter, zero current switching, transportation electrification, total semiconductor loss index (TSLI).**

I. INTRODUCTION

High power dc-dc converters have been widely applied in multiple transportation electrification areas such as aeronautical power distribution systems [1]–[3], electric ship power networks [4][5], and electric vehicles [6]. In aerospace secondary power distribution networks, the dc-dc converters are needed to interface the battery and the DC bus [7]. It provides the desired voltage for different load requirements [1][7]. For the marine vessels, the dc-dc converters also play an essential part in the integrated power systems in the propulsion units [8]–[11]. The shipboard DC power systems promote more energy saving compared with the conventional AC systems by adjusting the motors to work at an optimal speed [8]. In hybrid electric vehicle power trains, a bidirectional dc-dc converter is normally used to boost the battery voltage to a higher DC bus voltage to drive the high voltage electric motors or generators using a 3-phase voltage source inverter [12]–[14]. Typical voltage requirements of such a dc-dc converter are 300 V on the battery side and 650 V on DC bus side [15]. It aims to regulate the bus voltage, protect the battery from over/under voltage, excessive charge/discharge currents [15]–[17]. In a recent report of U.S. Department of Energy [6], by 2025, the electric traction drive system cost is expected to be lower than $2.7/kW, and the power density is supposed to exceed 100 kW/L based on the 100 kW power level. To achieve this goal, a proper topology with optimized device and passive component design should be deliberated and experimentally verified.

Conventional bidirectional boost/buck converter is a basic solution for such applications. A 40 kW bidirectional dc-dc converter based on boost topology is designed in [18] with 6 kW/L power density working at 20 kHz switching frequency. However, conventional boost converter suffers from low efficiency and bulky reactive components. To reduce the input and output capacitor size, a 3-phase interleaved boost converter with discrete inductors is assembled to achieve a power density of 30.8 kW/L and 97.9% peak efficiency [19]. But the total inductor core volume is about 1.3 Liters, which is very bulky. To overcome this issue, constant frequency quasi square wave zero voltage switching (ZVS) 3-phase interleaved boost converter is studied in [20]. But it is inefficient at light load. Variable-frequency boundary mode quasi square wave ZVS control is applied in a 200 kW Si IGBT based prototype [15] to further increase the peak efficiency to 98%, but the power density is only 6 kW/L. Besides, ZVS is realized to improve the efficiency based on a 150 kW, 8.6 L interleaved boost dc-dc converter with multiple split DC sources, but the power density is 17.44 kW/L [21]. Another widely investigated topology for this application is flying capacitor multilevel converter (FCMC) [22]–[25]. To increase the voltage conversion flexibility, an inductor is placed on the DC input side [12][26]. Over 97% efficiency at 30 kW continuous operation is claimed in [12] by using FCMC with a power density around 8.612 kW/L. However, it is difficult to realize a compact mechanical layout design considering the separate locations of the DC-side resonant inductor and AC-side resonant capacitor. SiC MOSFET power modules have shown better efficiency and higher temperature capability compared with the Si counterparts [27]–[30]. 1200 V 100 A SiC MOSFET power modules have been applied in a boost based 60 kW dc-dc converter, which can achieve 20 kW/L power density [31]. However, hard-switching operation at 75 kHz switching frequency doesn't fully utilize their advantages, which degrades the overall 98.7% peak efficiency. Recently, resonant multilevel dc-dc converters, resonant switched capacitor converters, and switched tank converters are investigated for their modularity, high power density and high efficiency

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Z. Ni is with the Electrical and Computer Engineering Department, North Dakota State University, Fargo, ND, 58108 (email: ze.ni@ndsu.edu). Y. Li is with AZ Power. Inc, Culver City, CA, 90230. (email: yanchao.li@ndsu.edu) C. Liu, M. Wei, and D. Cao are with the Electrical and Computer Engineering Department, University of Dayton, Dayton, OH, 45469. (emails: liuc30@udayton.edu, weim06@udayton.edu, dcao02@udayton.edu)

[25][32]–[37]. But the high power applications of these topologies have not been well explored.

Since different topologies use different voltage rating devices, it is difficult to compare the semiconductor die area usage among topologies. Relative total semiconductor chip area is introduced in [38], but it does not consider the relationship between total die area and the device power loss. Total switching device power is defined in [39] using the product of switch voltage and current stresses as the evaluation method. But it cannot indicate the optimized die area requirement for different topology designs. Dr. B. Jayant Baliga proposed a device-level index called figure of merit in [40], but it fails to evaluate the total device power loss among different topologies by using only on-resistance and the total gate charge.

This paper presents a switched tank converter (STC) for the 100 kW transportation electrification applications. It has the modular structure only utilizing low voltage and low current rating devices to achieve high voltage, high current, and high conversion ratio application. It can achieve soft switching strategies including ZCS [32][41][42] and ZVS [43] to minimize the switching losses with the help of the resonant tank design and appropriate control methods. High switching frequency could be adopted to minimize the resonant components' size. The low on-resistance feature of SiC MOSFET can be fully leveraged. In different electric vehicle applications, various voltage transfer ratios may be desired, which means different number of cells should be used for the proposed STC topology. For the specific application in this paper, i.e. 300 V – 600 V conversion, only one cell of the generalized STC structure is needed. Moreover, if the voltage regulation is expected in some applications, the ZVS control could be used to realize this function [35][44]. Another derivative STC topology could also regulate voltage with minimum efforts. This STC is integrated with a partial power processed voltage regulator [37]. It could achieve high voltage conversion ratio using multiple STC cells and achieve full voltage regulation without ZVS. This paper will focus on the one-cell STC for the 300 V – 600 V 100 kW vehicle application.

Although only 650 V SiC device is needed for such application, due to the high-current SiC module availability, 1200 V SiC power modules are selected for the hardware prototype design. In order to overcome the previous mentioned issue of comparing topologies with different device voltage rating, this paper proposes the total semiconductor loss index (TSLI) as the topology evaluation method. It tries to generate the relationship between the converter total semiconductor die area and the total device power loss. Different topologies could achieve similar power loss at their own optimization points with different semiconductor die area. The semiconductor die area has a direct relationship with the manufacturing costs. Thus, a customized die area usage for a converter with specific electrical parameters helps optimize the efficiency with reasonable device manufacturing costs. Therefore, a relatively fair total semiconductor power loss comparison assuming the same die area usage is important. It provides a more comprehensive understanding about which topology can achieve the lower power loss with the same die area usage.

Compared with the state-of-art high-power dc-dc converter research, this paper endeavors to apply a new topology derived from resonant switched capacitor concept and introduces a new evaluation index to compare potential topology candidates in terms of the device power loss and chip die area. High-power design challenges of both the active switches and passive components are analyzed. The corresponding solutions are provided in detail. A 100 kW hardware prototype using the proposed topology achieving 98.7% efficiency and 42 kW/L power density has been developed and tested. The circuit operation, component design procedure as well as hardware prototype experimental results will be presented in this paper.

II. Circuit Structure and Operation Principle

Fig. 1 shows the proposed generalized *N*-cell STC. Each cell can be considered as a four-terminal two-port network with two terminals on the input port and two terminals on the output port. All the cells share the same input and output port voltage. In the generalized *N*-cell STC architecture, *N* input ports are connected in parallel and N output ports are connected in series, while the bottom terminal of the output port in the 1st cell is connected with the top terminal of the input port, as shown in Fig. 1. As a result, the output voltage is (*N*+1) times V_{in}. A voltage transfer ratio of 1:(*N*+1) can be realized in a *N*-cell STC topology. The proposed topology can also provide opposite current flow when the input and output terminals are reversed.

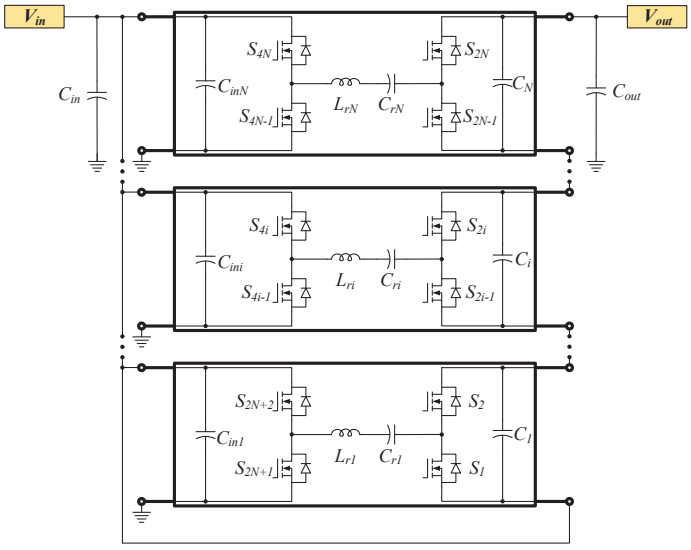


Fig. 1: Generalized *N*-cell STC topology with voltage transfer ratio 1:(*N*+1)

Each cell of the proposed STC is composed of two half-bridges, one resonant tank and two clamping capacitors on both the input and output sides. All the switch voltage stress of the proposed STC is equal to the low side voltage, which makes it more suitable for higher voltage applications. Recently published STCs [32][41][42] have some switches with voltage stress twice of the low side voltage, which are more suitable for the low voltage applications, e.g. 48 V – 12 V, where the 25 V and 40 V devices can be utilized. However, for the high voltage applications, the devices with voltage rating twice of the input voltage might not be available. The proposed STC could utilize all low voltage devices to achieve the high output voltage, e.g. 300 V – 1200 V utilizing the 650 V GaN HEMTs. The resonant

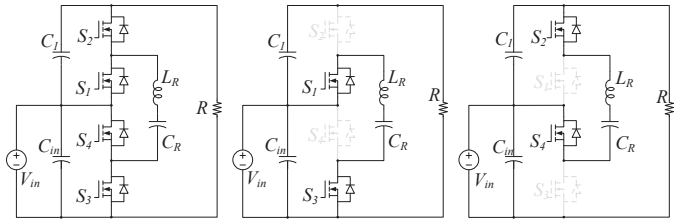
tank of the cell #i's capacitor C_{ri} DC bias voltage equals to i times V_{in}. The inductor L_{ri} has pure AC current. Thanks to the clamping of the capacitor C_i in each cell, the drain-source voltage stress of the switches is clamped to the low side voltage. For the current stress evaluation, from the switch current I_S in Eq. (1), the switch average current $I_{S(AVG)}$ is shown in Eq. (2) [45], which is $1/\pi$ of the switch peak current $I_{S(PK)}$.

In this N-cell generalized STC topology, the average switch current $I_{S(AVG)}$ is equal to the current on the low-current side. The current stress is π times the current on the low-current side. The detailed operation principles of the N-cell STC have been published in [37]. This paper will focus on the one-cell STC.

$$I_S = \begin{cases} I_{S(PK)} \cdot \sin \omega t & 0 \le t \le (T_S/2) \\ 0 & (T_S/2) < t \le T_S \end{cases} \quad (1)$$

$$I_{S(AVG)} = \frac{1}{T_S}\int_0^{\frac{T_S}{2}} I_{S(PK)} \cdot \sin(\omega t)dt = \frac{I_{S(PK)}}{\pi} \quad (2)$$

In order to validate the proposed topology for high voltage high power application, a 100 kW one-cell STC has been designed, developed and tested. Fig. 2(a) shows the utilized one-cell STC topology for the 100 kW 300 V – 600 V application. This topology has been briefly mentioned in [33], but the soft switching operation principles have not been illustrated in detail. There are two main switching modes of this STC operating at ZCS. When S_1 and S_3 are ON, the switching mode I is presented in Fig. 2(b). The resonant capacitor C_R is charged and resonant inductor L_R stores energy. When S_2 and S_4 are ON, the resonant capacitor C_R discharges together with the input voltage source in the switching mode II as presented in Fig. 2(c). The resonant inductor L_R releases energy in this mode.



(a) One-cell STC (b) Switching mode I (c) Switching mode II

Fig. 2: One-cell STC and equivalent circuits of the two switching modes

Fig. 3 presents the ideal operating waveforms of this topology. In switching mode I, C_1 keeps releasing energy to the load. C_{in} releases the energy most of the time. In switching mode II, C_1 stores energy most of the time. C_{in} keeps storing energy. According to the analysis in the generalized N-cell STC topology, the voltage transfer ratio is 2 in this one-cell STC circuit. As a result, a voltage doubler is achieved.

III. Total Semiconductor Loss Index (TSLI)

Different topologies use devices with various voltage ratings and operate at their own optimized output power. As investigated above, multiple topologies such as boost converter, FCMC could achieve relatively high efficiency by selecting specific semiconductor die areas at the same power rating. But different from the traditional boost converter, the FCMC and STC topologies utilize the devices with lower voltage rating. Thus, how to evaluate these topologies needs to be deliberated. A new evaluation index called total semiconductor loss index

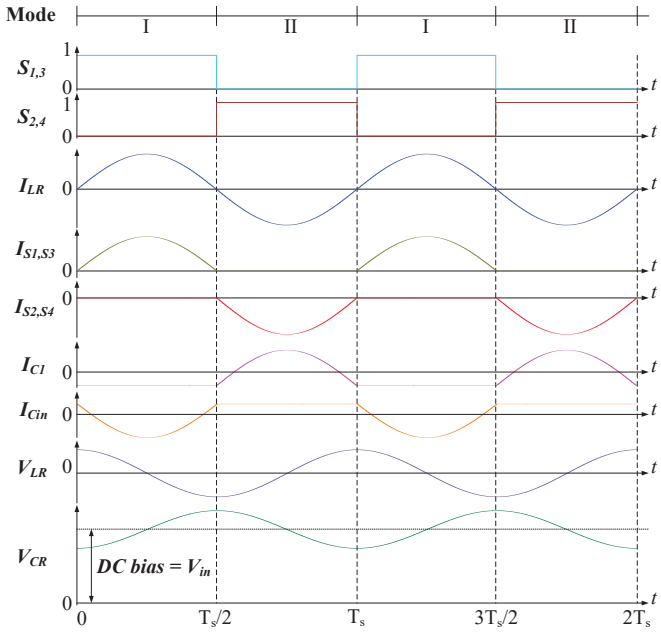


Fig. 3: Theoretical waveforms of the one-cell switched tank converter

(TSLI) is proposed to relate the device power loss with the total die area usage so that minimal device power loss with an optimized die area can be achieved.

The product of on-resistance $R_{ds(on)}$ and die area A_{die} , called specific on-resistance has been regarded as an index to reflect the device technologies [46]–[51]. By taking Cree/Wolfspeed® SiC MOSFET die for example, the $R_{ds(on)}{\cdot}A_{die}$ versus breakdown voltage V_B and the junction temperature T_j is plotted in Fig. 4. It can not only reflect that the specific on-resistance decreases with the voltage rating reduction, but also show the junction temperature's positive impact on the specific on-resistance. The FCMC and STC topologies utilize the devices with lower voltage rating to achieve smaller specific on-resistance, which indicates lower conduction loss and smaller die area. However, the device number increases with extended modules, which dwarfs these advantages. Therefore, by evaluating the total semiconductor die area usage, the topology-level specific on-resistance can reflect the impact of different chip technologies on the device conduction loss among various topologies.

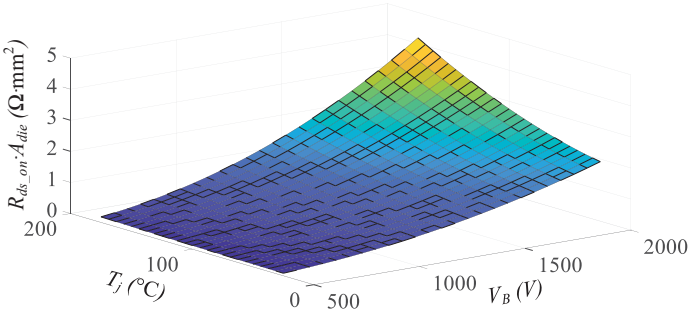


Fig. 4: Specific on-resistance vs. breakdown voltage and junction temperature (Take Cree/Wolfspeed® SiC MOSFET die for example)

Basically, the relationship between $R_{ds(on)}{\cdot}A_{die}$ and V_B can be represented by using the on-resistance technology function $\alpha(\xi, V_B)$ in Eq. (3) [46]–[51]. It is derived from the theoretical SiC $R_{ds(on)}{\cdot}A_{die}$ versus V_B curves and the product information.

$$R_{ds(on)} \cdot A_{die} = \alpha(\xi, V_B) = \xi \cdot (V_B)^X \quad (3)$$

where, ξ is the constant dependent on semiconductor manufacturing technologies. X is an exponent close to 2. The theoretical SiC limit $\alpha_{SiC}(\xi, V_B)$ is presented in Eq. (4).

$$\alpha_{SiC}(\xi, V_B) = 4\times10^{-8} \cdot (V_B)^{1.988} \quad (4)$$

The on-resistance technology function is represented as $\alpha_1(\xi, V_B)$ in Eq. (5) for SiC MOSFETs from Rohm and $\alpha_2(\xi, V_B)$ in Eq. (6) for those from Cree, based on the curve fitting results.

$$\alpha_1(\xi, V_B) = 3.984\times10^{-7} \cdot (V_B)^2 \quad (5)$$

$$\alpha_2(\xi, V_B) = 6\times10^{-8} \cdot (V_B)^{2.2735} \quad (6)$$

With different companies' semiconductor technology, the on-resistance technology function $\alpha(\xi, V_B)$ varies. Therefore, the device $R_{ds(on)}$ could be represented by Eq. (7).

$$R_{ds(on)} = \alpha(\xi, V_B)/A_{die} \quad (7)$$

In this way, the total device conduction loss P_{cond} and the device die area usage A_{die} can be correlated by using Eq. (8).

$$P_{cond} = \left(I_{RMS\_S}\right)^2 \cdot R_{ds(on)} = \left(I_{RMS\_S}\right)^2 \cdot \frac{\alpha(\xi, V_B)}{A_{die}} \quad (8)$$

where, I_{RMS_S} is the switch RMS current. When N devices are used, the total conduction loss function versus total semiconductor die area usage could be described in Eq. (9).

$$P_{cond}(A_{die\_t}) = \sum_{i=1}^{N}\left(\left(I_{RMS\_S(i)}\right)^2 \cdot \frac{\alpha_i(\xi_i, V_{B(i)})}{\kappa_i A_{die\_t}}\right) \quad (9)$$

where, κ_i is the die cutting factor ranging from 0 to 1, reflecting different die cutting strategies. The sum of each κ_i equals to 1. For the one-cell STC with four identical switches, $\kappa_1 = \kappa_2 = \kappa_3 = \kappa_4 = 0.25$. A_{die_t} is total die area of the converter devices. It can be used to compare the total conduction loss versus total die area usage. Since the blocking voltage information is included in this function, it can be also applied to evaluate the topologies with different device voltage stresses. This conduction loss function is normalized in Eq. (10).

$$P^*_{cond}(A_{die\_t}) = \frac{1}{P_o}\sum_{i=1}^{N}\left(\left(I_{RMS\_S(i)}\right)^2 \cdot \frac{\alpha_i(\xi_i, V_{B(i)})}{\kappa_i A_{die\_t}}\right) \quad (10)$$

Similarly, the normalized gate drive power loss, switching loss can be derived. When the die area is enlarged, the input capacitance increases [52]. Larger gate current is needed to charge the input capacitor. So, the total gate charge induced switching loss increases. The gate drive loss is in Eq. (11) [53].

$$P_{Gate} = Q_g \cdot \Delta V_{gs} \cdot f_s \;\; ; \;\; \beta = Q_g / A_{die} \quad (11)$$

where, Q_g is the total gate charge. ΔV_{gs} is the difference of the recommended maximum and minimum V_{gs} ratings. f_s is switching frequency. β is the device total gate charge per unit die area. The total normalized gate drive loss is in Eq. (12).

$$P^*_{Gate}(A_{die\_t}) = \frac{1}{P_o}\sum_{i=1}^{N}\left(\beta_i \cdot \kappa_i \cdot A_{die\_t} \cdot \Delta V_{gs(i)} \cdot f_{s(i)}\right) \quad (12)$$

Generalized turn-on and turn-off switching losses are derived in a similar manner in Eq. (13), (14), respectively.

$$P_{on} = E_{on} \cdot f_s \;;\; \delta = E_{on}/A_{die} \quad (13)$$

$$P_{off} = E_{off} \cdot f_s \;;\; \sigma = E_{off}/A_{die} \quad (14)$$

where, P_{on}, P_{off} are turn-on and turn-off power losses. E_{on} E_{off} are turn-on and turn-off energy. δ and σ are turn-on and turn-off energy per unit die area. The normalized turn-on and turn-off switching losses are in Eq. (15) and (16), respectively.

$$P^*_{on}(A_{die\_t}) = \frac{1}{P_o}\sum_{i=1}^{N}\left(\delta_i \cdot \kappa_i \cdot A_{die\_t} \cdot f_{s(i)}\right) \quad (15)$$

$$P^*_{off}(A_{die\_t}) = \frac{1}{P_o}\sum_{i=1}^{N}\left(\sigma_i \cdot \kappa_i \cdot A_{die\_t} \cdot f_{s(i)}\right) \quad (16)$$

In the ZCS case, the output capacitance C_{oss} discharge induced turn-on switching loss is considered. The gate-drain capacitance C_{gd} and drain-source capacitance C_{ds} increase with the die area [54][55]. Thus, C_{oss} (i.e. $C_{gd} + C_{ds}$) loss is positively dependent on die area. This turn-on switching loss is in Eq. (17) [56]. The corresponding normalized equation is in Eq. (18).

$$P_{C_{oss}} = C_{oss} \cdot {V_{ds}}^2 \cdot f_s \;\; ; \;\; \gamma = C_{oss}/A_{die} \quad (17)$$

$$P^*_{C_{oss}}(A_{die\_t}) = \frac{1}{P_o}\sum_{i=1}^{N}\left(\gamma_i \cdot \kappa_i \cdot A_{die\_t} \cdot {V_{ds(i)}}^2 \cdot f_{s(i)}\right) \quad (18)$$

where, V_{ds} is drain-source voltage. γ_i is the device output capacitance per unit die area, which is dependent on the device semiconductor manufacturing technologies.

The semiconductor device is the major cost contributor of a power converter. Since the semiconductor cost is proportional to total semiconductor die area usage, it is useful to identify the topology that can achieve the minimal power loss with the minimal semiconductor die usage. On the one hand, with the increase of the total device die area, the total device conduction loss reduces. On the other hand, the increased die area leads to larger parasitic capacitance, which causes higher switching loss and gate drive loss. So, the optimized total device die area exists to minimize total converter semiconductor power loss.

Therefore, in this paper, we propose total semiconductor loss index (TSLI), which is the normalized total semiconductor power loss as a function of total semiconductor die area. It can be used as a tool to evaluate the total device power loss in terms of total die area usage among different topologies and devices.

TSLI can be derived by summarizing the previous presented normalized power losses in Eq. (19).

$$TSLI(A_{die\_t}) = P^*_{cond}(A_{die\_t}) + P^*_{Gate}(A_{die\_t}) + P^*_{sw}(A_{die\_t}) \quad (19)$$

When hard-switching is applied, $P_{sw}{}^*$ is the sum of $P_{on}{}^*$ and $P_{off}{}^*$. When ZCS is utilized, $P_{sw}{}^*$ is equal to $P_{Coss}{}^*$. For a specific topology, when the output power and switching frequency are fixed, theoretically an optimal die area for each switch can be derived to achieve the minimized total device power loss. In other words, when the total device power loss is the same, the one with smaller total die area can achieve lower device manufacturing costs. These two evaluation perspectives based on the above TSLI parameter provide comprehensive understandings to compare different topologies and devices.

IV. Topology Comparison

Through investigating SiC MOSFETs with three different voltage ratings from two device companies, the proposed TSLI of the boost converter and the one-cell STC is compared.

For boost converter, 1200 V SiC devices are applied, since the device voltage stress is 600 V. Two SiC dies with 1200 V voltage ratings, i.e. Rohm S4103 [57] and Cree CPM2-1200-0025B [58] are selected. The device turn-on and turn-off losses are considered at continuous conduction mode assuming the inductor current ripple is 30% of its average current [59].

For the boost converter with two identical switches, the die cutting factors $\kappa_1 = \kappa_2 = 0.5$. From Eq. (10), normalized conduction loss of the boost converter is presented in Eq. (20).

$$P^*_{cond(B)}(A_{die\_t}) = \frac{2}{P_o}\left(I_{RMS\_S(B)}\right)^2 \cdot \frac{R_{ds(on)} \cdot A_{die}}{0.5 \cdot A_{die\_t}} \quad (20)$$

where, the subscript B represents boost converter. $I_{RMS\_S(B)}$ is device RMS current, which is 236.58 A in this application.

From Eq. (12), the normalized gate drive loss function of the boost converter can be described in Eq. (21).

$$P^*_{Gate(B)}(A_{die\_t}) = \frac{2}{P_o}\left(\frac{Q_g}{A_{die}} \cdot 0.5 \cdot A_{die\_t} \cdot \Delta V_{gs} \cdot f_s\right) \quad (21)$$

For Rohm's S4103 and Cree's CPM2-1200-0025B, ΔV_{gs} is 18 V and 25 V, respectively. f_s is 100 kHz.

From Eq. (15), (16), the normalized turn-on, turn-off loss functions for boost converter are in Eq. (22), (23), respectively.

$$P^*_{on(B)}(A_{die\_t}) = \frac{2}{P_o}\left(\frac{E_{on}}{A_{die}} \cdot 0.5 \cdot A_{die\_t} \cdot f_s\right) \quad (22)$$

$$P^*_{off(B)}(A_{die\_t}) = \frac{2}{P_o}\left(\frac{E_{off}}{A_{die}} \cdot 0.5 \cdot A_{die\_t} \cdot f_s\right) \quad (23)$$

The switching energy versus drain current curves of the two selected SiC bare dies can be found in the datasheets of Rohm 1200V SCT3022KL and Cree 1200V C2M0025120D SiC MOSFETs due to the matched on-resistance and current rating between the bare die and the corresponding device.

TSLI of the boost converter is the sum of the above four individual semiconductor loss indexes, as shown in Eq. (24).

$$TSLI_B(A_{die\_t}) = P^*_{cond(B)} + P^*_{Gate(B)} + P^*_{on(B)} + P^*_{off(B)} \quad (24)$$

One-cell STC is designed to operate at ZCS mode in this paper. C_{oss} discharge induced turn-on loss is included in the switching loss. In 300 V – 600 V application, 650 V, 900 V and 1200 V devices can be used. For the four identical switches, the die cutting factors $\kappa_1 = \kappa_2 = \kappa_3 = \kappa_4 = 0.25$. Similarly, based on Eq. (10), (12) and (18), the normalized conduction loss function, gate drive loss function and C_{oss} loss function of the one-cell STC are in Eq. (25), (26) and (27), respectively.

$$P^*_{cond(STC)}(A_{die\_t}) = \frac{4}{P_o}\left(I_{RMS\_S(STC)}\right)^2 \cdot \frac{R_{ds(on)} \cdot A_{die}}{0.25 \cdot A_{die\_t}} \quad (25)$$

where, $I_{RMS\_S(STC)}$ is the device RMS value of the one-cell STC, which is 261.8 A at full load.

$$P^*_{Gate(STC)}(A_{die\_t}) = \frac{4}{P_o}\left(\frac{Q_g}{A_{die}} \cdot 0.25 \cdot A_{die\_t} \cdot \Delta V_{gs} \cdot f_s\right) \quad (26)$$

For Rohm's 650 V S4003 and Cree's 900 V CPM3-0900-0010A, ΔV_{gs} is 18 V and 19 V, respectively.

$$P^*_{C_{oss}}(A_{die\_t}) = \frac{4}{P_o}\left(\frac{C_{oss}}{A_{die}} \cdot 0.25 \cdot A_{die\_t} \cdot V_{ds}^2 \cdot f_s\right) \quad (27)$$

where, C_{oss} is 148 pF and 350 pF for Rohm's S4003 and Cree's CPM3-0900-0010A, respectively. V_{ds} is the device voltage stress, which is 300 V in this application.

TSLI for the proposed one-cell STC is in Eq. (28).

$$TSLI_{STC}(A_{die\_t}) = P^*_{cond(STC)} + P^*_{Gate(STC)} + P^*_{C_{oss}(STC)} \quad (28)$$

The TSLIs of the boost converter and one-cell STC for the selected SiC bare dies with different voltage rating are plotted in Fig. 5 for a comprehensive comparison. Although various devices could reach the same level of power loss with different total semiconductor die areas, one-cell STC with 900 V Cree SiC bare die utilizes the minimal die area, which indicates lower die manufacturing costs. Compared with boost converter, one-cell STC can achieve lower total semiconductor loss with the same die area usage. In other words, at the same total device loss, one-cell STC consumes smaller total die area.

V. Design of Devices and Passive Components

The detailed component design is presented in this section. Part A talks about the design of SiC MOSFET power modules. Part B presents the heatsink design process. Part C discusses details regarding the resonant capacitor design. Detailed resonant capacitor design criteria is provided in Part C. The high current, high frequency resonant inductor design is also a major challenge to achieve the minimal size and power loss. The optimal considerations of the resonant inductor winding and core designs are analyzed in Part D. The DC capacitor design is discussed in detail in Part E.

A. Design of Devices

The challenges for the device design in the high-power applications are mainly caused by the high conduction power loss and potentially high die temperature rise. To respond to these challenges, both the optimized device power loss and temperature rise are to be achieved in a wide load range.

Based on the TSLI evaluation in Fig. 5, 900 V Cree and 650 V Rohm SiC MOSFET achieve lower semiconductor power loss. However, the SiC MOSFET products based on 900 V Cree die and 650 V Rohm die have limited current capability. As a result, multiple paralleled devices are needed, which increases the total device volume, induces current imbalance and leads to parasitic oscillation [60]. So, Rohm and Cree 1200 V SiC MOSFET power modules with higher current capabilities are evaluated. Fig. 6 shows the total MOSFET power loss of five 1200 V SiC MOSFET power modules at different output power ratings. The switching frequency is 100 kHz, and the maximum output power is 100 kW. Input, output voltages are 300 V and 600 V, respectively. The Rohm 1200 V 600 A SiC module can achieve the lowest total MOSFET power loss at full load.

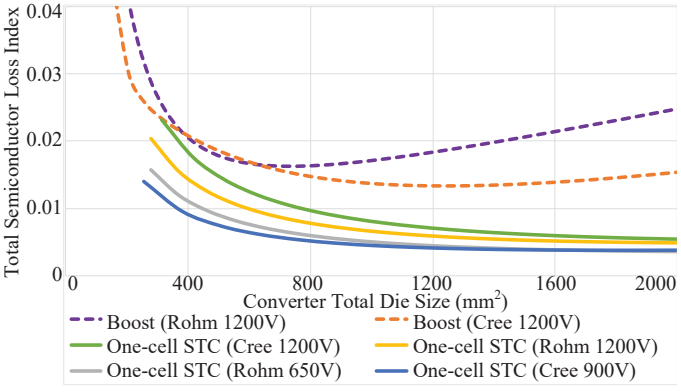


Fig. 5: Total semiconductor loss index comparison

To optimize the thermal performance of the devices, a temperature rise comparison of different SiC power modules is further conducted. The temperature rise calculation is based on the thermal resistance circuit in Fig. 7. The temperature rise vs. output power curves for these five SiC MOSFET modules are

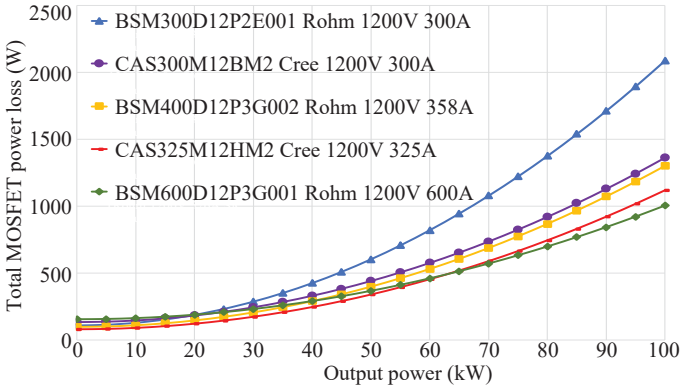


Fig. 6: Total MOSFET power loss comparison among different MOSFETs

presented in Fig. 8. With competitive thermal resistance, the Rohm 1200 V 600 A SiC module realizes lowest temperature rise in a wide output power range. Thus, the thermal performance is relatively optimized.

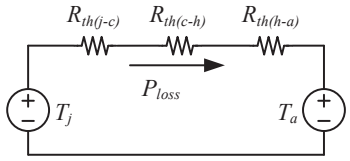


Fig. 7: Thermal resistance circuit

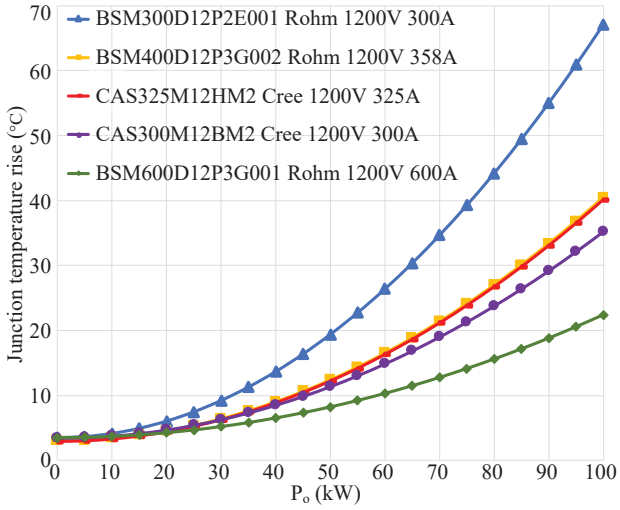


Fig. 8: Thermal performance comparison among five 1200 V SiC modules

Although higher frequency helps decrease the magnetic component size, speed up the transient load response, it introduces more AC loss to the high frequency resonant capacitor and AC busbar, increases the core loss of the resonant inductor. Considering this trade-off, the switching frequency is designed at 100 kHz for this project.

B. *Design of Heatsink*

Heatsink design is based on the thermal resistance circuit in Fig. 7. The heatsink thermal resistance can be derived in Eq. (29) according to the thermal dissipation and device power loss.

$$R_{th(h-a)} = \frac{T_j - T_a}{P_{loss}} - R_{th(j-c)} - R_{th(c-h)} \tag{29}$$

where, $R_{th(h-a)}$, $R_{th(j-c)}$ and $R_{th(c-h)}$ are thermal resistance between heatsink and ambient, junction and case, case and heatsink, respectively. $R_{th(j-c)}$ and $R_{th(c-h)}$ are equal to 0.061 °C/W and 0.015 °C/W, respectively [61]. T_j and T_a are junction and ambient temperature. P_{loss} is the total power loss of the devices.

The maximum junction temperature for the selected SiC module is 175 °C [61]. The total device power loss at 100 kW is 1004.37 W based on previous calculation. To reflect the real cooling system in hybrid electric vehicles, the ambient temperature T_a is designed as the water tank outlet temperature 85 °C [62]. Therefore, designed heatsink-ambient thermal resistance should satisfy: $R_{th(h-a)} \leq 0.0136$ °C/W. An off-the-shelf water cooling heatsink from wakefiled-vette® is selected. With 5.3 L/minute water flowing speed, the thermal resistance is around 0.013 °C/W. With this heatsink, maximum junction temperature is 174.39 °C at 85 °C water cooling temperature.

C. *Design of Resonant Capacitor*

The major challenges in this high-power resonant capacitor design are high frequency and high RMS current. High frequency helps shrink the passive component size, but brings in non-negligible voltage rating drops in the polypropylene film capacitors. High RMS current levels up the current capability threshold, which narrows the available candidate range. Another challenge is regarding the compact size while satisfying the current capability. When we try to solve these challenges, the resonant capacitor design is comprehensively conducted based on operating frequency range, resonant capacitance, required resonant inductance, volume, maximum allowed RMS voltage and current capability, as shown below.

To achieve the high-frequency and high RMS current resonant operation, both ceramic and film capacitors could be used. The Class II multi-layer ceramic capacitors (MLCC) have higher power density compared to the film capacitors assuming the same capacitance and current rating. However, considering that the ceramics are weak in tension, a crack can be relatively easily generated when excessive board flex is put on the soldered MLCC [63]. As a result, an electrical conduction between the two electrodes would happen, which could progress to a short circuit. Therefore, MLCCs are not preferred for the automotive, aerospace and marine power electronic applications due to these reliability concerns. Thus, the polypropylene film capacitors with the excellent current capability are considered for the desired resonant tank design.

Based on a summarization of high power resonant capacitors from different companies [64], the polypropylene film capacitors from Illinois Capacitor® provides specifically designed high-current, high-frequency resonant capacitors. Thus, all the conduction cooled high-density resonant capacitors from this company are studied, including LC1 ~ LC6, HC1 ~ HC6 and HC3A, HC3B series. In each category, one type with highest capacitance density, satisfying frequency range, full-load peak voltage and current requirements is selected. Fig. 9 shows the comparison of the capacitance density per unit volume. From the results in Fig. 9, LC2 and LC3 series can achieve much higher capacitance density.

Not only should the volume of the resonant capacitors be considered, but also does the whole resonant tank size need to be analyzed. Thus, the smaller inductance is preferred in our design. Fig. 10(a) shows the relationship between the required

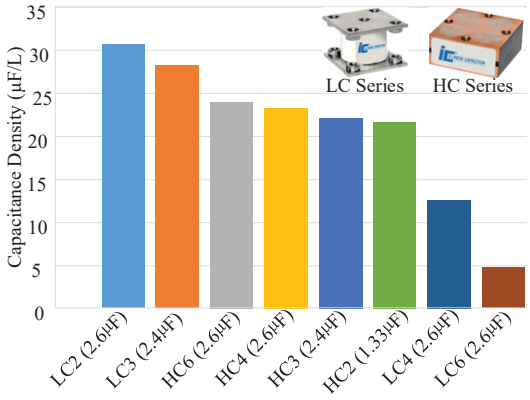
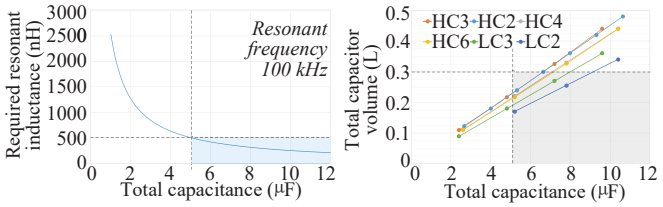


Fig. 9: Capacitance density per unit volume comparison

inductance and total resonant capacitance. Considering the practical size as well as the design of core and winding, the maximum inductance has been designed as 500 nH. Correspondingly, the minimum resonant capacitance is 5.066 μF. Besides, considering the power module and heatsink layout, the total capacitor volume is designed below 0.3 L. Fig. 10(b) shows the trade-off between the total capacitance and the volume. The remaining candidates in the shaded area are further compared in Table I, from which three 2.4 μF LC2 and three 2.6 μF LC3 are preferable due to smaller required inductance.



(a) (b)

Fig. 10: Capacitor evaluation based on required inductance and total volume

TABLE I: COMPARISON AMONG PROSPECTIVE CAPACITORS

Series	Total capacitance (μF)	Total volume (L)	RMS voltage (V)	RMS voltage capability at 100kHz (V)	Required inductance at 100kHz (nH)
HC2	5.32	0.24	319.79	500	476.13
HC4	5.2	0.22	320.69	500	487.12
HC6	5.2	0.22	320.69	600	487.12
LC3	7.2	0.27	310.96	410	351.81
LC2	5.2	0.17	320.69	350	487.12
LC2	7.8	0.26	309.36	350	324.75

However, the polypropylene film capacitor voltage rating drops at higher switching frequency, because of the heat generated by the AC loss at high frequency [65]. Thus, a safe margin needs to be maintained between the full-load peak voltage and the maximum voltage capability after derating at 100 kHz resonant frequency. In Fig. 11, the voltage derating with the resonant frequency of selected film capacitors are shown. The margin between the full-load voltage peak and the maximum voltage capability for the LC2 series is about 41 V, while for LC3 series it is around 100 V, which makes LC3 series more suitable for our application.

Finally, to evaluate the thermal performance of the selected resonant capacitors, the thermal impedance and temperature rise are calculated in Eq. (30), (31), respectively.

$$R_{TH(Cr)} = \Delta T_{Cr(\max)} \Big/ \left[\left(I_{Cr(RMS\_\max)} \right)^2 \cdot ESR \right] \quad (30)$$

$$\Delta T_{Cr} = R_{TH(Cr)} \cdot \left(I_{Lr(RMS)} / 3 \right)^2 \cdot ESR \quad (31)$$

Based on Eq. (30), the thermal resistance is calculated as (40 °C) / [(650 A)^2 × 0.2 mΩ] = 0.47 °C/W. From calculation results, 7.8 μF LC2 and 7.2 μF LC3 experience the temperature rise of 3.01 °C and 1.44 °C, respectively at full load and 100 kHz resonant frequency. By taking the above comparison and temperature verification into comprehensive consideration, three 2.4 μF LC3 capacitors have been finalized.

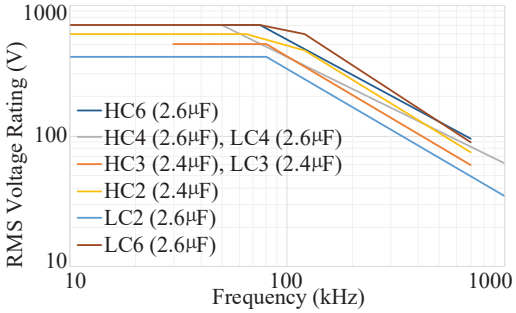


Fig. 11: Voltage derating curves for HC and LC series capacitors

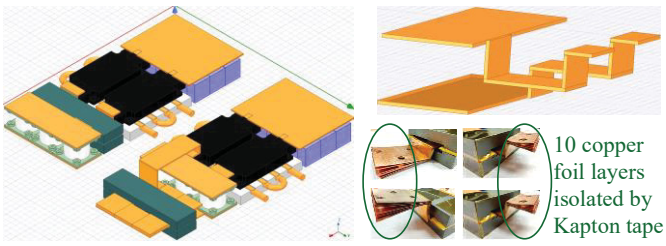
D. *Design of Resonant Inductor*

The challenges of the resonant inductor selection in this application are primarily due to high RMS current, high frequency core and winding design. High RMS, high frequency current is responsible for the remarkable AC winding loss due to the skin effect. A multi-layer AC busbar is designed to alleviate this issue. High power and high frequency also lead to significant core loss and corresponding temperature rise. Therefore, a careful core material evaluation and the trade-off between the core thermal performance and core volume are conducted to conquer this problem.

With the above 7.2 μF resonant capacitance design, to achieve a 100 kHz resonant frequency, the resonant inductance value is required to be 351.81 nH. The winding design and core design will be conducted in this section.

1) *Winding Design*

Fig. 12(a) shows two resonant side layout possibilities. The left-hand side presents a layout with only one-turn winding. The inductor is split into two with similar inductance. The right-hand side layout can achieve more flexible number of turns, but it brings challenge for the winding geometry design. The connecting copper joint between adjacent copper layers introduces more manufacturing difficulties. The copper bar linking with the power module overpasses resonant capacitors,



(a) (b)

Fig. 12: (a) One-turn and multiple-turn winding design layouts. (b) above: AC busbar 3D model; below: AC busbar assembly

which increases AC copper loss and prolong the prototype height. Thus, one-turn winding design is adopted. The AC inductor could be designed in the similar height with the AC capacitors, power module, heatsink, and the DC side. Thus, the space can be fully utilized in a compact way.

Multi-layer copper foil AC busbar is designed for this high-current high-frequency winding. By distributing the current through multiple layers, this arrangement reduces AC loss caused by the AC current skin effect. The Kapton tape with the wide-range temperature capability is applied to insulate each layer. The skin depth δ is calculated based on Eq. (32) [66][67].

$$\delta = \sqrt{\rho/(\pi f \mu)} \tag{32}$$

where, f is the AC frequency. The copper resistivity ρ and permeability μ are 1.76 × 10^{-8} Ω·m, 1.257 × 10^{-6} H/m, respectively. At 100 kHz, the skin depth for copper is calculated as 0.211 mm. So, the copper foil with a thickness no larger than 0.211 mm has been selected. To further design the copper cross-section area and number of layers, the current density should be considered. For the one-turn winding design, current density is recommended as 300 mil^2/A or 5.167 A/mm^2 to avoid excessive copper loss and temperature rise [68]. Considering that AC RMS current value is 370.24 A and the cross-section area of selected one-layer copper foil is 7.112 mm^2, the total number of layers is (370.24 / 5.167) / (7.112) ≈ 10. Thus, 10-layer copper foil has been applied in this AC busbar. The total cross-section area of AC busbar A_{AC_Busbar} is 71.12 mm^2. Its 3D model and assembly are shown in Fig. 12(b). More inductor winding optimization strategies will be addressed in future publications.

2) Core Design

The core loss induced heat is a significant design constraint in the AC inductor design [69]. Thus, the core loss and temperature rise are compared in the core selection. The trade-off between the core temperature rise and volume is analyzed.

The powder cores and ferrite cores from major magnetic manufacturers are compared. The core loss density equation of Chang Sung Corporation (CSC) cores and Hitachi soft ferrite cores is in Eq. (33) [70][71].

$$P_V = (K_h \cdot f + K_e \cdot f^{\lambda}) \cdot (B_{PK})^Y \tag{33}$$

where, P_V is the core loss density with the unit of kW/m^3. f is the frequency (kHz). K_h is the hysteresis loss efficient. K_e is the eddy current loss efficient. Y is an exponent close to 2.

Core loss density of Hitachi HLM50 amorphous powder core, Magnetics powder, ferrite cores is in Eq. (34) [72]–[74].

$$P_V = a \cdot (B_{PK})^b \cdot (f)^c \tag{34}$$

By applying the above two equations, the core loss density comparison is plotted in Fig. 13 at 100 kHz frequency. Hitachi soft ferrite core ML29D is finalized due to its smaller core loss density in the 0.1 ~ 1 T flux density range.

E-shaped cores are selected in this project because it can achieve simpler assembly and more cost-effective solutions compared with pot cores [75]. Fig. 14 shows a typical E-core dimension and the magnetic paths. In this design, α_2 is fixed as 152.4 mm due to the length constraints of the heatsink and SiC module. β_2 is restricted by the height of the prototype, which is selected as 15 mm. According to the reference design of planar E cores [66][76], the core height β_2 is the sum of β_1 and α_1.

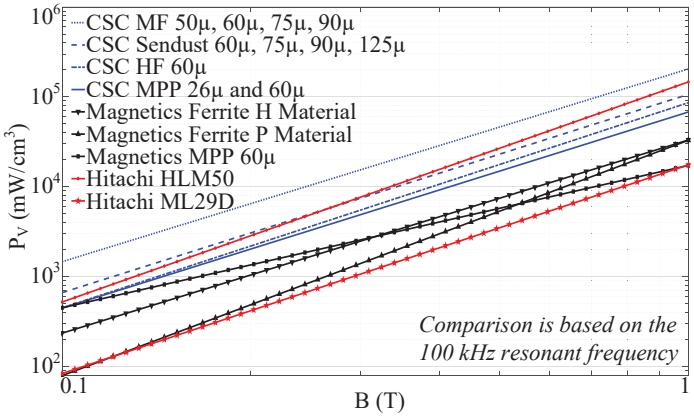


Fig. 13: Core loss density comparison at 100 kHz frequency

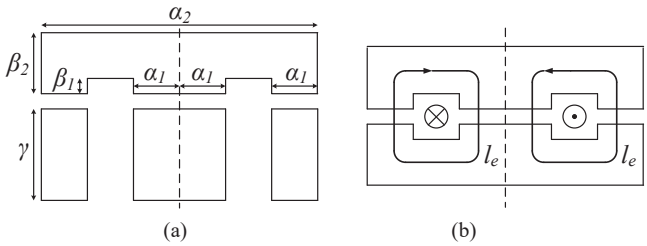


Fig. 14: (a) E core dimensions. (b) Equivalent magnetic paths

To achieve desired inductance, core cross-section area A_e and air gap length l_g need to be designed based on Eq. (35) [77].

$$L = \left(N^2 \cdot A_e\right) / \left[\left(l_g/\mu_0\right) + \left(l_e/\mu_c\right)\right] \tag{35}$$

where, N is number of turns. A_e is effective core cross-section area. μ_0, μ_c are permeability of the free space and core, respectively. l_g is air gap length. l_e is equivalent magnetic path length as shown in Eq. (36) [78].

$$l_e = 2\left(\alpha_2/2 - 2\alpha_1 + 2\beta_1 + l_g\right) + \pi \cdot \alpha_1 \tag{36}$$

A proper core shape needs to satisfy the window utilization requirement due to the winding insulation. The window utilization factor K_u should be less than 0.65 for low voltage foil inductor design [79], as shown in Eq. (37).

$$K_u = A_{AC\_Bus} / A_{window} = 71.12 mm^2 / A_{window} \le 65\% \tag{37}$$

Based on the core geometry in Fig. 14(a), the window area A_{window} equals to $2\beta_1 \cdot (\alpha_2/2\text{-}2\alpha_1)$. Thus, a constraint for α_1 is derived: $\alpha_1 \le 13.87$ mm. In this project, 13 mm has been applied. The magnetics path length can be further calculated once α_1 is fixed. The calculated l_e is 149.24 mm from Eq. (36) while the air gap length is relatively small to be ignored here.

To further determine the core width γ and corresponding core cross-section area A_e, a trade-off between core temperature rise and core volume should be made. According to Faraday's law, the flux density swing ΔB is derived as shown in Eq. (38).

$$\Delta B = \left| \left[\int_{T_s/4}^{3 \cdot T_s/4} L di_L(t) \right] \Big/ \left(N \cdot A_e\right) \right| \tag{38}$$

From Eq. (2), the peak resonant current I_{PK} is π times the average output current. Thus, ΔB is further derived in Eq. (39).

$$\Delta B = \left(L \cdot 2I_o \cdot \pi\right) / \left(N \cdot A_e\right) \tag{39}$$

For the AC flux swing in our case, peak flux density B_{PK} is half the flux density swing ΔB [73], as shown in Eq. (40).

$$B_{PK} = \Delta B/2 = \left(L \cdot P_o \cdot \pi\right) / \left(N \cdot A_e \cdot 2V_{in}\right) \tag{40}$$

The core loss density P_V is further derived in Eq. (41) by

combining Eq. (33) and Eq. (40).

$$P_V = (K_h \cdot f + K_e \cdot f^{\lambda}) \cdot \left[(L \cdot P_o \cdot \pi) / (2N \cdot A_e \cdot V_{in}) \right]^X \quad (41)$$

where, K_h is 0.1035. K_e is 7.178×10^{-7}. λ is 2. X is 2.323 [71]. N is 1. f and L are 100 kHz and 351.18 nH, respectively as designed in the previous sections. P_o is 100 kW. V_{in} is 300 V.

Core loss density is further shown in Eq. (42) considering $A_e = 2\alpha_1 \cdot \gamma$. The core volume V is in Eq. (43). Correspondingly, the core power loss can be calculated by $P_{core} = P_V \cdot V$. The core temperature rise is estimated by Eq. (44) [69].

$$P_V = (K_h \cdot f + K_e \cdot f^{\lambda}) \cdot \left[(L \cdot P_o \cdot \pi) / (4N \cdot \alpha_1 \cdot \gamma \cdot V_{in}) \right]^X \quad (42)$$

$$V = 4 \cdot \alpha_1 \cdot (\beta_2 - \alpha_1) \cdot \gamma + \alpha_1 \cdot \alpha_2 \cdot \gamma \quad (43)$$

$$\Delta T_{core} = \left(P_{core} / A_{surface} \right)^{0.833} \quad (44)$$

where, ΔT_{core} is the core temperature rise with the unit °C. P_{core} is of the unit mW. $A_{surface}$ has the unit of cm^2.

Based on above analysis, the core temperature rise versus core width is plotted in Fig. 15. To reflect the optimized design region for the core width, the core volume is also plotted. Two constraints have been considered in the core width design. One is the core temperature rise, which is limited below 100 °C in order to guarantee a safe operation region without external cooling for the core. Another is the core volume, which is designed to be smaller than 0.1 Liter, considering the dimensions of the resonant capacitors, heatsink and SiC power modules. Hence, a design range can be obtained based on this quantitative trade-off. Correspondingly, the core width γ range from 32.5 to 48 mm is derived for this application. Thus, the core cross-section area A_e has the range of 845 ~ 1248 mm^2.

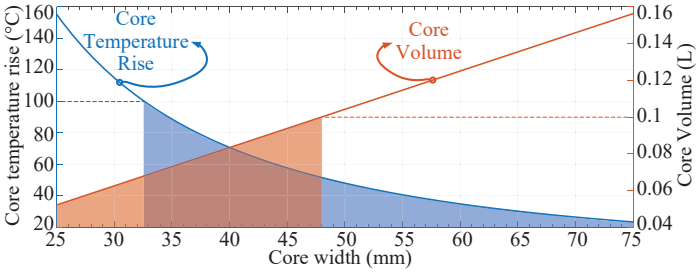


Fig. 15: Core temperature rise and core volume trade-off

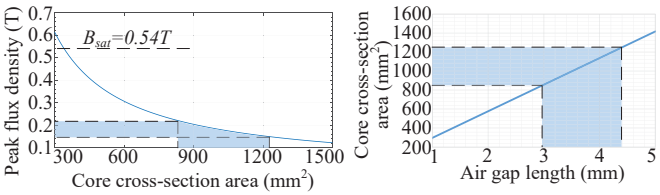
Based on the derived range of the core cross-section area, Fig. 16(a) shows the range of the peak flux density, i.e. 0.1476 ~ 0.218 T according to Eq. (40). Considering 0.54 T saturation magnetic flux density B_{sat} for the ML29D core with 1000 A/m magnetic field strength at 23 °C [80], the designed flux density range is below half the saturated flux density. Thus, the full utilization and the flux saturation of the core are avoided.

When the inductance and the number of the winding are fixed, based on the inductance calculation in Eq. (35), the relationship between A_e and l_g is described in Eq. (45).

$$A_e = L \cdot \left(l_g / \mu_0 + l_e / \mu_c \right) \quad (45)$$

Since the range of the core cross-section area is known, based on Eq. (45), the relationship between A_e and l_g is plotted in Fig. 16(b). A design range for the air gap length l_g can be derived. From the figure, l_g ranges from 2.967 mm to 4.407 mm.

With the above core temperature rise and volume trade-off considered, in the finalized design, a core width of 40 mm is selected in the preferable region. Based on this designed core



(a) (b)

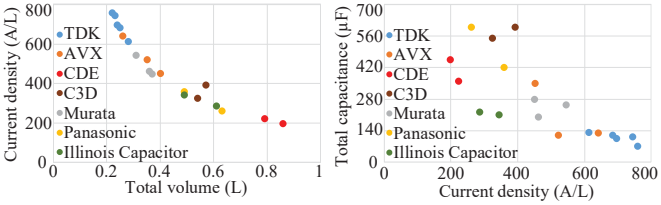
Fig. 16: The relationship between (a) flux density and core cross-section area. (b) core cross-section area and air gap length

width, the corresponding core cross-section area is calculated as 1040 mm^2. The peak flux density and the air gap length are finalized as 0.1771 T and 3.664 mm, respectively. With this designed core shape, according to the curve in Fig. 15, the core temperature rise is about 70 °C at 100 kW. According to the core loss density P_V and core temperature rise ΔT_{core} equations, there exists a relationship between the core temperature rise and output current $\Delta T_{core} \propto (I_o)^{(2.323\times0.833)}$. Hence, at 50 kW, the core temperature rise is 0.2615 times the counterpart at the full load, which is about 18.3 °C. So, this inductor shape design results in a desired thermal region at both the 50 kW and 100 kW.

E. Design of DC Capacitors

Challenges of DC capacitor design in this application are mainly from the high RMS current. Higher current capability per volume normally accompanies smaller capacitance, which may not meet the minimum voltage ripple needs. Another challenge is to achieve a compact size while satisfying the other requirements. To solve these challenges, three parameters are selected as the design criteria, i.e. the total capacitance, RMS current capability, and capacitor volume. The larger total capacitance, higher RMS current density per unit volume, and smaller total volume are preferred in the evaluation.

Fig. 17 shows seven major film capacitor manufacturer investigation, considering the RMS current capability requirement indicated in the simulated C_1 and C_{in} current waveforms in Fig. 19(b). In each provider, the series with highest RMS current density per unit volume have been identified. Fig. 17(a) shows three prospective candidates, i.e. FFB and FFV3 Series from AVX®, FH series from Murata®, and B32674D Series from TDK®, have higher RMS current density. Fig. 17(b) presents that TDK series capacitors achieve smaller capacitance compared with others. Although the total capacitance is smaller compared with the other candidates, it can still satisfy the minimum DC capacitance requirement to realize desirable small voltage ripple. Based on the PLECS simulation, 75 µF DC capacitance is enough to achieve a 5% voltage ripple. Therefore, the B32674D3126 from TDK has been selected for its highest RMS current per unit volume and



(a) (b)

Fig. 17: Investigation of DC capacitors from major manufacturers

the smallest volume with sufficient capacitance.

In order to decide a proper number of DC capacitors, the trade-off between the temperature rise and DC capacitor volume is conducted in Fig. 18. This design selects 9 input and 9 output capacitors considering these two factors as well as the practical mechanical layout, which needs to match the dimensions of the power modules and heatsink. The full-load temperature rise is about 39 °C. Due to the half capacitor RMS current at the half load, the 50 kW temperature rise can be derived as one quarter of the full-load temperature rise, which is around 9.75 °C. The full-load temperature is designed to be 64 °C at 25 °C ambient temperature. This is lower than the rated temperature, which is 85 °C [81].

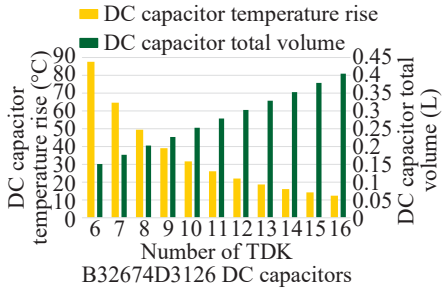
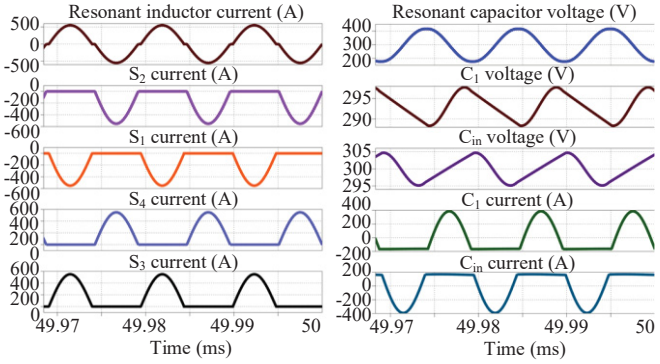


Fig. 18: Trade-off between temperature rise and total volume

VI. Simulation and Experiment Results

100 kW 300 V - 600 V one-cell STC at ZCS mode has been simulated in PLECS. Fig. 19(a) shows resonant current and S_1, S_2, S_3, S_4 switch current. Fig. 19(b) presents resonant capacitor voltage, DC capacitor voltage and current. The simulation results are consistent with the analysis in Section II.



(a) (b)

Fig. 19: Simulation results at 300 V – 600 V 100 kW

Fig. 20 shows the developed100 kW prototype. The control is realized through the TI® TMS320F28335 microcontroller and Xilinx® FPGA Spartan-6 XC6SLX9 IC. Fig. 20 also presents the three dimensions of the converter. The length, width and height are 37.8 cm, 15.1 cm and 4.2 cm, respectively. So, the converter main power processing part volume and the power density are about 2.4 L, and 41.7 kW/L, respectively.

In the test, the switching frequency is fine-tuned as 84.9 kHz, which includes the deadtime. Deadtime is set as 300 ns. The actual resonant frequency of the design is higher than the switching frequency. Fig. 21 shows the testing results at 50 kW with 300.24 V V_{in}, 598.98 V V_o and 100 kW with 299.95 V V_{in}, 584.23 V V_o. As shown Fig. 21(a), the switch drain current

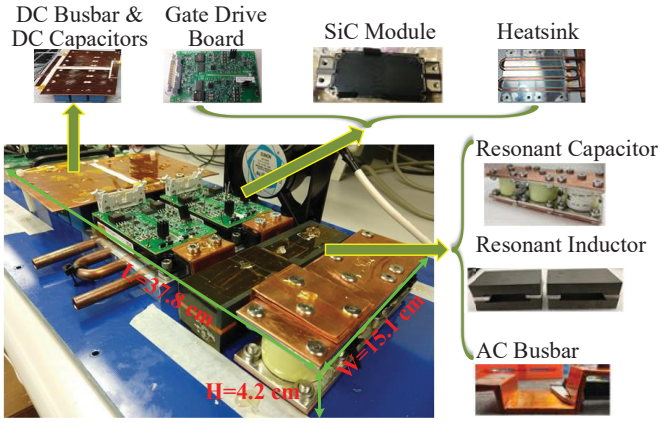
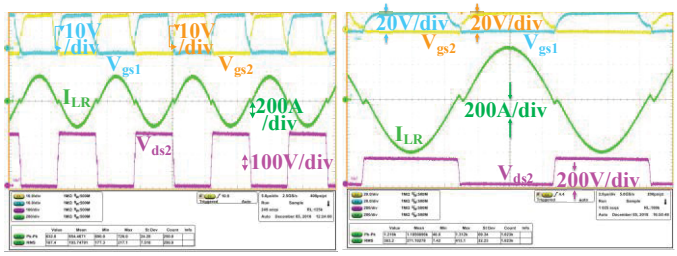


Fig. 20: The designed and assembled 100 kW one-cell STC

decreases to zero before it is turned off so that the ZCS is achieved. The top two waveforms are V_{gs} of switches S_1, S_2 corresponding to Fig. 2(a). The middle one is tested resonant current with the RMS value around 383.2 A. Based on Eq. (2), the corresponding theoretical RMS current value is 370.24 A, which is smaller than the tested value. This is because the current peak rises when the deadtime is included. The bottom trace is V_{ds} of S_2. Tested waveforms at 50 kW are in Fig. 21(b).



(a) (b)

Fig. 21: 300 V – 600 V test results at (a) 50 kW and (b) 100 kW

The tested thermal performance at 50 kW continuous operation is shown in Fig. 22 captured from the thermal camera. The steady-state DC and AC busbar maximum temperature is around 64.4 °C and 81.2 °C, respectively.

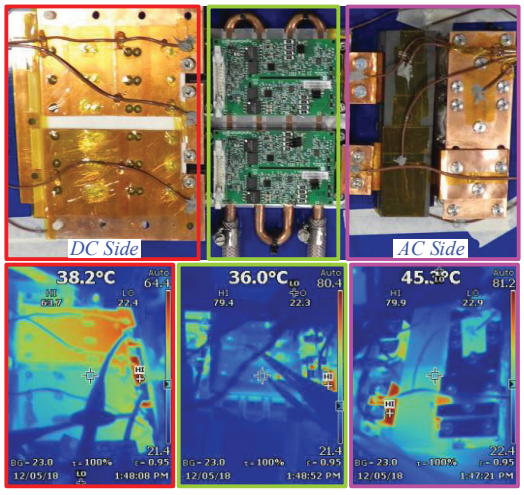


Fig. 22: Tested thermal performance at 50 kW continuous operation

Table II shows the detailed tested thermal performance at 50 kW continuous operation, based on thermal couple

measurement. The resonant inductor core temperature rise is 17.5 °C, which matches the theoretical half-load thermal analysis in Part D of the Section V. The two DC capacitors C_{in} and C_1 show temperature of 37 °C and 24 °C, respectively. Thus, the maximum temperature rise for the DC capacitor is about 12 °C, which matches the 9.75 °C theoretical temperature rise at half load in Part E of the Section V. From the thermal results, high DC and AC busbar power losses are indicated.

TABLE II: STEADY-STATE TEMPERATURE AT 50 KW OPERATION

Component	Temperature (°C)	Component	Temperature (°C)
AC busbar	56.5	Heatsink	25
V_{in} DC busbar	59	Inductor core	42.5
V_o DC busbar	46	DC capacitors C_{in}	37
GND DC busbar	54	DC capacitors C_1	24

The baseplate temperature measured based on the negative temperature coefficient thermistor inside the SiC power module is acquired through the analog-to-digital sampling circuit and DSP code. It can be further utilized to derive the junction temperature T_j based on the junction-baseplate thermal impedance 61 °C/kW [61]. Considering the self-heating effect caused by the increased junction temperature, the iterations have been conducted based on the $R_{ds(on)}$ vs. T_j relationship until the T_j arrives to stable. T_j is calculated based on Eq. (46).

$$T_j = T_c + R_{th(j-c)} \cdot \left(\left(I_{RMS\_S} \right)^2 \cdot R_{ds(on)} \left(T_{j(1)} \right) + P_{Gate} + P_{Coss} \right) \quad (46)$$

where, $T_{j(1)}$ is the junction temperature in the previous state. The estimated T_j is used to evaluate the thermal performance of the SiC module. Fig. 23 shows the tested baseplate temperature and calculated T_j. Based on the curve fitted polynomial linear model in MATLAB curve fitting tool, the relationship between junction temperature and output power is presented in Eq. (47).

$$T_j = p_1 \cdot (P_o)^3 + p_2 \cdot (P_o)^2 + p_3 \cdot (P_o) + p_4 \quad (47)$$

where, p_1, p_2, p_3, p_4 are -4.174×10^{-5}, 7.416×10^{-3}, -0.05791, and 34.44, respectively. Based on Eq. (47), the full-load junction temperature could be estimated as 61.07 °C. Compared with the theoretical junction temperature evaluation for the selected SiC module in Fig. 8, if the ambient temperature is assumed as 25 °C, the tested T_j at 50 kW continuous operation is about 5 °C higher. This could be explained from three aspects. First, the total practical thermal impedance is larger than estimated. Second, the deadtime induced device RMS current increase was not considered in Fig. 8. Third, the impact of junction temperature on $R_{ds(on)}$ increase was not included.

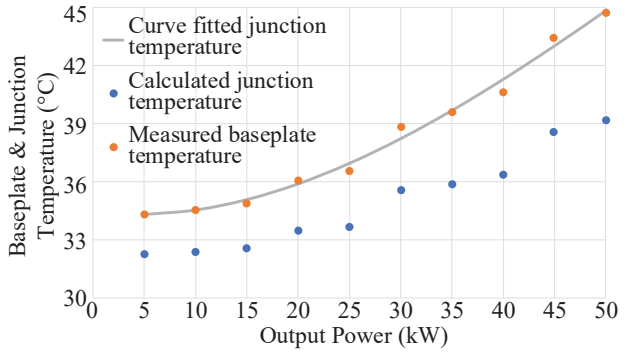
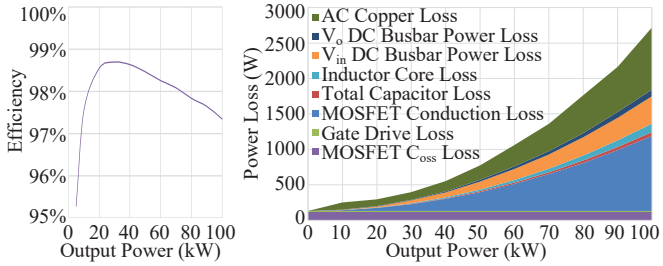


Fig. 23: The tested baseplate temperature and calculated junction temperature

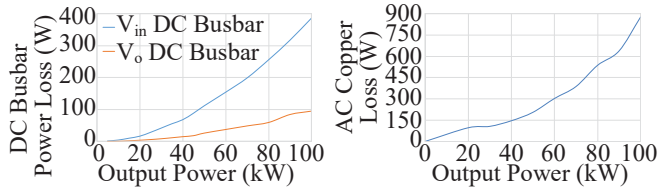
Fig. 24(a) shows tested efficiency based on the measured voltage, current and power data from Yokogawa® WT1800 power analyzer. The tested peak efficiency reaches to about 98.7% at around 30 kW. The tested full-load and half-load efficiencies are about 97.35% and 98.47%, respectively. The power loss breakdown is conducted with different output power in Fig. 24(b). From the plot, the MOSFET conduction loss is a major contribution at full load. Both the on-resistance increase with the junction temperature and the device RMS current increase with the deadtime have been included in the conduction loss estimation. Besides, the V_{in} DC busbar loss and AC copper loss are also significant in the total power loss. The V_{in} and V_o DC busbar power losses are calculated based on the measured voltage drops between two ends on the V_{in} DC busbar and V_o DC busbar, respectively.



(a) (b)

Fig. 24: (a) Tested efficiency. (b) Tested power loss breakdown

Fig. 25 presents the changes of DC busbar power loss and AC copper loss with output power. Fig. 25(a) shows that at 100 kW output power, the V_{in} and V_o DC busbar power losses reach to around 386.9 W, and 94.4 W, respectively. The AC copper loss is estimated based on the difference between the tested total power loss and the power loss estimated from the output and input power difference. Fig. 25(b) illustrates the AC copper loss versus the output power, from which the maximum AC copper loss reaches up to about 876.2 W at 100 kW output power.



(a) (b)

Fig. 25: (a) DC busbar power loss vs. P_o. (b) AC copper loss vs. P_o

To verify the theoretical calculated TSLI based on Rohm 1200 V 95 A SiC die (part number: S4103 [57]), a comparison has been conducted in Fig. 26 between the theoretical and tested TSLIs with changing output power for this application. Considering 576 A current rating (at 60 °C case temperature) of the selected Rohm 1200 V SiC power module, six S4103 bare dies would be needed. Besides, four SiC MOSFETs are utilized in the prototype. Therefore, the total die area is 24 times the S4103 die area. The difference between the theoretical and tested TSLI could be mainly caused by the current measurement noise, which further impacts the total conduction losses. As can be seen from Fig. 26, the tested TSLI based on the 1200 V 576

A SiC MOSFET module matches well with the theoretical value calculated from the 1200 V 95 A SiC bare die.

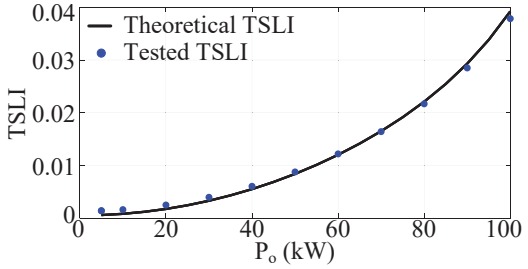


Fig. 26: Comparison between the theoretical and tested TSLIs

VII. Conclusions and Future Work

This paper has demonstrated a development of a 100 kW SiC based switched tank converter for the transportation electrification applications. The proposed total semiconductor loss index (TSLI) has been shown as an effective method to evaluate different topologies and device technologies to achieve the lowest device power loss with minimum semiconductor die area. By applying this index, the optimal topology and device technology for the STC could be identified. From the detailed design procedures and passive component optimization, a compact resonant tank with single-turn soft-ferrite-core inductor and three low-volume high-current high-frequency polypropylene film capacitors has been achieved. From the experimental results, the proposed thermal design has shown expected performance at 50 kW continuous operation and 100 kW peak operation. The assembled prototype main power circuit power density is about 42 kW/L. The tested peak efficiency is around 98.7% at 30 kW. The tested 100 kW efficiency is about 97.35%. Future power density and efficiency improvement will include more suitable lower-voltage-rating power device selection, high frequency AC and DC busbar optimization with reduced volume and power loss.

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References

[1] M. D. Kankam and M. E. Elbuluk, “A Survey of Power Electronics Applications in Aerospace Technologies,” 2001.

[2] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, “High-Power Bidirectional DC–DC Converter for Aerospace Applications,” *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4366–4379, Nov. 2012.

[3] R. Shuttleworth, A. J. Forsyth, and R. T. Naayagi, “Bidirectional control of a dual active bridge DC–DC converter for aerospace applications,” *IET Power Electron.*, vol. 5, no. 7, pp. 1104–1118, Nov. 2012.

[4] G. Yang, F. Xiao, X. Fan, R. Wang, and J. Liu, “Three-Phase Three-Level Phase-Shifted PWM DC–DC Converter for Electric Ship MVDC Application,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 162–170, Mar. 2017.

[5] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, “Modeling and Control of the Isolated DC–DC Modular Multilevel Converter for Electric Ship Medium Voltage Direct Current Power System,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 124–139, Mar. 2017.

[6] U.S. Department of Energy, “Electrical and Electronics Technical Team Roadmap,” *U.S. DRIVE Partnership*, 2017. [Online]. Available: https://www.energy.gov/sites/prod/files/2017/11/f39/EETT Roadmap 10-27-17.pdf.

[7] X. Zhao, J. M. Guerrero, and X. Wu, “Review of aircraft electric power systems and architectures,” in *ENERGYCON 2014 - IEEE International Energy Conference*, 2014, pp. 949–953.

[8] B. Zahedi, “Shipboard DC Hybrid Power Systems : Modeling, efficiency analysis and stability control,” Norwegian University of Science and Technology, Department of Electric Power Engineering, 2014.

[9] S. Castellan, R. Menis, A. Tessarolo, and G. Sulligoi, “Power electronics for all-electric ships with MVDC power distribution system: An overview,” in *2014 Ninth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, 2014, pp. 1–7.

[10] J. S. Chalfant and C. Chryssostomidis, “Analysis of various all-electric-ship electrical distribution system topologies,” in *2011 IEEE Electric Ship Technologies Symposium*, 2011, pp. 72–77.

[11] S. Castellan, R. Menis, A. Tessarolo, F. Luise, and T. Mazzuca, “A review of power electronics equipment for all-electric ship MVDC power systems,” *Int. J. Electr. Power Energy Syst.*, vol. 96, pp. 306–323, Mar. 2018.

[12] W. Qian and H. Cha et al., “55-kW variable 3X DC-DC converter for plug-in hybrid electric vehicles,” *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1668–1678, Apr. 2012.

[13] T. Kim and S. Baek, “A direct DC bus voltage regulation of the variable voltage converter in the electric traction drive system,” in *2017 IEEE Transportation and Electrification Conference and Expo, ITEC 2017*, 2017, pp. 732–736.

[14] L. Chen, “A variable voltage converter with direct bypass for traction drive inverters,” in *2013 IEEE Energy Conversion Congress and Exposition, ECCE 2013*, 2013, pp. 2793–2798.

[15] J. Elmes, “High-Density and High-Efficiency Soft Switching Modular Bi-Directional DC-DC Converter for Hybrid Electric Vehicles,” Ph.D Thesis, University of Central Florida, 2010.

[16] L. Chen, L. Xu, N. Narayanachar, and S. Zarei, “Development of a drive cycle based evaluation method for Variable Voltage Converter in vehicle electrification applications,” in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 254–259.

[17] L. Chen, “Variable Voltage Converter with Direct Output Voltage Clamping,” US 2012/0019231 A1, 2012.

[18] X. Jia and D. Xu et al., “A High Power Density and Efficiency Bi-Directional DC / DC Converter for Electric Vehicles,” in *ECCE Asia, Seoul*, 2015, pp. 874–880.

[19] J. Scoltock, G. Calderon-lopez, and A. J. Forsyth, “Topology and Magnetics Optimisation for a 100-kW Bi-Directional DC-DC Converter,” in *2017 IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2017, pp. 1–6.

[20] J. Zhang, J. S. Lai, R. Y. Kim, and W. Yu, “High-power density design of a soft-switching high-power bidirectional dc-dc converter,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.

[21] D. Christen, S. Tschannen, and J. Biela, “Highly efficient and compact DC-DC converter for ultra-fast charging of electric vehicles,” in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, p. LS5d.3-1 to 3–8.

[22] W. Qian, J. G. Cintrón-Rivera, F. Z. Peng, and D. Cao, “A multilevel DC-DC converter with high voltage gain and reduced component rating and count,” in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2011, pp. 1146–1152.

[23] C. Schaef, J. S. Rentmeister, and J. Stauth, “Multimode Operation of Resonant and Hybrid Switched-Capacitor Topologies,” *IEEE Trans. Power Electron.*, pp. 1–1, 2018.

[24] Y. Lei, W.-C. Liu, and R. C. N. Pilawa-Podgurski, “An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters,” *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1–1, Mar. 2017.

[25] M. Vasic, D. Serrano, P. Alou, J. A. Oliver, P. Grbovic, and J. A. Cobos, "Comparative analysis of two compact and highly efficient resonant switched capacitor converters," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2018, vol. 2018-March, pp. 2168–2174.

[26] J. Itoh, K. Matsuura, and K. Orikawa, "Reduction of a boost inductance using a switched capacitor DC-DC converter," in *8th International Conference on Power Electronics - ECCE Asia*, 2011, pp. 1315–1322.

[27] T. Zhao, J. Wang, A. Q. Huang, and A. Agarwal, "Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems," *2007 IEEE Ind. Appl. Annu. Meet.*, pp. 331–335, 2007.

[28] C. Sintamarean, F. Blaabjerg, and H. Wang, "Comprehensive evaluation on efficiency and thermal loading of associated Si and SiC based PV inverter applications," *IECON Proc. (Industrial Electron. Conf.*, pp. 555–560, 2013.

[29] S. Pettersson, S. Kicin, E. Bianda, T. Holm, P. Raisanen, and F. Canales, "Performance evaluation of custom-made 1.2-kV 100-A silicon carbide half-bridge module in three-phase grid connected PWM rectifier," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, pp. 4138–4144, 2015.

[30] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, 2002.

[31] G. Calderon-Lopez and A. J. Forsyth, "High Power Density DC-DC Converter with SiC MOSFETs for Electric Vehicles," in *IET PEMD*, 2014, pp. 1.4.01--1.4.01.

[32] S. Jiang, S. Saggini, and C. Nan et al., "Switched tank converters," *IEEE Trans. Power Electron.*, vol. Sept, pp. 1–1, 2018.

[33] M. Shoyama, F. Deriha, and T. Ninomiya, "Resonant boost switched capacitor converter with high efficiency," in *30th Annual Conference of IEEE Industrial Electronics Society, 2004. IECON 2004*, 2004, vol. 1, pp. 222–226.

[34] K. Sano and H. Fujita, "Performance of a high-efficiency switched-capacitor-based resonant converter with phase-shift control," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 344–354, Feb. 2011.

[35] Y. Li, B. Curuvija, X. Lyu, and D. Cao, "Multilevel modular switched-capacitor resonant converter with voltage regulation," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 88–93.

[36] Z. Ni, Y. Li, J. Johnson, and D. Cao, "Resonant Multilevel Modular Boost Inverters for Single-Phase Transformerless Photovoltaic Systems," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR*, 2018, pp. 2555–2562.

[37] Z. Ni *et al.*, "A GaN Switched Tank Converter with Partial Power Voltage Regulation for Electric Vehicle Applications," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, vol. 2019-March, pp. 1682–1689.

[38] T. Friedli, M. Hartmann, and J. W. Kolar, "The Essence of Three-Phase PFC Rectifier Systems -- Part II," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 543–560, Feb. 2014.

[39] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," in *Power Electronics in Transportation (IEEE Cat. No.04TH8756), Novi, MI, USA*, 2004, pp. 125–132.

[40] B. J. Baliga, "Power MOSFETs," in *Fundamentals of Power Semiconductor Devices*, 1st ed., Springer US, 2008, pp. 279–506.

[41] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, "A 98.55% Efficiency Switched-Tank Converter for Data Center Application," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6205–6222, Nov. 2018.

[42] X. Lyu, Y. Li, N. Ren, C. Nan, D. Cao, and S. Jiang, "Optimization of High-Density and High-Efficiency Switched-Tank Converter for Data Center Applications," *IEEE Trans. Ind. Electron.*, pp. 1–1, 2019.

[43] Y. Li, Z. Ni, and D. Cao, "Optimal Operation of Multilevel Modular Resonant Switched-Capacitor Converter," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 218–224.

[44] D. Cao, X. Lu, X. Yu, and F. Z. Peng, "Zero voltage switching double-wing multilevel modular switched-capacitor DC-DC converter with voltage regulation," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2013, pp. 2029–2036.

[45] R. W. Erickson and D. Maksimovic, "Eq. (19.4), Chapter 19.1 Sinusoidal Analysis of Resonant Converters," in *Fundamentals of Power Electronics*, 2nd ed., Springer Science & Business Media, 2007, p. 711.

[46] D. Reusch and J. Strydom, "Evaluation of Gallium Nitride Transistors in High Frequency Resonant and Soft-Switching DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5151–5158, Sep. 2015.

[47] P. Shamsi, M. McDonough, and B. Fahimi, "Wide-Bandgap Semiconductor Technology: Its impact on the electrification of the transportation industry," *IEEE Electrif. Mag.*, vol. 1, no. 2, pp. 59–63, Dec. 2013.

[48] A. Lidow and J. Strydom, "Gallium Nitride (GaN) Technology Overview," in *GaN Transistors for Efficient Power Conversion*, 1st ed., Efficient Power Conversion Corporation, 2012, pp. 1–6.

[49] S. L. Colino and R. Beach, "Fundamentals of Gallium Nitride Power Transistors," *EPC (Efficient Power Conversion)*. pp. 1–4, 2011.

[50] N. Kaminski, "State of the Art and the Future of Wide Band-Gap Devices," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1–9.

[51] A. O. Adan, D. Tanaka, L. Burgyan, and Y. Kakizaki, "The Current Status and Trends of 1200-V Commercial Silicon-Carbide MOSFETs: Deep Physical Analysis of Power Transistors From a Designer's Perspective," *IEEE Power Electron. Mag.*, vol. 6, no. 2, pp. 36–47, Jun. 2019.

[52] B. J. Baliga, "Section 6.15.1 Input Switching Power Loss in Chapter 6 Power MOSFETs," in *Fundamentals of Power Semiconductor Devices*, 2008, p. 427.

[53] G. Lakkas, "MOSFET power losses and how they affect power-supply efficiency," *Analog Appl. J.*, pp. 22–26, 2016.

[54] B. J. Baliga, "Section 6.13 Device Capacitances in Chapter 6 Power MOSFETs," in *Fundamentals of Power Semiconductor Devices*, 1, Ed. Springer US, 2008, p. 409.

[55] B. J. Baliga, "Section 6.13.2 Power VD-MOSFET Structure Capacitances in Chapter 6 Power MOSFETs," in *Fundamentals of Power Semiconductor Devices*, 1st ed., Springer US, 2008, p. 394.

[56] J. B. Fedison, M. Fornage, M. J. Harrison, and D. R. Zimmanck, "Cossrelated energy loss in power MOSFETs used in zero-voltage-switched applications," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2014, pp. 150–156.

[57] Rohm Semiconductor, "Datasheet of N-channel Silicon Carbide Power MOSFET bare die - S4103," 2018. [Online]. Available: https://www.rohm.com/datasheet/S4103/s4103-e.

[58] Wolfspeed/Cree Inc., "Datasheet of 2nd-Generation Z-FET® 1200-V, 25-mΩ, Silicon-Carbide MOSFET Bare Die," 2016. [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/152/product/2/cpm2_1200_0025b.pdf.

[59] B. Hauke, "Basic Calculation of a Boost Converter's Power Stage (Rev. C)," *Texas Instruments Application Report*, 2014. [Online]. Available: http://www.ti.com/lit/an/slva372c/slva372c.pdf.

[60] Toshiba Electronic Devices & Storage Corporation, "MOSFET Parallening (Parasitic Oscillation between Parallel Power MOSFETs)," 2018.

[61] Rohm Semiconductor, "SiC MOSFET Power Module BSM600D12P3G001 Datasheet," 2015. [Online]. Available: https://www.rohm.com/datasheet/BSM600D12P3G001/bsm600d12p3g001-e.

[62] C. Wang, Q. Sun, and L. Xu, "Development of an Integrated Cooling System Controller for Hybrid Electric Vehicles," *J. Electr. Comput. Eng.*, vol. 2017, pp. 1–9, Apr. 2017.

[63] TDK Corporation, "Flex Crack Countermeasures in MLCCs (Multilayer Ceramic Chip Capacitors)," 2019. [Online]. Available: https://product.tdk.com/info/en/products/capacitor/ceramic/mlcc/technote/solution/mlcc02/index.html.

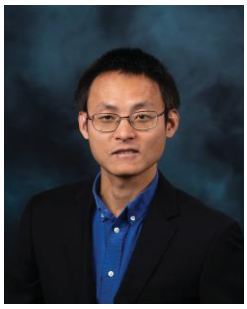
[64] Richardson RFPD, "Power Capacitors Selection Guide for Energy Storage & Power Conversion Applications," 2018. [Online]. Available: http://www.richardsonrfpd.com/resources/RellDocuments/SYS_31/Capacitor_Selection_Guide.pdf.

[65] Rubycon Corporation, "Caution for Proper Use of Film Capacitors." p. 2, 2017.

[66] S. Wang, "Modeling and Design of Planar Integrated Magnetic Components," MS Thesis, Virginia Polytechnic Institute and State University, 2003.

[67] P. Fay, "Chapter I: Introduction to Microwaves and RF," in *RF and Microwave Applications and Systems*, 2nd ed., M. Golio and J. Golio, Eds. CRC Press, 2008, pp. I–6.

[68] A. I. Pressman, K. Billings, and T. Morey, "Chapter 2 Push-pull and forward converter topologies," in *Switching power supply design*, 3rd ed., McGraw-Hill Education, 2009, p. 64.
[69] M. A. Swihart, "Inductor Cores – Material and Shape Choices," *Magnetics Inc.*, 2018. [Online]. Available: https://www.mag-inc.com/getattachment/Design/Design-Guides/Inductor-Cores-Material-and-Shape-Choices/Inductor-Cores-Material-and-Shape-Choices-08142013.pdf?lang=en-US.
[70] Chang Sung Corporation, "Magnetic powder cores Ver.13." [Online]. Available: http://www.mhw-intl.com/assets/CSC/CSC_Catalog.pdf.
[71] Hitachi Metals, "Mn-Zn Ferrite Core loss data (1000-3000kHz)," 2016.
[72] Hitachi Metals, "High Performance Amorphous Powder Core HLM50 Series," 2017. [Online]. Available: https://www.hitachi-metals.co.jp/products/elec/tel/pdf/hl-fm35.pdf.
[73] Magnetics Inc, "Powder Core Loss Calculation," 2018. [Online]. Available: https://www.mag-inc.com/Design/Design-Guides/Powder-Core-Loss-Calculation.
[74] Magnetics Inc, "Curve Fit Equation Tool," 2018. [Online]. Available: https://www.mag-inc.com/Design/Design-Guides/Curve-Fit-Equation-Tool.
[75] Magnetics Inc, "Learn More about Ferrite Shapes," 2018. [Online]. Available: https://www.mag-inc.com/Products/Ferrite-Cores/Ferrite-Shapes/Learn-More-about-Ferrite-Shapes.
[76] Magnetics Inc, "Planar E Core OR49938EC Datasheet," 2018. [Online]. Available: https://www.mag-inc.com/Media/Magnetics/Datasheets/0R49938EC.pdf.
[77] R. W. Erickson and D. Maksimović, "Chapter 13 Basic Magnetic Theory," in *Fundamentals of Power Electronics*, Springer, 2001, p. 500.
[78] R. A. Clarke, "Effective Length," *Magnetism: quantities, units and relationships*, 2014. [Online]. Available: http://info.ee.surrey.ac.uk/Workshop/advice/coils/terms.html#eflen.
[79] Robert W. Erickson and D. Maksimović, "Chapter 14: Inductor Design," in *Fundamentals of Power Electronics*, Springer, 2001, p. 542.
[80] Hitachi Metals, "Material： ML29D," 2016.
[81] TDK Corporation, "Film Capacitors Metallized Polypropylene Film Capacitors (MKP)." [Online]. Available: https://www.tdk-electronics.tdk.com/inf/20/20/db/fc_2009/MKP_B32674_678.pdf.



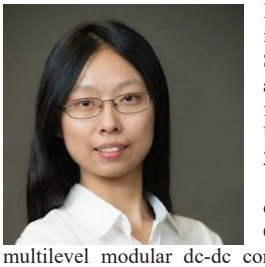
Ze Ni (S'16) received his B.S. degree from Hubei University of Technology, Wuhan, China, in 2010 and M.S. degree from Harbin Institute of Technology, Shenzhen, China, in 2013, both in Electrical Engineering. From 2013 to 2015, he worked on 10 kV Static Synchronous Compensator in Shenzhen. Since January 2016, he has been a Ph.D. student in North Dakota State University, Fargo, ND, USA. He is currently working at Oak Ridge National Laboratory as a research intern.

His research interests include wide-bandgap device reliability and applications, switched-capacitor resonant converter and multilevel inverter.

Yanchao Li (SM'15-M'19) received his B.S. degree from Southwest Jiaotong University, Chengdu, China, in 2012. He received the M.S. degree in Electrical and Computer Engineering from NYU Tandon School of Engineering, United States, in 2014. And he received his and Ph.D. degree from North Dakota State University, United States, in 2019. He has joined AzPower as application engineer since 2019. He once worked in Philips Lighting North America Corporation as a design engineer intern, in 2014.

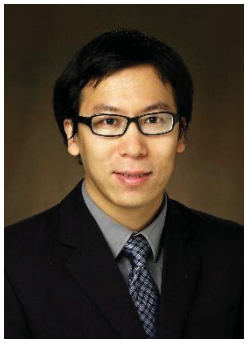
His main research interests include SiC and GaN devices based power converters for data center, power grid and electric vehicle applications, such as modular multilevel dc-dc converter, high density and high efficiency dc-dc converter, grid connected inverter, PMSM motor drive and LED driver.

Chengkun Liu (S'19) received B.S. degree in Computer Science in 2010 and M.S. degree in Mechatronic engineering in 2015 both from Beijing University of Posts and Telecommunications, Beijing, China. He worked at Power Department, China Aerospace Science and Industry Corporation as an electrical engineer for two and half years. He used to work on 100kW, 400Hz inverter and 3kW UPS. He is currently pursuing a Ph.D. degree in electrical engineering at University of Dayton. His research focus on reliability and power converter about wide bandgap devices.



Mengxuan Wei (S'18) received the B.E. degree in electrical engineering and automation from Sichuan University, Chengdu, China, in 2015, and the M.S. degree in electrical engineering from State University of New York (SUNY) University at Buffalo, Buffalo, NY, USA, in 2017.

She is currently pursuing the Ph.D. degree in electrical engineering at University of Dayton, OH, USA. Her research interests include multilevel modular dc-dc converter application, high-power density high-efficiency dc–dc converter application and wide bandgap devices application.



Dong Cao (M'09) received the B.S. degree from Zhejiang University, Hangzhou China, in 2005, the M.S. and Ph.D. degrees in electrical engineering from Michigan State University, East Lansing USA, in 2010 and 2012, respectively. He worked at Ford Motor Company as a core power electronics engineer for hybrid electric vehicle electrified driveline hardware development from 2012 ~ 2014. He was an assistant professor at North Dakota State University from 2014 ~ 2019. He joined University of Dayton at as GE EPISCenter professor and associate professor in since Aug. 2019.

His research interests include high power or high frequency wide bandgap devices i.e. SiC or GaN smart gate drive and their applications; high density and high efficiency power conversion for data center, LED driving, electric grid, solar farm, electric vehicle and electrified airplane applications; health monitoring and lifetime prediction of power converters using artificial intelligence. He received three prize paper awards from IEEE. He received a couple of presentation and poster awards from IEEE conference. He is the associated editor and guest editor for several IEEE Journal and Transactions.