Mobility extraction of air stable p-type polythiophene field effect transistors fabricated using oxidative chemical vapor deposition

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Keywords: polythiophene; oxidative chemical vapor deposition (oCVD); field effect transistors (FETs); mobility; organic semiconductors

Abstract

We report on the air stable organic field effect transistors (FETs) based on unsubstituted polythiophene (PT) channel, processed using oxidative chemical vapor deposition. The intrinsic properties of PT, including rigid backbone structure and resistance to reactions with water and oxygen, lead to the excellent air stability of the oCVD PT-based FET devices. Further, the effect of channel/metallization contact resistance on the extraction of field effect mobility (μ_{FE}) of PT-based FETs is investigated. Due to the channel/metallization contact resistance, the actual voltages applied to the channel is found to be significantly lower than the intended drain bias because of the voltage drops occurred at the source/drain contacts. Transmission-line measurements reveal that greater than 30% of the intended drain bias is lost at all gate voltages applied to the channel. Re-constructed output characteristics excluding the contact effect allow for extracting corrected μ_{FE} which is approximately 40% higher than that with contact resistance.

1. Introduction

In recent years, organic semiconductors have been garnering considerable attention for use in electronic and optoelectronic devices due to their low cost, mechanical flexibility and easy tuning of materials properties[1-4]. Organic semiconductors have been implemented in various devices, including organic solar cells[2], batteries[5], fuel cells[6] and electrochromic devices[7-8]. Efforts also have been made to employ organic materials as channels in thin film field effect transistors (FETs)[3]. Although most of organic materials for this application demonstrated the field effect mobility ranging from 10^{-6} to 10^{-2} cm^2/Vs [3], more recent advancements from novel materials design and carefully controlled device fabrication have led to a significant enhancement in mobility. Approximately 0.05 cm^2/Vs was achieved with poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (known as PEDOT:PSS)[9], ~ 0.2-4 cm^2/Vs with small molecules such as pyrene[10] and pentacene[10], ~0.6-10 cm^2/Vs with donor-acceptor polymers[11-13]. However, the majority of these organic FETs need to operate in a vacuum, or inert gas environment since many of these organic materials are not stable in air over time. This air instability has been reported due to trapping molecular species such as oxygen and/or water (i.e., reaction with oxygen and water) at crystalline boundaries (if channel is a crystalline material), nano-scale porosity, or at the channel/dielectric interface for FET application[14-15]. Achieving stable device performance over time in air is the next crucial challenge for the implementation of organic semiconductors for real world device applications. There have been efforts to mitigate the issue of air instability by employing postprocessing thermal annealing[16]; single or bilayer encapsulations to decelerate the diffusion and reaction kinetic rates for water and oxygen[14, 17]; the use of molecular additives to passivate the defect sites[18]. Although these reported methods made some enhancement in air stability for organic FET devices, the suggested solutions require

one or more additional process steps and treatments that often deteriorate material properties during the application of annealing and/or deposition of encapsulation layers. Further, additives may act as scatter centers that limit carrier transport in channel materials. Therefore, realizing intrinsically air-stable organic semiconductors is expected to contribute, in ways of sustainable device performance and cost-effectiveness, to the field of organic electronics such as organic solar cells, sensors and displays that are supposed to be exposed to air during actual operation.

Oxidative chemical vapor deposition (oCVD) has emerged as a technique to synthesize, deposit and dope polymeric materials in a single step process[19-20]. The vapor phase oCVD technique provides excellent uniformity, high conductivity, the ability to control film thickness in a simple way and capability of large area deposition. In addition, the oCVD technique tune, in a facile way, the doping level of the resulting polymers during deposition *in situ* by adjusting substrate temperature and varying oxidizing agents and *ex situ* by post treatments such as acid rinsing. The vapor phase oCVD process allows for expanding the number of processable polymers, due to no requirement of monomer solubility in solvents[21]. Further the oCVD technique enables polymer depositions on virtually any substrates since the oCVD technique require no film wetting on substrates.

In this study, the oCVD technique was used to promote organic FET device applications, particularly by employing unsubstituted polythiophene (PT) as an FET channel material. Polythiophene has been difficult to process through solution-based techniques, which is primarily due to its insoluble nature. Recently, however, we demonstrated[21-22] the successful synthesis of PT and its integration into FETs with the carrier density of 10^{16}-10^{18} /cm^3 and the

field effect mobility of ~ 10^{-4} - 10^{-2} cm^2/Vs, depending on the degree of conjugation of PT films and external stimuli such as light[22]. This present study focuses on the important effect of the interfacial contact resistance on the measurement of field effect mobility of PT-based FETs, and a strategy to accurately extract the field effect mobility is suggested. Further, the intrinsic air-stable nature of the oCVD PT is discussed and the air stable performance of the oCVD PT-based FETs will be presented.

2. Experimental

Detailed procedures of the oCVD PT synthesis and deposition processes can be found elsewhere[21-22]. Briefly here, unsubstituted thiophene monomer (≥99%, Sigma-Aldrich) was evaporated from a jar outside the oCVD chamber, at room temperature (25 °C), and the vapor was introduced to the chamber through a valve-operated gas line. The oxidizing agent, iron chloride ($FeCl_3$, 97%, Sigma-Aldrich) was sublimated in the chamber at 200 °C (a ramping rate of ~5 °C/min used), which was used to initiate the oxidative polymerization of PT and also to dope PT for p-type conductivity. The resulting PT was deposited onto glass and silicon substrates with no intentional substrate heating. A rotating substrate stage was used at a rate of 5 rpm to enhance surface uniformity of PT films. After the oCVD PT depositions, the samples were rinsed with diluted (0.2M) HCl for 5 mins followed by a MeOH rinse for longer than 10 mins to remove unreacted monomers and residual oxidizing agents, and then dried in air.

Bottom-gated PT-based FETs with transmission line patterns were fabricated on heavily-doped Si substrates (0.003-0.005 Ωcm) with shadow masks for the oCVD PT channel (~35 nm) and silver source/drain metallization (~65 nm). Silver was thermally evaporated on top of the PT

channel through a shadow mask as metallization and at a substrate rotation speed of 5 rpm without substrate heating. For the dielectric, thermally grown SiO_2 with a thickness of 50 nm was employed to limit the gate leakage current at a reasonably low level during device operation and the resulting SiO_2 shows a smooth and uniform surface for the deposition of the oCVD channel PT. Gate back side contact was made with Ag paste after scratching the heavily-doped Si wafer surface with a diamond scriber to ensure the removal of any native oxides and exposing heavily-doped region of the substrate. The transistor device performance was evaluated with an Agilent B1500 semiconductor parameter analyzer in a light tight probe station in air at room temperature.

For the investigation of interfacial contact properties between the channel PT and metallization and the contact effect on the measurement of the field effect mobility, transmission line measurements were made on the oCVD PT-based FETs as a function of channel length (L=60, 100 and 200 μm used in this study) with a fixed channel width of 1000 μm. More than 100 oCVD PT-based FET devices were fabricated and measured for the analysis.

3. Results and Discussion

The oCVD technique allows for a facile synthesis and deposition of unsubstituted polythiophene of which the monomer is insoluble in solvents and therefore has been difficult to synthesize through the conventional solution-based methods. Our group, recently, demonstrated excellent stability of oCVD PT in air over time[22] of which the air-stability is attributed to the rigid back bone structure of the PT. This rigid feature leads to the low reactivity with water and oxygen in air as well as the insoluble nature in solvents. Therefore, achieving stable FET and other device

performance that utilizes organic semiconductors may benefit from the oCVD technique; as it is able to synthesize and process insoluble but rigid materials, which are potentially stable in air. A schematic of the gate-down test FET device is presented as an inset in Figure 1(a) where the device employs an oCVD PT channel (35 nm), SiO_2 gate dielectric (50 nm), heavily-doped Si gate, and Ag as the source/drain metallization (65 nm); with channel width (W) and length (L) aspect ratio of W/L=1000 μm /200 μm. Output characteristics of drain current (I_D) vs drain bias (V_D) were evaluated as a function of gate bias (V_G), in the usual way, by sweeping drain bias, from 0 to -25 V and the gate bias from 12 to -15 V in -3 V steps for p-type channel FET devices. Resulting typical I_D-V_D plots, shown in Figure 1(a), demonstrate well-saturated drain current behaviors and clear on-and-off state characteristics. In order to confirm ohmic contacts between channel and metallization, I_D-V_D properties were evaluated at a small range of drain bias from -0.7 to 0.7 V and they are shown in Figure 1(b). No current crowding is observed and the drain current increases linearly with increasing drain bias, which verifies that ohmic contacts were made at the channel/metallization. Transfer characteristics serve as another indicator to evaluate the FET performance by measuring I_D as a function of V_G at a fixed drain bias, V_D = -0.2 V in this study. Drain current, I_D relates field effect mobility (μ_{FE}), device aspect ratio (W/L), oxide capacitance (C_{ox}= 6.903 x 10^{-8} F/cm^2 for 50 nm SiO_2) and FET threshold voltage (V_{Th}) with V_G and is defined by the metal-oxide-semiconductor FET (MOSFET) equation for $V_D << (V_G-V_{Th})$ [23]:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}\left[(V_G - V_{Th})V_D - \frac{V_D^2}{2}\right] \qquad (1)$$

$$\approx \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{Th})V_D \qquad (2)$$

A typical plot of log (I_D) vs V_G of the devices is displayed on the right axis of Figure 1(c) from which the device on/off ratio is determined to be approximately 10^3 by estimating from the

lowest I_D to the highest I_D in the plot, which is comparable to other organic FET devices[12, 24]. The left axis of Figure 1(c) depicts linear I_D *vs* V_G curve, where the μ_{FE} is derived from the slope of the linear portion of the curve, while V_{Th} is extracted from the intercept between extrapolation of the linear portion of the I_D-V_G curve and zero drain current. The determined saturation mobility and threshold voltage are μ_{FE} = 4.7±1.09 x 10^{-3} cm^2/Vs and V_{Th} = -1.14±0.41 V. The field effect mobility and threshold voltage were also measured from the saturation regime and the values are similar to those measured in the linear regime as ~4.3 x 10^{-3} cm^2/Vs and -1.02 V, respectively. The FET device performance obtained from oCVD PT is considered competent, compared with those of most reported organic semiconductor-based FETs: (1) the threshold voltage is the required bias to switch device on- and off-state and, therefore, values near zero for V_{Th} are desired. The measured small threshold voltages (-0.6 to -1.2 V that are enhanced or comparable to those of state-of-the-art organic FETs[10, 25]) is of important relevance to various electronic devices such as portable sensors and biomedical testers that require low operation voltages. (2) the field effect mobility achieved, ~5x10^{-3} cm^2/Vs is comparable to the mobilities (~<10^{-6}-10^{-2} cm^2/Vs) of the majority of organic channel FETs found in the literature[3, 26-27] and slightly less than that of current-standard amorphous Si-based FETs (~10^{-2}-1 cm^2/Vs)[10]. Although the novel synthetic and processing strategies are not yet trivial and not available for large area applications, some organic FET studies demonstrated high field effect mobility over 10 cm^2/Vs by utilizing an alternating donor-acceptor moiety (N-alkyl diketopyrrolopyrrole) as channel[28] and by off-center spin-coating to produce a highly aligned organic semiconductor (2,7-dioctyl[1]benzothieno[3,2-b][1] benzothiophene)[29-30].

Transmission line measurements (TLM) were made on a series of PT-based FETs at channel lengths (L) of 60, 100 and 200 μm. The TLM method requires the followings to validate the measurements and the PT devices in this investigation satisfy all the requirements: (i) horizontal contact geometry, (ii) linear resistance between metallization and channel, (iii) low resistivity metallization, (iv) identical sheet resistance underlying the contact to that outside contact (i.e., uniform channel resistivity), and (v) planar contact with $L_C/L_T \geq 2$, where, L_C is the source/drain contact length (L_C=400 μm fixed in this study), L_T is the transfer length which indicates the effective source/drain contact length; the ratio $L_C/L_T \geq 4$ in this study [31-33]. In a series model of resistance, total resistance (R_{Total}), which consists of two contact resistances ($2R_C$) at the two terminals (*i.e.*, source and drain) and channel resistance ($(R_S \cdot L)/W$) as described in Equation (3), was extracted using Ohm's law in the linear portion of the output characteristics (V_D = -0.2 V in this study) as a function of channel length and gate bias applied:

$$R_{Total} = 2R_C + \frac{R_S}{W} L \qquad (3)$$

where R_S is the channel sheet resistance from which the channel conductivity is determined with channel thickness (t) using the equation, resistivity $\rho = R_S \times t$.

Linear curves of R_{Total} *vs* L are shown in Figure 2 with gate bias ranging from 0 to -15 V. From Equation (3), contact resistance is simply determined from the y-axis intercept and the resulting contact resistance at the two terminals ($2R_C$) is plotted on the left side of Figure 3.

The contact resistance ($2R_C$ to account for both contacts at source and drain) was measured to be relatively large as 48.12 Mohm at zero gate bias, then monotonically decreases with increasing gate bias (negatively) on the left axis of Figure 3 and the $2R_C$ was extracted to be 10.75 Mohm at V_G = -15 V. An increase in negative gate bias injects more holes in the PT channel and therefore

the increased hole carrier density accounts for the observed decrease in contact resistance[33-34]. In order to specify the portion of contact resistance in the total resistance at each gate bias, the ratio of $2R_C/R_{Total}$ *vs* V_G is shown on the right axis of Figure 3. At all the gate bias applied, the $2R_C/R_{Total}$ ratio is greater than 30% at gate voltages (at V_G = 0 and -3 V, $2R_C/R_{Total}$ > 40%). The high contact ratios of 30-40% indicate that a significant portion of drain bias is lost due to large contact resistance at the two channel/metallization interfaces (i.e., source and drain). In equation (1) and (2), drain current, drain bias and field effect mobility are closely interrelated, which implies that the field effect mobility may be significantly underestimated due to the 30-40% lower drain bias (effective drain bias) applied to channel.

The current high contact resistance can be mitigated by aligning work functions between channel and metallization in order to achieve better ohmic contact and also minimizing the potential barrier between dissimilar materials that often limits charge flows at the barrier. Another practical strategy is to provide a thin buffer layer (in general, thickness < 10 nm for a buffer layer) between the channel PT and metallization. The buffer layer is preferred to have higher carrier concentration than the channel to buffer the large difference in carrier densities at the channel/metallization interface[33-34]. In addition, the buffer layer should also provide favorable interfacial compatibility with channel PT. Therefore, conducting polymers with higher conductivity than that of PT such as doped poly(3,4-ethylenedioxythiophene) (i.e., PEDOT) are expected to enhance the contact properties. Further studies of mitigating the high channel/metallization contact resistance by using oCVD PEDOT as a buffer are underway.

In order to investigate the effect of the contact resistance on the performance of the PT-based FET devices, the output characteristics shown in Figure 1(a) were re-constructed at each gate

voltage to reflect the effect of gate bias modulation on the contact resistance and drain current, by which the large contact effects were excluded. Effective drain bias (V_{ef}) was determined with the extracted contact resistance using the equation[35] below:

$$V_{ef} = V_D\left(\frac{R_{Total}-2R_C}{R_{Total}}\right) \qquad (4)$$

Re-constructed drain current (dotted for V_{ef}) is higher than that with contact effects (solid for V_D) in Figure 4 of the I_D-V curves. The field effect mobility of the PT FETs was re-calculated using the same MOSFET equation from the re-constructed characteristics, which allows for identifying the effect of the large and modulating contact resistance on the measurement of field effect mobility. Note that since the calculated effective channel voltage (V_{ef}) is based on TLM measurements where the R_{total} (i.e., $2R_C$ + channel resistance) was extracted in the linear regime of the output characteristics at V_D = -0.2 V. Therefore, the values of R_{Total} and R_C in Eq. (4) are most reliable at V_D = -0.2 V in the linear regime where the field effect mobility is determined. The re-evaluated field effect mobility excluding the contact effect is determined to be 6.31 x 10^{-3} cm^2/Vs, which is ~40% higher than that including the contact effect. The simple series resistance model used in this study proposes a general method to calculate a correct mobility and suggests that performance of organic semiconductor-based TFTs can be further improved by developing metallization strategies to reduce contact resistance between channel and source/drain metallization.

Although some recent studies implemented extrinsic strategies, such as post-process treatments, single or bilayer encapsulation and use of molecular additives, to enhance air stability, still the majority of organic semiconductors (small molecules and polymers) and their FET devices degrade their electrical properties such as conductance and carrier transport upon exposure to air.

Uptakes of water and oxygen that promote the recombination events between holes and delocalized electrons for most p-type organic semiconductors have been reported to be in charge of the degradation for conductivity and mobility in air over time [19, 36-37].

Overall performance of the oCVD PT-based FET devices were monitored over 90 days in air to investigate the air stability of the devices, and no significant changes in output and transfer characteristics were observed. Two major performance factors, i.e., threshold voltage and field effect mobility that surrogate FET device stability in air are shown in Figure 5(a) and (b), respectively. Note that the field effect mobilities plotted in Figure 5(b) are the corrected values according to the TLM measurements and the re-calculated output characteristics presented in Figure 4. These two device properties measured during the period are similar to their initial values, which implies that the oCVD PT and its FET application show excellent air stability. Over the course of air exposure for 90 days, no significant changes in contact resistance was observed either since the overall device performance remained nearly the same during the air exposure.

The thermal stability of PT at elevated temperatures, ranging 20 to 160 °C, was also investigated through *in-situ* electrical measurements from PT-based TFTs[20]. The conductivity of the oCVD PT with carrier density of ~10^{17} /cm^3 was thermally activated to increase from 2.77 × 10^{-5} S/cm at room temperature to 4.36 × 10^{-4} S/cm at 160 °C with an activation energy of 48 meV, of which the value is within the hopping conduction range[20, 38-39]. The conductivity at each temperature was maintained nearly constant during the *in-situ* measurements for longer than 2 hours, which indicates that the excellent thermal stability in air was achieved for the oCVD PT up to 160 °C. During the elevated temperature measurements, both the on- and off-state currents of the FETs increased, as expected, due to the enhanced conductivity. Further, it should be noted

that the demonstrated air stability of oCVD PT is an intrinsic nature of the material unlike those shown in other reports [16, 40] that extrinsically enhanced air stability with post-process thermal annealing, encapsulation layers to slow down diffusion kinetics or molecular additives, all of which require additional process costs and time, reduce the yield rate of materials and/or damage the materials during additional processes. The intrinsic air stability of the oCVD PT is attributed to the use of unsubstituted thiophene monomer resulting in the substantially rigid polymer backbone structure in oCVD PT that enhances resistance to reactions with other molecules including water and oxygen and to the rotation of unsubstituted monomers[3, 41-44]. Therefore, the air stable PT achieved through the oCVD technique is expected to be a useful asset for air stable organic electronic device applications such as organic solar cells and sensors as well as thin film FETs that are to be unavoidably exposed to air during actual device operations.

4. Conclusion

Air stable unsubstituted polythiophene was synthesized using oCVD and integrated into bottom-gated thin film FET devices. The demonstrated air stability is an intrinsic nature of the oCVD PT that is attributed to the processability of unsubstituted thiophene monomer, which has been challenged, that leads to the rigid backbone structure and the enhanced resistance to reactions with water and oxygen. This study also focuses on the effect of contact resistance at the channel/metallization interface on the extraction of field effect mobility and the results reveal that high contact resistance may significantly underestimate the mobility due to huge voltage drops at the source and drain contacts. A simple but general approach to the extraction of the corrected field effect mobility was used based upon the series resistance model. According to this approach, the field effect mobility of the oCVD PT-based FETs is approximately 40%

higher than the measured values reflecting contact resistance. This suggests that a further enhancement in organic FET performance can be achieved by engineering channel metallization contact interface to have chemically compatible metallization materials and lower contact resistance interface.

Acknowledgements

The authors gratefully acknowledge the financial support from Purdue University. The materials and device characterizations were partially supported by National Science Foundation (NSF) grant No. ECCS-1931088. H.W.S. acknowledges partial support from the Improvement of Measurement Standards and Technology for Mechanical Metrology (Grant No. 19011032). N. K. acknowledges support from the Basic Science Research Program (NRF-2018R1A2B6002194) through the NRF Korea funded by the Ministry of Science and ICT.

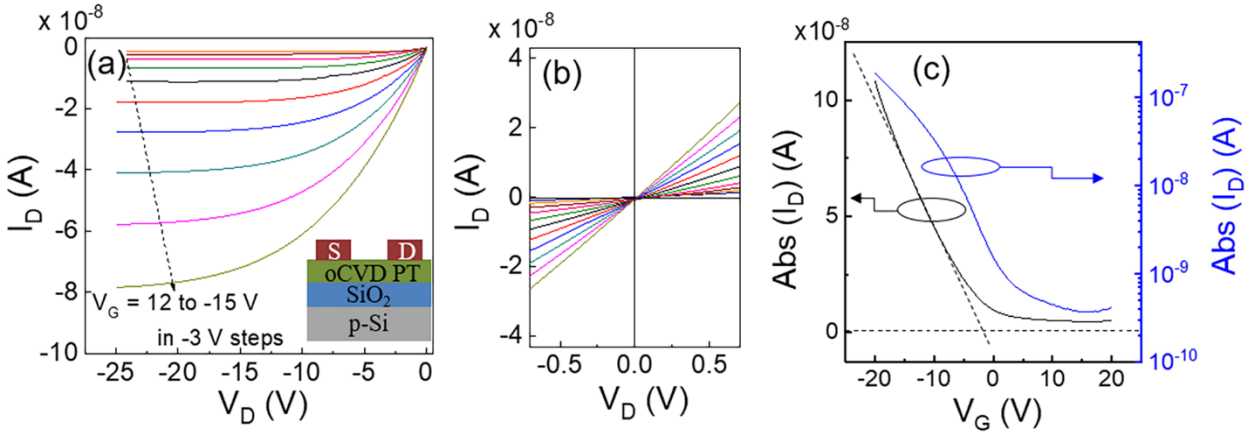

Figure 1. oCVD PT-based typical FET performance: (a) I_D-V_D output characteristics, (b) ohmic contact behavior with linear I_D-V_D of oCVD PT/Ag channel/metallization and (c) transfer characteristics. The inset in (a) shows a schematic side view of the FET device.

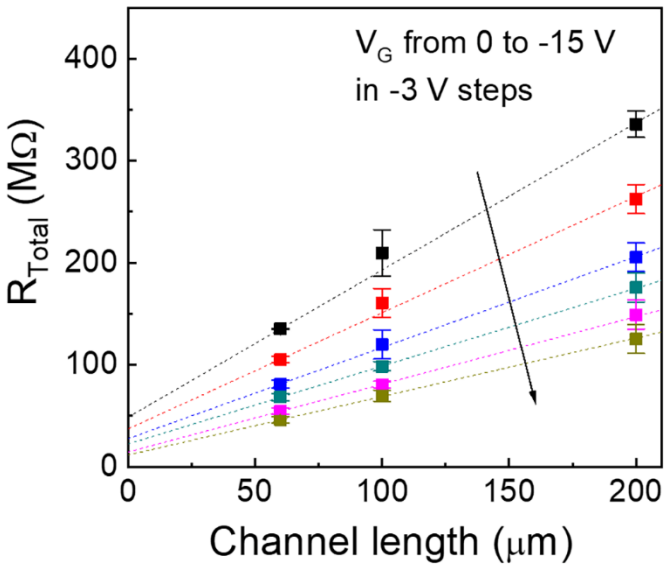

Figure 2. Total resistance (R_{Total}) vs channel length (L) as a function of gate bias (V_G) ranging from 0 to -15 V in -3 V steps.

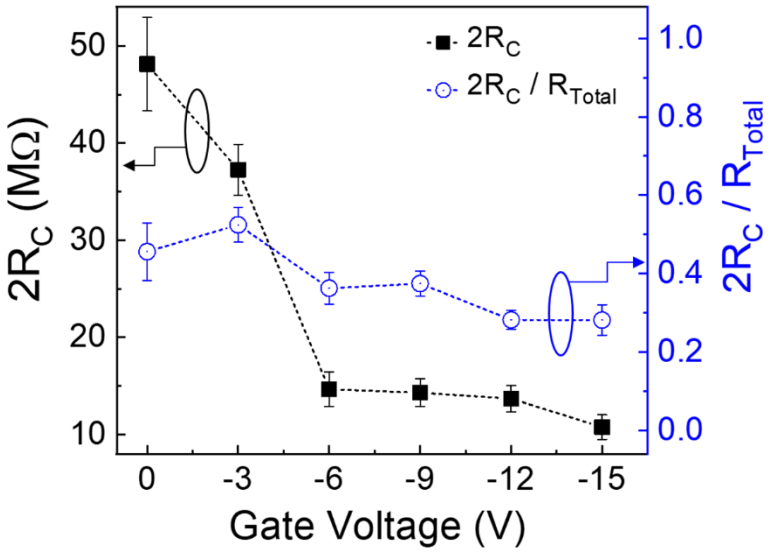

Figure 3. Contact resistance ($2R_C$ for the two terminals of source and drain) on the left axis and the ratio of contact resistance over total resistance ($2R_C/R_{Total}$) as a function of gate bias

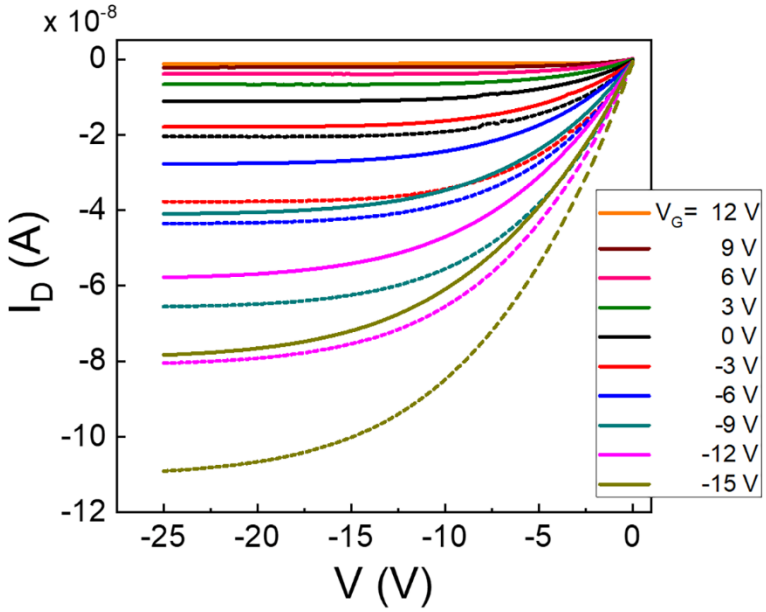

Figure 4. Experimentally obtained I_D *vs* V_D characteristics reflecting contact resistance (solid) and corresponding I_D *vs* V curves corrected using the series resistance model excluding contact resistance (dotted).

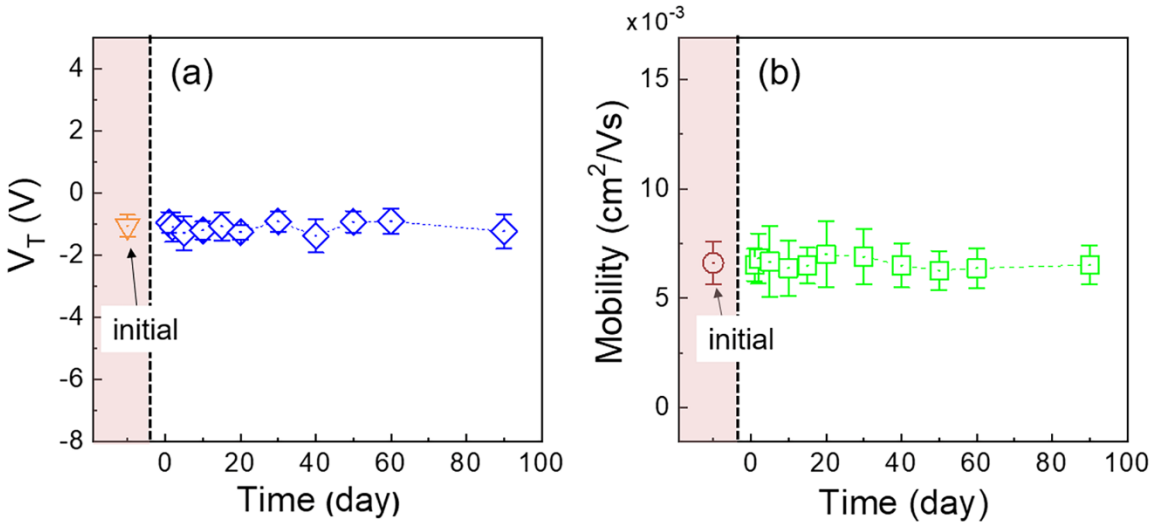

Figure 5. Air stability of the PT-based organic FET devices: (a) changes in threshold voltage and (b) field effect mobility (corrected) as a function of time, compared to its initial values where no significant instability is observed in both threshold voltage and field effect mobility, which implies that the PT channel and its FET devices present excellent air stability over time.

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