

The Adiabatically Driven StrongARM Comparator

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Abstract—Adiabatic logic, also known as charge recovery logic, is subject to active research in the field of low-energy computation. Although the principles of adiabatic operation are well understood in digital circuits, analog and mixed-signal circuit implementations are largely unexplored. In this work, it is shown that the StrongARM comparator can take advantage of adiabatic principles by i) being powered by a sine-wave, the power-clock, rather than the conventional DC power supply, V_{DD} , and ii) using an adiabatic buffer as the output stage, rather than an SR-latch. Post-layout simulations in a 65nm technology show that the adiabatically driven StrongARM has similar characteristics to the traditional strongARM: +2% noise, +1% input offset voltage, while only consuming between 28% and 55% of the energy of the traditional StrongARM.

Index Terms—Comparator, ADC, charge recovery comparator, adiabatic comparator, adiabatic logic, charge recovery logic, charge recovery circuits.

I. INTRODUCTION

In modern integrated circuits, digital data is represented as a set of node voltages that change state thanks to the movement of electric charge. A logic gate is responsible to charge, or discharge, a given node (output), depending on the charge distribution of a set of other nodes (inputs). The energy dissipated on the transistors, acting as switches, is converted to heat through joule effect. Adiabatic logic achieves energy reduction with respect to static CMOS by i) gradually charging output nodes and ii) recycling the charge that is used to store information on node capacitances. In order to do so, time varying signals, called power-clock (PC), usually sine-waves, are both responsible for supplying energy and timing to each logic gate. Depending on the logic family, there can be two, four, or more power-clock signals that needs to be synchronized between each other, hence the common definition of two- or four-phase logic family.

Recently, adiabatic principles were used for the first time to design mixed-signal circuits, in the form of two different topologies of comparators [1], [2]. The development of an adiabatic comparator, a fundamental building block of many analog-to-digital converters (ADC), enables the design of fully adiabatic System-on-Chips, increasing the applications in which such systems can be deployed. The strongARM is a mixed-signal circuit that can be used as a latch, sense amplifier, and comparator [3]. Originally introduced in [4] as a sense amplifier, this circuit takes the name from its use in the strongARM microprocessor. In this work, the principles of adiabatic logic are used to decrease the energy consumption of strongARM comparator [3], by way of using a power-clock signal instead of the traditional V_{DD} power supply.

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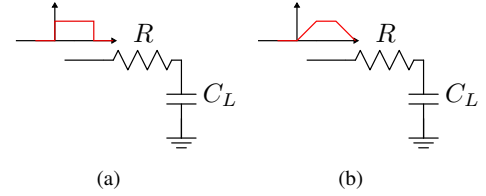


Fig. 1. Charging a capacitance (a) abruptly, and (b) adiabatically.

The engineering task of generating the power-clock phases and synchronizing them is known for all adiabatic circuits in literature, and not exclusive to the proposed adiabatically driven comparator in this brief. Generation of efficient and synchronized power clocks is a research area in its own, such as in [5]. From a performance analysis point-of-view, an adiabatic system will have the power-clock signals routed globally on chip, and the effects of routing the power-clock are rightfully excluded from the performance analysis of individual components in literature. The performance of a system-level implementation will ultimately depend on the combined energy and energy efficiency of the adiabatically-driven (mixed-signal and/or digital) circuit components, as well as those of the global power and clock distribution networks. The comparator circuit analysis in this brief is very encouraging to the continued investigation of these system-level performance behavior in future work.

The remainder of this article is organized as follows: Section II presents the fundamental principles behind adiabatic logic. Section III reviews the traditional strongARM comparator, or SA. Section IV shows the adiabatically driven strongARM comparator, or ADSA. Section VI shows results from post-layout simulations, comparing the proposed adiabatically driven strongARM with the traditional strongARM. Section VII concludes the paper.

II. ADIABATIC PRINCIPLES

Figure 1 shows two different ways of charging and discharging a capacitance C_L through a resistance R : abruptly (with a square-wave) or adiabatically (with a trapezoidal-wave). In the first case, Figure 1(a), the energy E_C dissipated on the resistance is:

$$E_C = C_L V_{DD}^2 \quad (1)$$

where V_{DD} is the magnitude of the square-wave. The energy E_A dissipated on the resistance of Figure 1(b), on the other hand, is:

$$E_A = 8 \frac{C_L^2 V_{DD}^2 R}{T} \quad (2)$$

where V_{DD} and T are the magnitude and the period of the trapezoidal-wave, respectively [6]. For $T \rightarrow \infty$, the energy

dissipated on the resistance R becomes zero; that is the reason why the term *adiabatic* is used for this energy profile. If a sine-wave is used in place of the trapezoidal-wave, Equation (2) becomes:

$$E_A = \frac{\pi^2}{2} \frac{C_L^2 V_{DD}^2 R}{T} \quad (3)$$

where V_{DD} and T are the peak-to-peak voltage and the period of the sine-wave, respectively. Equation (1) describes the dynamic energy consumption of static CMOS, domino logic, and other traditional logic families, while Equation (3) is the dynamic energy consumption of charge recovery logic, also known as adiabatic logic [6]. In order for the adiabatic charge method of Figure 1(b) to consume less energy than the abrupt charge of Figure 1(a), the ratio E_A/E_C must be < 1 :

$$\frac{E_A}{E_C} = 8 \frac{C_L R}{T} < 1 \quad (4)$$

The latter inequality shows how, given the technology and design dependent values C_L and R , the proper waveform period can be chosen. One of the primary challenges of adiabatic logic implementations has been the scaling of frequency subject to this equation, while preserving the low-energy characteristics over traditional CMOS implementations [6].

III. THE TRADITIONAL STRONGARM (SA)

The operation of the traditional strongARM (SA) shown in Figure 2(b), can be divided in two phases: precharge and evaluation. During precharge, the clk signal is low, and transistors M_{P1} , M_{P2} , M_{P3} , and M_{P4} charge nodes X , Y , P , and Q to V_{DD} . Transistor M_0 is off, so the only path to ground is open. During the evaluation phase, when clk goes high, transistors M_{P1} , M_{P2} , M_{P3} , and M_{P4} turn off, and transistor M_0 starts to conduct. Transistors M_3 , M_4 , M_5 , and M_6 are initially off, because their drain to source voltages are zero. Transistors M_1 and M_2 are conducting, discharging nodes P and Q at different rates, depending on V_{in} . Once P and Q are at $V_{DD} - V_{TN}$, where V_{TN} is the threshold voltage of the NMOS, M_3 and M_4 start conducting as well, introducing feedback and increasing the gain of comparator. The charge on nodes X and Y can now flow towards ground, and when the voltages of X and Y are at $V_{DD} - V_{TP}$, where V_{TP} is the threshold voltage of the PMOS, transistors M_5 and M_6 start conducting as well. The two back-to-back inverters realized by transistors M_3 , M_4 , M_5 , and M_6 settle on one of the two stable states: $V_X = V_{DD}$ and $V_Y = 0$, or vice versa.

A. Energy Profile

From Equation (1), assuming that the comparator is symmetrical and ignoring the charge deposited on node S , the dynamic energy dissipated by the strongARM comparator, E_{SA} , during every cycle is:

$$E_{SA} = (C_{X,Y} + 2C_{P,Q})V_{DD}^2 \quad (5)$$

where $C_{X,Y}$ is the capacitance on nodes X and Y , and $C_{P,Q}$ is the capacitances on nodes P and Q . Capacitance $C_{X,Y}$ is not multiplied by 2 because during the evaluation phase, only X or Y is discharged to ground.

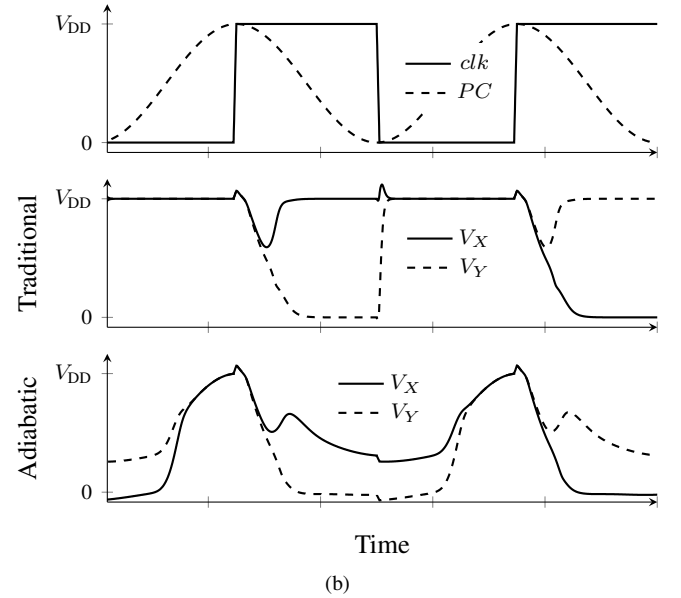
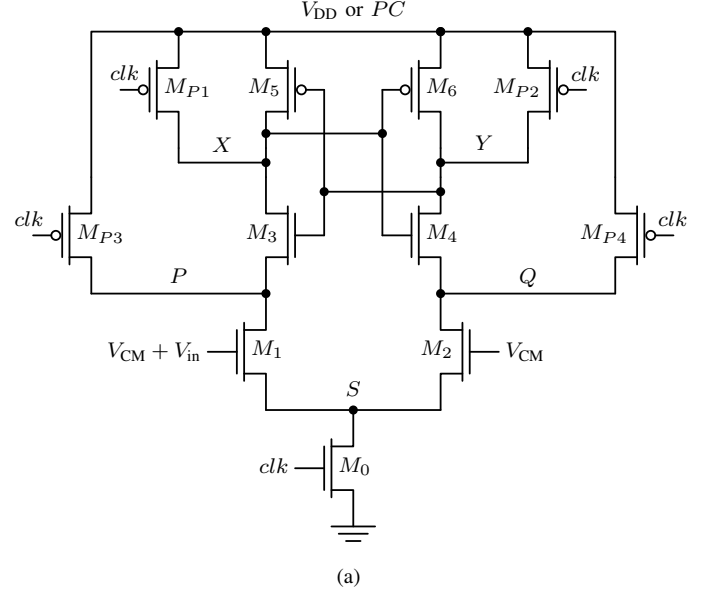


Fig. 2. The strongARM comparator, (a) schematic, and (b) its behavior when DC driven and adiabatically driven.

IV. THE ADIABATICALLY DRIVEN STRONGARM (ADSA)

The key idea of the proposed methodology is to use an adiabatic precharge in order to decrease the energy consumption of the strongARM comparator. In order to do so, a sinusoidal signal PC is introduced and replaces V_{DD} , as shown in Figure 2(a).

The operation of the ADSA of Figure 2(a) and its signals, Figure 2(b), can again be divided in two phases: precharge and evaluation. In the precharge phase, the clk signal is low, and transistors M_{P1} , M_{P2} , M_{P3} , and M_{P4} are conducting. Thanks to the slope of the rising edge of PC , nodes X , Y , P , and Q are adiabatically charged to V_{DD} . Transistor M_0 is off, so the only path to ground is open. The evaluation phase begins when clk goes high, just like in the SA. Signal clk is synchronized such that as soon as PC reaches V_{DD} , clk goes high: transistors M_{P1} , M_{P2} , M_{P3} , and M_{P4} turn off,

and transistor M_0 starts to conduct. Transistors M_1 and M_2 discharge nodes P and Q at different rates. Once P and Q are at $V_{DD} - V_{TN}$, M_3 and M_4 start conducting, and the charge on nodes X and Y can now flow towards ground. When the voltages of X and Y are at $V_{DD} - V_{TP}$, transistors M_5 and M_6 start conducting as well. Once again, the two inverters realized by transistors M_3, M_4, M_5 , and M_6 settle on one of the two stable states: $V_X = PC$ and $V_Y = 0$, or vice versa. The outputs of the ADSA, when operating at frequencies close to its maximum, are not rail-to-rail, but look like the signals of Figure 2(b). Because of that, the outputs of the ADSA are not suitable to drive adiabatic logic directly. In order to address this issue, a buffer must be used, not dissimilarly from the SR-latch needed for the traditional strongARM [3].

A. Energy Profile

The energy savings with respect to the SA comparator are primarily due to the precharge. In Figure 2(b), both X and Y are initially at zero, and thanks to M_{P1} and M_{P2} , both follow PC , hence charging adiabatically. When PC is at its highest magnitude, namely V_{DD} , clk goes high and starts the evaluation phase. At this point, the adiabatically driven strongARM behaves just like the traditional strongARM: node X is asserted high while node Y is asserted low. It is important to note that nodes Y, P , and Q are discharged to ground, abruptly, through transistors M_{3-4}, M_{1-2} , and M_0 , while node X is discharged adiabatically through M_5 , until $V_X \approx V_{TP}$.

Since the ADSA has an adiabatic precharge and also an abrupt discharge component, the dynamic energy consumption is a mix of the two energy profiles of Equations (1) and (3). The adiabatic component $E_{ADSA,A}$ is due to all nodes adiabatically charging to V_{DD} during the precharge phase, and that one output node is adiabatically discharged after the evaluation phase. Hence, following Equation (3):

$$E_{ADSA,A} = \frac{\pi^2}{4} (3C_{X,Y} + 2C_{P,Q})^2 V_{DD}^2 R_{on} / T \quad (6)$$

where R_{on} is the equivalent resistance of transistors $M_{P1}, M_{P2}, M_{P3}, M_{P4}, M_5$, and M_6 . T is the period of signals PC and clk . The non-adiabatic dynamic energy consumption $E_{ADSA,NA}$, following Equation (1), is:

$$E_{ADSA,NA} = \frac{1}{2} (C_{X,Y} + 2C_{P,Q}) V_{DD}^2. \quad (7)$$

For the sake of simplicity, it is assumed that $C_{X,Y} = 2C_{P,Q} = C_L$, so that the ratio of the total dynamic energy consumption of the adiabatically driven strongARM E_{ADSA} and the traditional strongARM E_{SA} is:

$$\frac{E_{ADSA}}{E_{SA}} = \frac{E_{ADSA,NA} + E_{ADSA,A}}{E_{SA}} = 0.5 + \frac{5}{6} \pi^2 \frac{C_L R_{on}}{T}. \quad (8)$$

The result of Equation (8) is a lower bound for the normalized dynamic energy consumption. In the best case scenario, i.e. $5/6 \pi^2 C_L R_{on} / T \ll 0.5$, the ADSA consumes only 50% of the traditional strongARM. In practice, there are two other effects that further decrease the total energy consumption of the adiabatically driven strongARM with

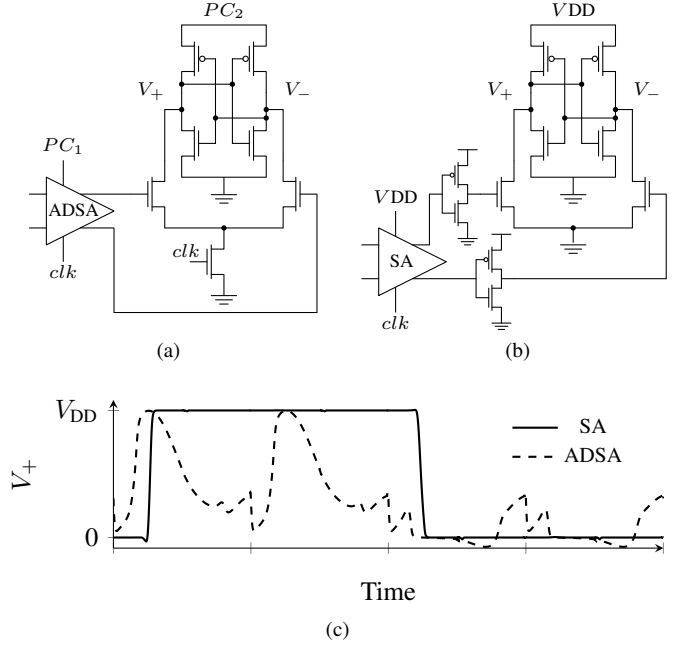


Fig. 3. Adjusting the output, (a) adiabatically driven strongARM and output buffer, (b) traditional strongARM and SR-latch, and (c) V_+ nodes.

respect to the traditional strongARM: i) the leakage, short-circuit, and kickback currents are modulated by PC , and ii) at high frequencies, the outputs of the ADSA are not rail-to-rail. The first effect comes from the fact that the adiabatically driven strongARM is powered by a sinusoidal signal with a DC component of $V_{DD}/2$, hence it is expected that the impact of leakage currents be smaller, since the average voltage that causes them is $V_{DD}/2$. When clk is going from high to low, transistors M_{P3}, M_1 , and M_0 provide a path from V_{DD} to ground. When adiabatically driven, the strongARM presents the same path between PC and ground, but since PC is low at that time, it prevents short-circuit energy consumption. The second effect occurs because during the evaluation phase, the output of the ADSA that is asserted high is not driven to V_{DD} , but to PC . Depending on the operating frequency, by the time the evaluation phase is concluded, PC can be at a lower voltage, hence the output node is not driven all the way up to V_{DD} . For example, with reference to Figure 2(b), during the first evaluation phase node X decreases until transistors M_3-M_5 turn on, then it is driven to PC , which at that point is $\approx 2/3 V_{DD}$. Though this effect lowers the energy consumption, it also signals the fact that the ADSA is operating close to its maximum frequency limit.

V. DRIVING THE OUTPUT

As mentioned in Section III, the traditional strongARM comparator needs a circuit to convert its outputs to suitable signals. The outputs of the SA are rail-to-rail but cannot be used directly to drive CMOS logic, because during precharge the outputs are both at V_{DD} , hence invalid. In order to convert the outputs to signals that are valid at all times, an SR-latch can be used [3]. On the other hand, the outputs of the adiabatically driven strongARM are not rail-to-rail at higher frequencies,

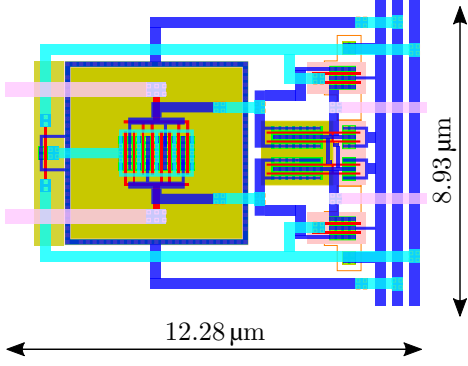


Fig. 4. Layout of the strongARM comparator.

TABLE I
TRANSISTOR DIMENSIONS

	M_0	M_1, M_2	M_3, M_4	M_6, M_5	$M_{P1} - M_{P4}$
W (μm)	0.4	4	3	0.75	0.75
L (μm)	0.06	0.06	0.06	0.06	0.06
Corr	—	0.75	0.75	0.75	0.75

and need to be recovered to full-swing. This is achieved by using an adiabatic buffer, as proposed in this work.

Figure 3 shows the buffer and the SR-latch for the adiabatically driven strongARM and the traditional strongARM, respectively. For the ADSA, Figure 3(a), the outputs of the comparator are connected to a circuit based on the PAL2N buffer [7], with the addition of a footer NMOS transistor connected to the *clk* signal, in order to reduce short circuit currents. The buffer of the ADSA is connected to another phase of the power-clock, PC_2 , as typically available in adiabatic logic [6]. For the traditional strongARM, Figure 3(b), the outputs of the comparator are inverted and then connected to an SR-latch [3]. Figure 3(c) shows the outputs of the buffered ADSA and of the latched traditional strongARM. The former signal is suitable to drive an adiabatic logic gate, while the latter is suitable to drive a static CMOS logic gate. The energy consumption and other characteristics of the output buffer and SR-latch are not reported as they do not impact performance as much as the strongARM comparator itself.

VI. EXPERIMENTAL RESULTS

The strongARM comparator of Figure 2 is implemented in a 65 nm technology with a nominal voltage of $V_{DD} = 1.2\text{ V}$, with the dimensions reported in Table I. The layout of the strongARM comparator has an area of about $36\mu\text{m}^2$, and is shown in Figure 4. The layout is used to estimate parasitics in order to simulate the circuits behavior more accurately, and the following data is obtained with extracted circuits, unless otherwise specified.

Figure 5 shows the energy consumption, per conversion, of the strongARM and the adiabatically driven strongARM comparators, for different *clk* frequencies, as well as the normalized energy, on the right axis. For operating frequencies in the range from 100 Hz to 500 MHz, the ADSA consumes less energy than the SA. At very low frequencies, namely

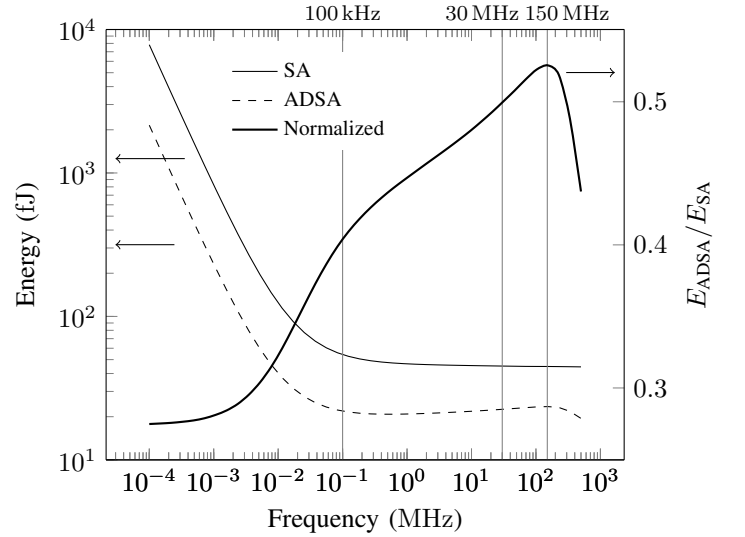


Fig. 5. Energy per conversion for the strongARM (SA) comparator and the adiabatically driven strongARM (ADSA). On the right axis, the energy of the ADSA normalized to the energy of traditional strongARM.

$< 100\text{ kHz}$, the normalized energy consumption converges to ≈ 0.28 . The energy consumption at such low-frequencies is dominated by leakage currents. As such, it is postulated that the ADSA has only 28 % of the leakage energy consumption with respect to the SA, thanks to the modulation effect of PC mentioned earlier. In the range between 100 kHz and 30 MHz, the leakage is not the primary component of the total energy consumption (dynamic energy and kickback currents based energy start to be relevant), and the normalized energy consumption rises with the frequency. Although this behavior is to be expected, the normalized energy consumption is less than the 0.5 minimum dictated by Equation (8). This fact signifies that in the 100 kHz to 30 MHz range, the energy consumption is not dominated by the dynamic energy component analyzed in Section IV-A, but rather by energy consumption arising from kickback currents. Kickbacks currents are one of the main drawbacks of the strongARM topology, and arise from the parasitics capacitors that couple the input nodes and nodes P , Q , and S [3]. For frequencies between 30 MHz and 150 MHz, the dynamic energy consumption becomes the dominant component, and the total energy consumption follows Equation (8). After 150 MHz, the energy of the ADSA decreases, due to the fact that the outputs are not rail-to-rail at such high frequencies. Shortly after that, both the SA and the ADSA reach their limit frequency of 500 MHz.

The noise behavior, obtained through periodic steady state simulations, is shown in Figure 6: the input referred noise of the ADSA presents the same profile as the input referred noise of the SA. The adiabatically driven strongARM presents a maximum of 2 % increase input referred noise with respect to the strongARM comparator.

The method proposed in [8] is used with the correlation coefficients reported in Table I on the pre-layout netlist. The value of 0.75 for the correlation coefficient is chosen because it is equivalent to two interdigitated transistors with four

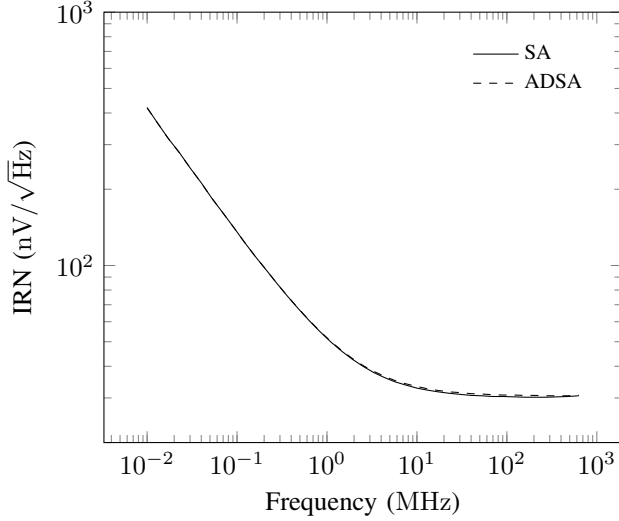


Fig. 6. Input referred noise, IRN, for $V_{CM} = 0.6$ V.

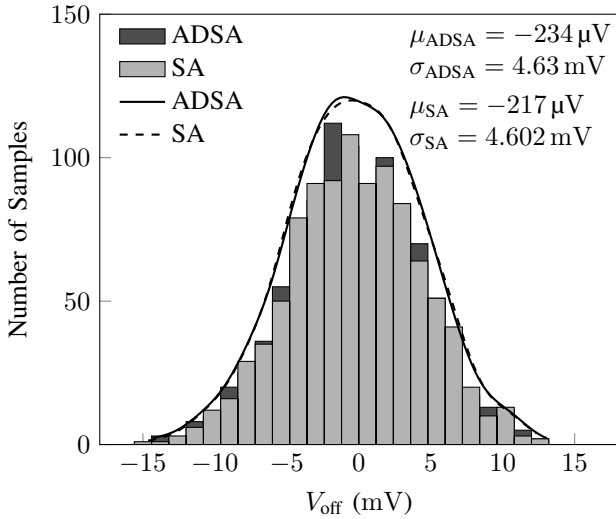


Fig. 7. Input offset voltage of the traditional (SA) and adiabatically driven (ADSA) strongARM comparator, as resulting from a 1000 runs monte carlo analysis, at 500 MHz and with $V_{CM} = 0.6$ V.

fingers [9]. The value of the correlation coefficients is arbitrary and cannot be used to compare the offset value with state-of-the-art comparators. Regardless, the goal of these simulations is to show how the strongARM comparator behaves when driven adiabatically, and how that changes its input offset voltage. To that end, Figure 7 shows the results of 1000 monte carlo simulations of the SA and ADSA, operating at its maximum frequency of 500 MHz. The average value μ in Figure 7 shows that the input offset voltage of the strongARM comparator, when driven adiabatically, changes by less than 1 %. Simulations of the extracted netlists are also carried out across corners and temperature variations. Both the ADSA and the SA comparators operate from -25°C to 125°C , and the minimum common-mode voltage V_{CM} for correct operation is 600 mV. Figure 8 shows the energy consumption of the DSA normalized to the energy consumption of the SA, for different temperature and at different corners. The ADSA consumes

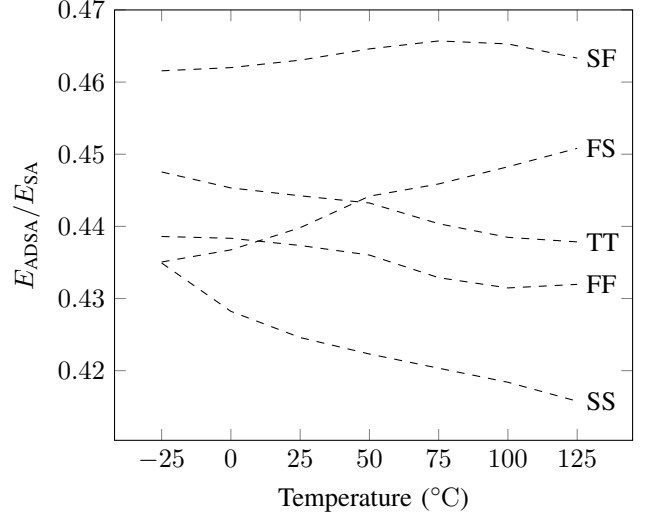


Fig. 8. Normalized energy consumption at 500 MHz, with $V_{CM} = 600$ mV and $V_{in} = 5$ mV, across PVT variations.

between 41.5 % and 46.6 % of the SA between -25°C and 125°C , across all the corners.

VII. CONCLUSIONS

This brief presents an analysis of the strongARM comparator driven adiabatically. The circuit consist of the classic strongARM comparator topology, driven with a sinusoidal signal instead of a DC voltage. The adiabatically driven strongARM presents the same characteristics of the traditional strongARM in terms of noise, input offset voltage, process and temperature variations, while consuming less than 55 % of the energy of the traditional strongARM. Future work includes investigating system level (e.g. in a flash ADC implementation) generation and synchronization of *clk* and *PC*, as well as the impact of adiabatic logic in the control/conversion circuitry of an ADC.

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